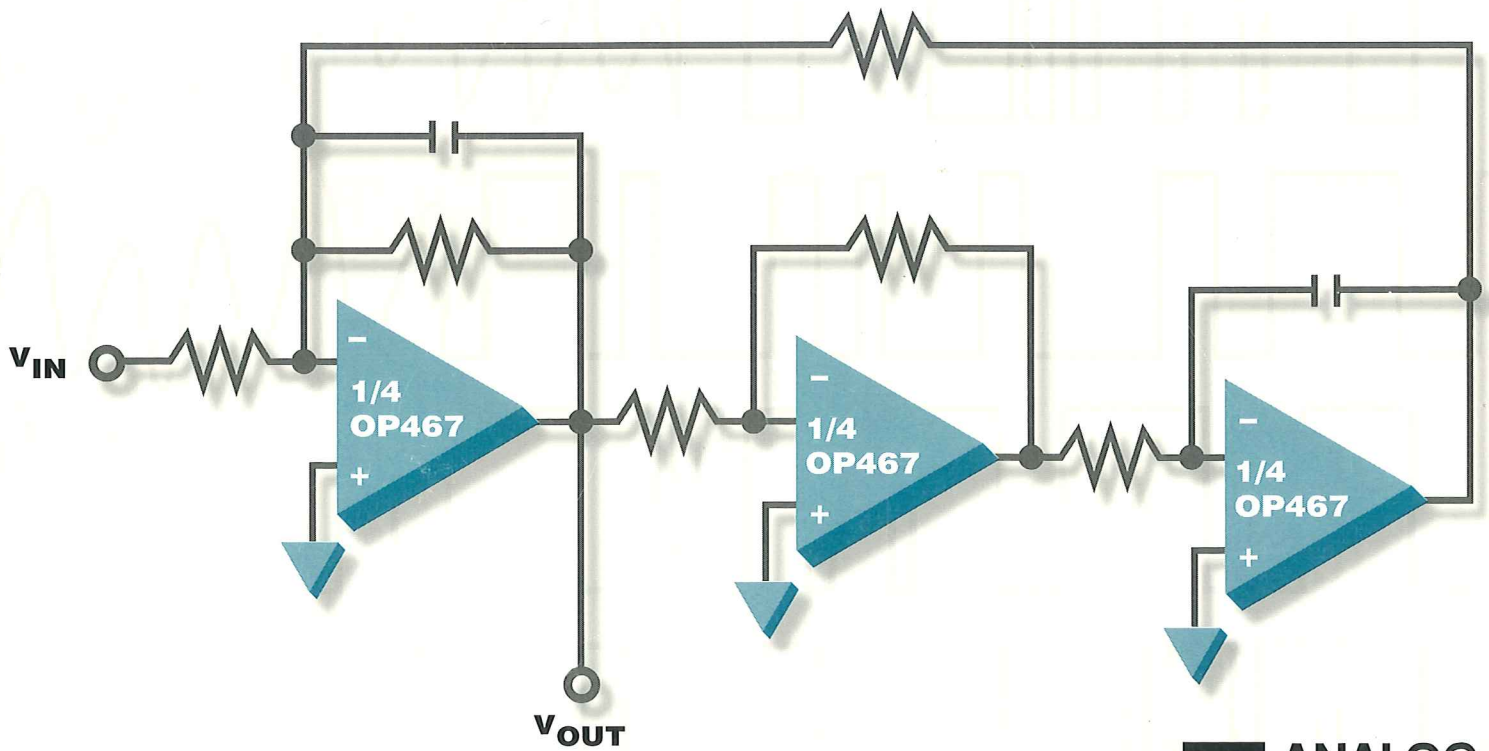
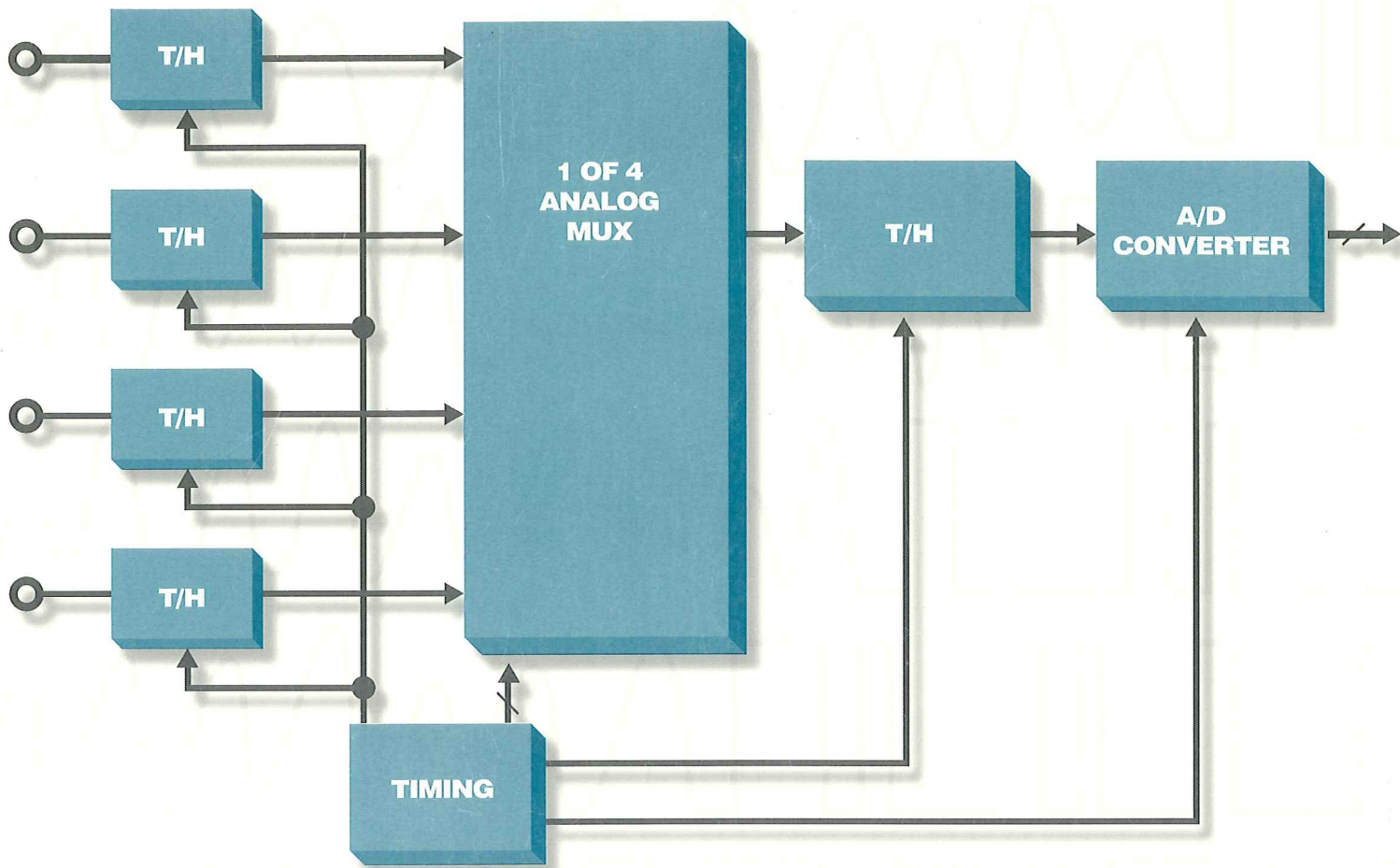


# LINEAR DESIGN SEMINAR



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# LINEAR DESIGN SEMINAR



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## SECTION 1

1

## OPERATIONAL AMPLIFIERS

*James Bryant, Walt Kester*

This section describes operational amplifiers and discusses their structure and specifications. It is hard to decide which to discuss first, since discussion of specifications, to be useful, entails reference to structures, and discussion of structures likewise requires reference to the performance feature that they are intended to optimize.

Since the majority of readers will have at least some familiarity with operational amplifiers and their specifications, we shall discuss structures first, and assume that readers will have at least a first-order idea of the definitions of the various specifications. Where this assumption proves ill-founded, the reader should look ahead to verify any definitions required.

## OPERATIONAL AMPLIFIERS

- Structure and Specifications are Interdependent
- In this section, we look at
  - ◆ Structures First: Input and Output
- THEN
- ◆ Specifications

Figure 1.1

## DEFINITION OF AN OP AMP

An Operational Amplifier (hereafter referred to as an "op amp") is an amplifier with a differential input having high common-mode rejection, and high, but not particularly stable or well-defined, differential gain. In most applications, its closed loop gain is stabilized by large amounts of negative feedback. Op amps have positive and negative supplies, but few, if any, have a ground connection, so the output does not have its own reference potential.

In the past, high precision op amps have sometimes been referred to as

"instrumentation grade" op amps, but this term can give rise to misunderstandings and should be discouraged. An instrumentation amplifier (hereafter referred to as an "in-amp") is not an op amp (see Figure 1.2). An in-amp, like an op amp, has a high impedance differential input with high common-mode rejection, but its gain is *accurately defined* without the need for an external network to provide the negative feedback to its inputs. Almost all in-amps have an output voltage reference pin.

## THE OP AMP IS NOT AN INSTRUMENTATION AMP

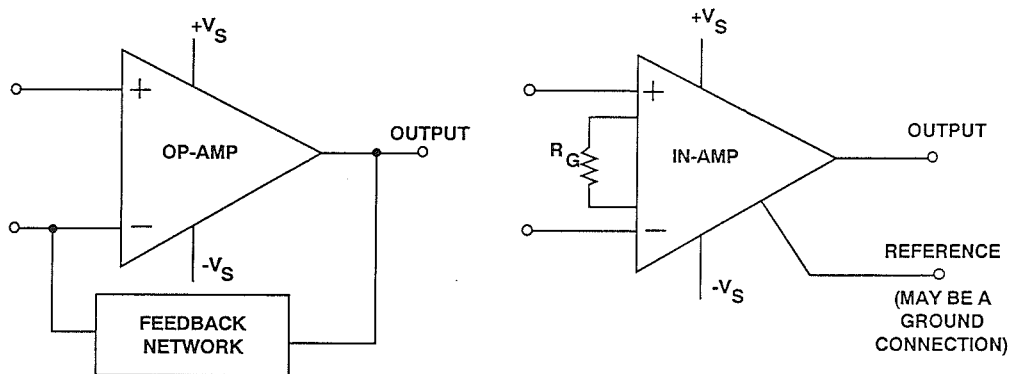


Figure 1.2

The most common type of in-amp is made with three op-amps and seven precision resistors as shown in Figure 1.3. In the past, a common use of quad op amps was the construction of in-amps, but today it is cheaper to use an IC in-amp. The performance of an in-amp is critically dependent on the

matching of its resistors. For instance, if a common mode rejection ratio (CMRR) of only 80 dB is required, the cost of the necessary 0.01% ratio-matched resistors will be much greater than the cost difference between an IC in-amp with on-chip trimmed resistors and a quad op amp.

## THREE OP-AMP INSTRUMENTATION AMP

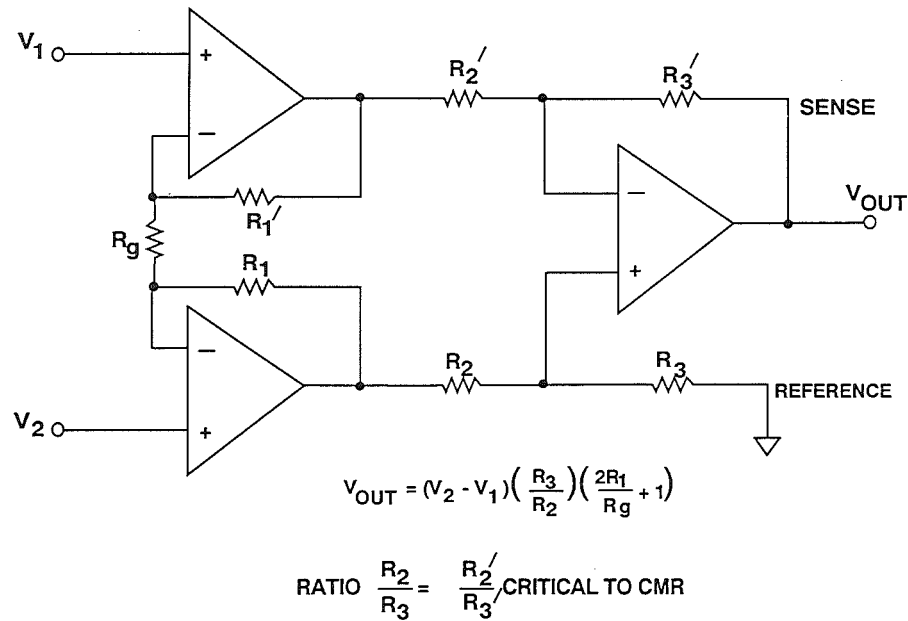


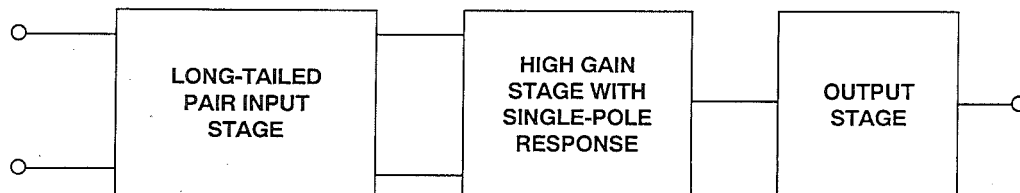
Figure 1.3

## STRUCTURE OF CLASSICAL (VOLTAGE FEEDBACK) OP AMPS

The first operational amplifiers were manufactured in the 1940s and 1950s and used thermionic valves (vacuum tubes), but their basic structure was essentially similar to modern voltage feedback op amps and is shown in Figure 1.4. The input stage consisted of

a long-tailed pair (a differential input/differential output structure having good common-mode rejection). There was then a high gain stage with a single pole frequency response, and finally a single-ended output stage.

### VOLTAGE FEEDBACK OP AMP STAGES



MODEL

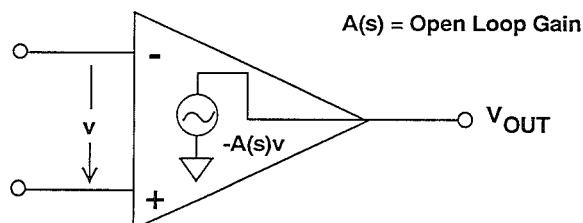


Figure 1.4



The op amp's gain to the differential input voltage,  $v$ , is its *open loop voltage gain*  $A(s)$ .  $A(s)$  is a dimensionless quantity and is expressed as number or in dB.  $A(s)$  is usually a large quantity (in most cases 100,000 or greater) and is a function of frequency. The op amp operating in the open loop mode as shown in Figure 1.4 is not very useful (except, under certain conditions, as a comparator). A small amount of input voltage will cause the output of the op

amp to swing to one of the supply rails (depending on the input polarity) and saturate. By applying negative feedback from the output of the op amp to the inverting input using a feedback network, we create the classical *closed loop* configurations shown in Figure 1.5. We will now define some important parameters associated with feedback circuits: *feedback factor*, *noise gain*, and *loop gain* (see Reference 1).

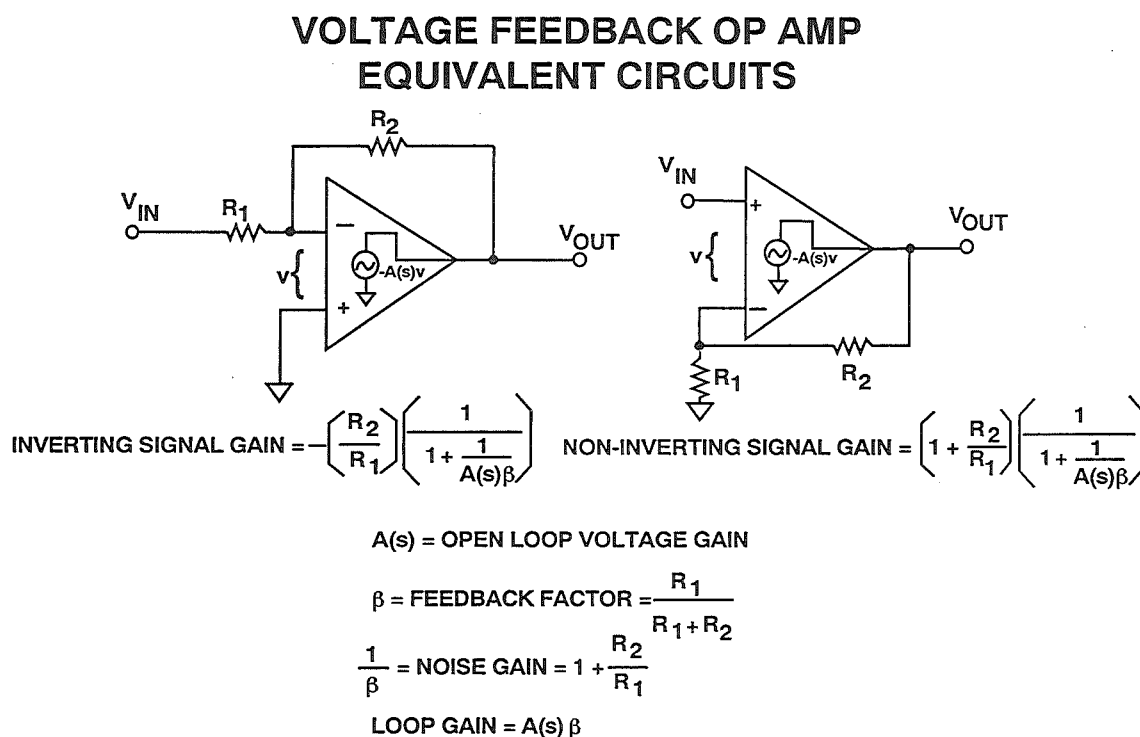


Figure 1.5

The *feedback factor* is the ratio of the output signal to the signal fed back to the inverting input and is given by

$$\beta = \frac{R_1}{R_1 + R_2}$$

The reciprocal of the feedback factor is the *noise gain* of the circuit. It is called this because it represents the voltage

gain to the output of a voltage noise source in series with the op amp input terminals.

$$\text{Noise Gain} = \frac{1}{\beta} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1}$$

Notice that the signal fed back from the output is attenuated by the feedback factor  $\beta$  and is then amplified by  $A(s)$ . The total gain of the loop is  $A(s)\beta$ , or the

loop gain. The loop gain is a measure of how closely the amplifier approaches the ideal. This can be seen by examining the closed-loop signal gain expressions in Figure 1.5. In the case of the inverting mode,

$$\text{Signal Gain} = -\frac{R_2}{R_1} \left( \frac{1}{1 + A(s)\beta} \right)$$

The greater the loop gain,  $A(s)\beta$ , the closer the op amp is to ideal performance. In an ideal op amp,  $A(s) = \infty$ , and the signal gain is  $-R_2/R_1$ . In practice, either a greater  $A(s)$  or a greater  $\beta$  (more feedback) maximizes  $A(s)\beta$ .

It is the value of the loop gain at a specified frequency which will determine the overall accuracy of the op amp at that frequency. As the frequency increases, the loop gain decreases, causing a loss of accuracy and linearity.

If the op amp has a single-pole open-loop gain response and gain is plotted in dB versus the logarithm of the frequency, then the open-loop gain decreases at a rate of 6dB/octave starting at the corner frequency defined by the pole. The loop gain  $A(s)\beta$  decreases at the same rate.

Since the gain stage is embedded in the amplifier, it is rarely of concern to the end-user, so we shall mainly be concerned with the input and output stages. All classical voltage feedback op amps use a long-tailed pair as an input stage. Its basic structure is a pair of matched amplifying devices, current fed in their joined cathodes (or emitters or sources), with the differential input applied to their grids (or bases or gates), with the output appearing as a differential current in their anodes (or collectors or drains) (see Figure 1.6).

## A TYPICAL OLD FASHIONED LONG-TAILED PAIR

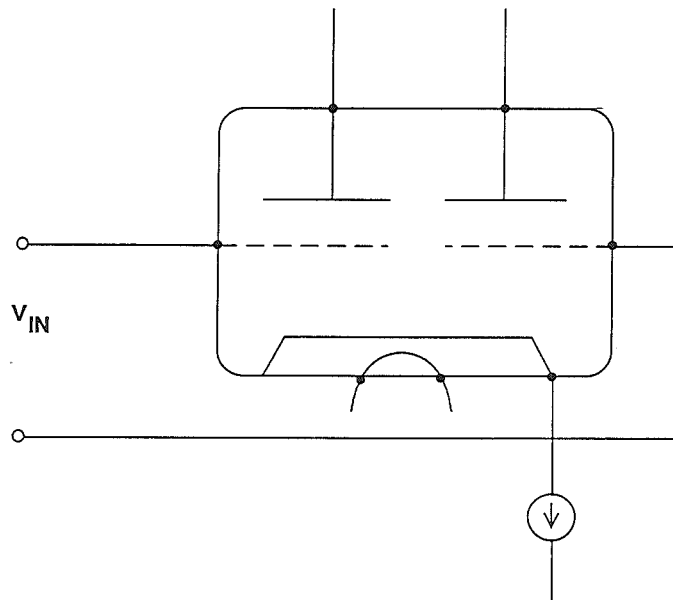


Figure 1.6

Since valves (tubes) are rarely used today, we shall consider the structures used in monolithic op amps, starting

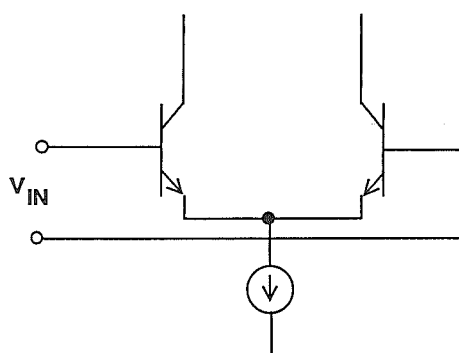
with the simple bipolar transistor input stage.

## Bipolar Input Stage

The basic bipolar input stage shown in Figure 1.7 consists of a long-tailed pair built with bipolar transistors. It has a number of advantages: it is simple, has very low offset, the bias currents in the inverting and non-inverting inputs are well-matched and do not vary greatly with temperature, and minimizing the

initial offset voltage of a bipolar op amp by laser trimming also minimizes its drift over temperature. This architecture is used by the earliest monolithic op amps such as the  $\mu A709$ , as well as some modern high-speed types like the AD817.

### BIPOLAR TRANSISTOR INPUT STAGE



- Low Offset: As Low as  $10\mu V$
- Low Offset Drift: As Low as  $0.1\mu V/^{\circ}C$
- Temperature Stable  $I_{bias}$
- Well-Matched Bias Currents
- Low Voltage Noise: As Low as  $1nV/\sqrt{Hz}$
- High Bias Currents:  $50nA - 10\mu A$
- (Except Super-Beta:  $50pA - 5nA$ , More Complex and Slower)
- Medium Current Noise:  $1pA/\sqrt{Hz}$

Figure 1.7

The input bias current is the base current of the long-tailed pair. It can be quite high, especially in high speed amplifiers, because the collector currents are high. The current noise of a bipolar input op amp is not particularly low.

The bias current of a simple bipolar input stage may be reduced by using *super-beta* transistors. These are devices with a very narrow base region

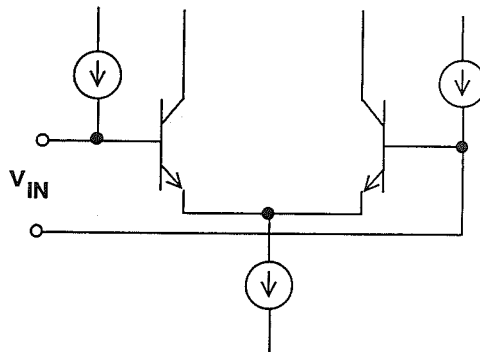
and a current gain of thousands or tens of thousands, rather than the more usual hundreds. Operational amplifiers with super-beta input stages have lower bias currents, but they have limited frequency response. Since the breakdown voltages of super-beta devices are quite low, they require additional circuitry to protect the input stage from damage caused by over-voltage. The AD705 and OP-97 are typical high performance super-beta op amps.

## Bipolar Bias Current Compensated Input Stage

The simple bipolar input stage exhibits high bias current because the bias currents are the base currents of the input transistors. If we provide the necessary bias current by means of a current source at each input (see Figure 1.8), the only *external* current flowing in

the input terminals is the difference current between the base current and the current source. This can be quite small. The well-known OP-07 and all its family are examples of bias compensated op amps.

### BIAS-CURRENT COMPENSATED BIPOLAR INPUT



- Low Offset Voltage: As Low as  $10\mu\text{V}$
- Low Offset Drift: As Low as  $0.1\mu\text{V}/^\circ\text{C}$
- Temperature Stable  $I_{\text{bias}}$
- Low Bias Currents:  $< 0.5 - 10\text{nA}$
- Low Voltage Noise: As Low as  $1\text{nV}/\sqrt{\text{Hz}}$
- Poor Bias Current Match (Currents May Even Flow in Opposite Directions)
- High Current Noise
- Not Very Useful at HF

Figure 1.8

Bias current compensated input stages have many of the good features of the simple bipolar input stage: low voltage noise, low offset, and low drift. Additionally, they have low bias current which is fairly stable with temperature. However, their current noise is not very good, and their bias current matching is poor. These features result from the external bias current being the *difference* between the current source and the input transistor base current. Both of these currents inevitably have noise. Since they are uncorrelated, the two noises add (root sum of squares), even though the currents subtract.

Since the external bias current  $I_b$  is the difference between two nearly equal currents, there is no particular reason why the net current should have any particular polarity, so the bias currents of bias-compensated op amps may not only be mismatched, they may actually flow in opposite directions! In most applications this is not important, but in some it can have unexpected effects (for example the droop of a sample-and-hold (SHA) built with a bias-compensated op amp may have either polarity).

## FET Input Stages

Field-Effect Transistors (FETs) have much higher input impedance than bipolar junction transistors (BJTs) and would therefore seem to be ideal devices for op amp input stages. However, they cannot be manufactured on all bipolar IC processes, and when a process allows their manufacture, they have their own problems.

FETs have high input impedance, low bias current, and good high frequency performance (the lower  $g_m$  of the FET devices allows higher tail currents, thereby increasing the slew rate of the op amp). FETs also have low current

noise. The offset of FET long-tailed pairs, however, is not as good as the offset of BJTs, and trimming for minimum offset does not minimize drift. A separate trim is needed for drift, and as a result, offset and drift in a JFET op amp, while good, are not as good as the best BJT ones (see Figure 1.9). It is possible to make JFET op amps with very low voltage noise, but the devices involved are very large and have quite high input capacitance, which varies with input voltage, and so a trade-off is involved between voltage noise and input capacitance.

### JUNCTION FIELD EFFECT TRANSISTOR (JFET) INPUT OP AMP STAGE SHOWING OFFSET AND DRIFT TRIMS

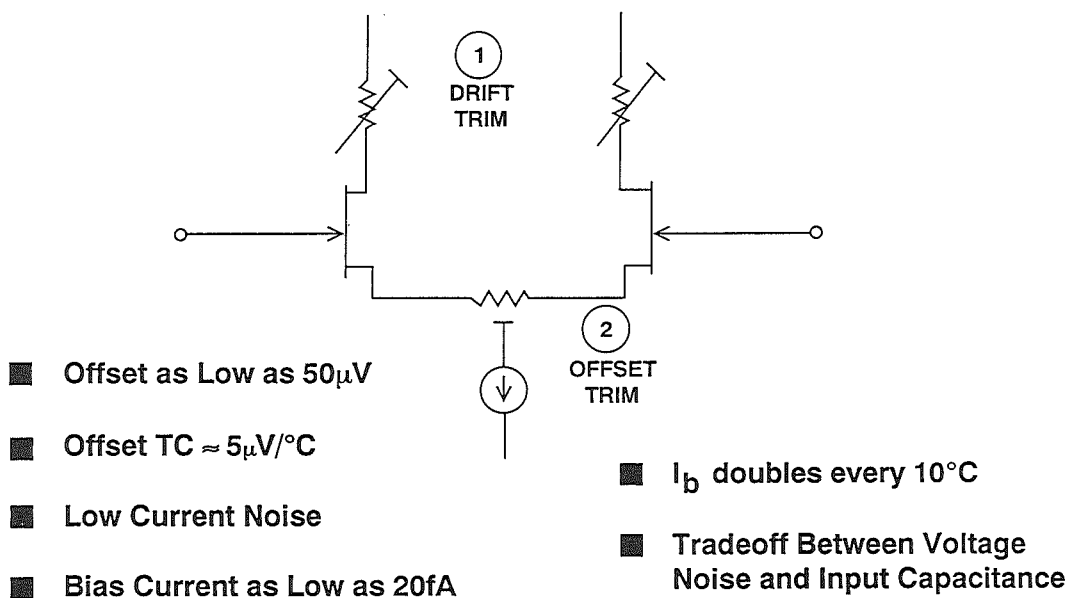


Figure 1.9

The bias current of an FET op amp is the leakage current of the gate diffusion (or the leakage of the gate protection diode, which has very similar characteristics, in the case of a MOSFET). Such leakage currents double with every  $10^{\circ}C$  increase in chip temperature so

that the bias current of an FET op amp is ONE THOUSAND TIMES GREATER at  $125^{\circ}C$  than at  $25^{\circ}C$ . Obviously this can be important when choosing between a bipolar or FET input op amp, especially in high temperature applications.

In speaking of FET op amps, we have spoken generally of all kinds of FETs, both junction (JFETs) and MOS (MOSFETs). In practice, op amps using bipolar technology and JFETs (BiFET and similar technologies) have far better performance than op amps using MOSFET or CMOS technology. One or two manufacturers do make very high performance op amps with MOS or CMOS input stages, but in general, MOS and CMOS op amps have poor offset and drift, poor voltage noise, and poor high-frequency performance, and even their power consumption is barely

lower than that of bipolar op amps with comparable, or even better, performance. (CMOS is a low-power process when used for logic because it does not pass current except when switching, but an op amp requires a standing or quiescent current, therefore a CMOS op amp is not intrinsically low power.)

JFETs require more headroom than BJTs and are more difficult to operate at very low power supply voltages, since their pinchoff voltage is typically greater than a BJT's base-emitter voltage.

## JFET VERSUS MOS / CMOS OP AMPS

- MOS and CMOS are not very good linear processes (with a few exceptions).
- They have poor offset voltage, drift, voltage noise and output drive, but Input Bias Current is very low.
- Although they can be low power, better performance at similar power can often be achieved with bipolar processes.

Figure 1.10

## Chopper Stabilized Op Amps

The best bipolar op amps may have guaranteed offsets as low as  $10\mu\text{V}$ . If offsets lower than this are required, a different op amp topology is necessary. This is "chopper stabilization" - the input signal is converted to AC by modulation, amplified, and demodulated. Any offsets in the system are eliminated in the modulation/demodulation process.

Early chopper stabilized amplifiers actually used relays to chop the signal, but today such amplifiers are mono-

lithic and use MOS switches to do the job. Early monolithic amplifiers of this type had high noise at the chopping frequency (which may be between a few hundred Hz and a few tens of kHz). This high-frequency noise is less of a problem in the latest devices, which may contain quite effective filters at the chopper frequency (although careful layout and supply decoupling is still important with these parts), but switching noise is still the major problem with chopper stabilized op amps.

### CHOPPER STABILIZED OP AMPS

- Use fairly fast switches to convert inputs into AC which is amplified and then demodulated
- Negligible DC errors result (zero offset voltage)
- Very noisy because of chopping action, therefore output must be heavily filtered or averaged
- Low Offset almost impossible to realize except at frequencies  $< 0.1\text{Hz}$

Figure 1.11

Because of the technology used to manufacture them (frequently CMOS), many chopper-stabilized op amps have a voltage noise of several  $\mu\text{V}$  in the band 0.1-10 Hz, and it is therefore necessary to integrate their output for several seconds or tens of seconds if we wish to obtain the low offset of the which they are potentially capable. Not all systems allow such long integration times, and so a compromise becomes

necessary between offset and speed. For many applications, a bipolar op amp such as the OP-177, which has  $10\mu\text{V}$  offset and low voltage noise, may be more practical. There is no doubt, however, that in applications where long integration times are acceptable, a chopper-stabilized op amp has virtually zero offset, less bias current than a bipolar op amp, and is the device of choice.

### PRECISION OP AMP VERSUS CHOPPER: A COMPARISON OF CRITICAL PARAMETERS

	BIPOLAR	CHOPPER
OFFSET VOLTAGE	10-50 $\mu\text{V}$	<5 $\mu\text{V}$
OFFSET DRIFT	0.1 $\mu\text{V}/^\circ\text{C}$	~0 $\mu\text{V}$
OPEN LOOP GAIN	10 Million	10 Million
NOISE: HF GLITCH	None	>100mVp-p
NOISE: 0.1-10Hz	<0.2 $\mu\text{Vp-p}$	>1 $\mu\text{Vp-p}$
COST	Lower	Higher
EXTERNAL COMPONENTS	None	Some Require 2 Caps.
SATURATION RECOVERY	10-20 $\mu\text{s}$	>100ms to seconds

Figure 1.12



## Rail-Rail Input Stages

With increasing emphasis on low voltage and single-supply operation, there is a demand for op amps whose input common-mode range includes both supply rails. Such a feature is undoubtedly useful in some applications, but engineers should recognize that there are relatively few applications where it is absolutely essential. These should be carefully distinguished from the many applications where common-mode range *close* to the supplies is necessary, but rail-rail is not.

The problem is that a true rail-rail input stage requires two long-tailed

pairs (see Figure 1.14), one of NPN BJTs (or N-channel FETs), the other of PNP (or P-channel devices). These two pairs have different offsets and bias currents, so that as the common-mode voltage changes so does  $V_{OS}$  and  $I_b$ . This results in relatively poor CMRR and common-mode  $Z_{in}$ . These specifications should be considered carefully when choosing a rail-rail input op amp for a non-inverting configuration.  $V_{OS}$ ,  $I_b$ , and even CMRR may be quite good over part of the common-mode range and much worse in the region where operation shifts between the NPN and PNP devices.

## RAIL-TO-RAIL INPUT STAGES

- Require two long-tailed pairs with inputs in parallel:  
     One with NPN BJTs (or P-Channel FETs)  
     One with PNP BJTs (or N-Channel FETs)
  - $V_{OS}$ ,  $I_b$ , and CMRR varies over their common mode range
- OR
- An on-chip inverter may be used to generate a power rail outside the external power supplies, but this adds noise.
  - It is often possible to use an op amp which allows the input signal to go to only *one* of the rails (usually ground)

Figure 1.13

## OP-291 RAIL-TO-RAIL BIPOLAR INPUT STAGE

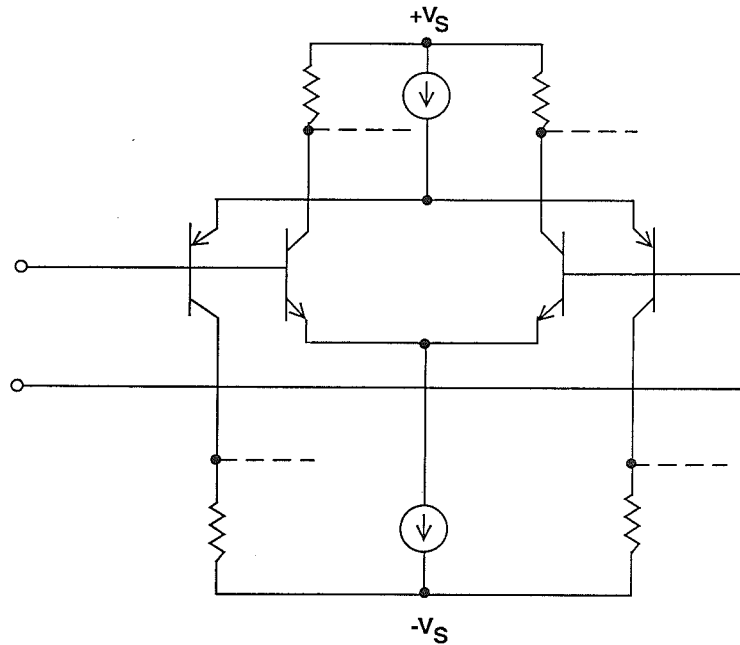


Figure 1.14

It is possible to make a monolithic op amp with a true rail-rail input using only NPN (or only PNP) transistors (or the corresponding FETs). This requires a small inverter on the chip to produce a power rail *outside* the external power supplies. Amplifiers of this type are not common, but do have good CMRR, and stable  $V_{OS}$ . Their problem is inverter noise — like chopper amplifiers they have an internal oscillator, and its signal tends to leak, even with careful decoupling.

In general, applications which appear to require true rail-rail inputs should be carefully evaluated to see if other techniques are possible. If they are not,

the amplifier should be chosen very carefully to ensure that its  $V_{OS}$ ,  $I_b$ , CMRR and noise (voltage and current) are suitable for the application involved.

In many single-supply applications, it is required that the input go to only *one* of the supply rails (usually ground). Amplifiers which will handle zero-volt inputs are relatively easily designed using either PNP transistors (see OP-90 in Figure 1.15) or N-channel JFETs (see AD820 in Figure 1.16). P-channel JFETs can be used where inputs must include the positive supply rail (but not the negative rail) as shown in Figure 1.16 for the OP-282/OP-482.

## OP-90 PNP INPUT STAGE ALLOWS INPUT TO GO TO THE NEGATIVE RAIL

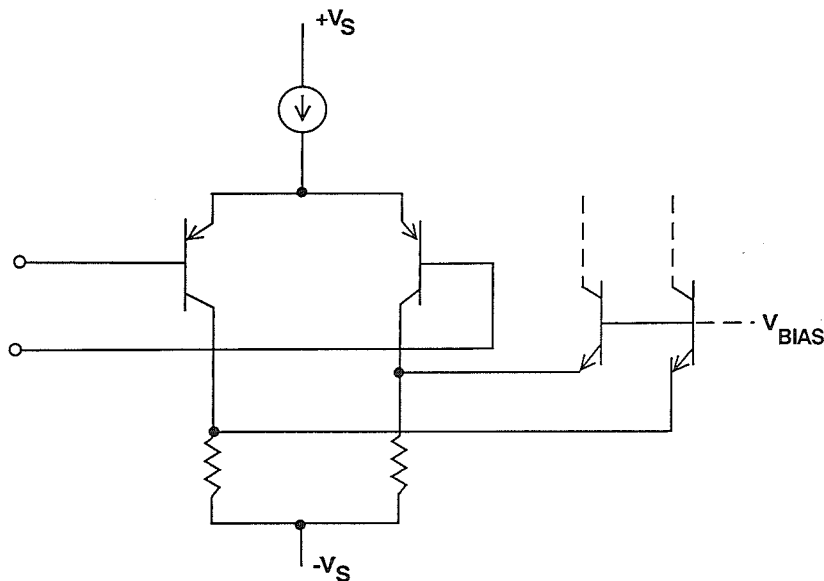


Figure 1.15

## AD820/AD822 INPUT CAN INCLUDE NEGATIVE RAIL, OP-282/OP-482 CAN INCLUDE POSITIVE RAIL

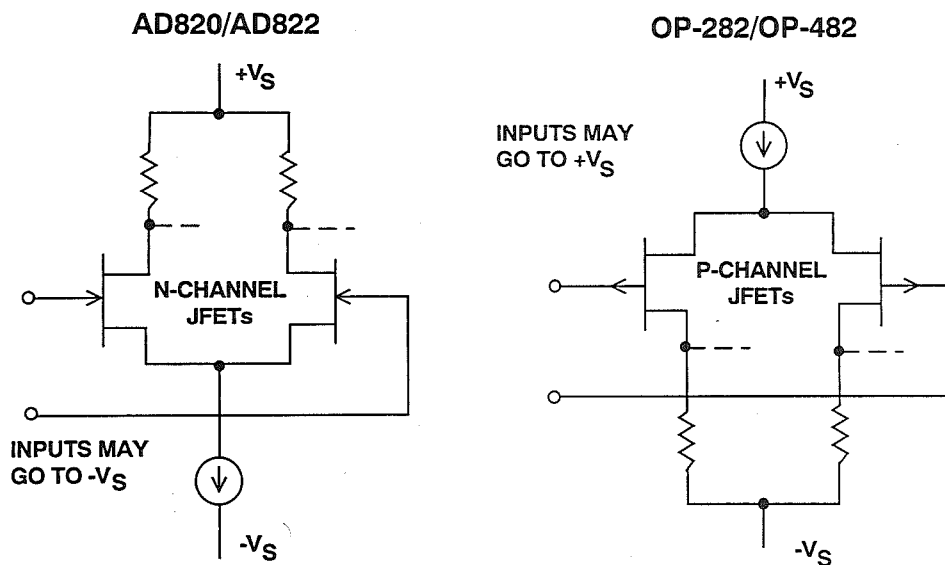


Figure 1.16

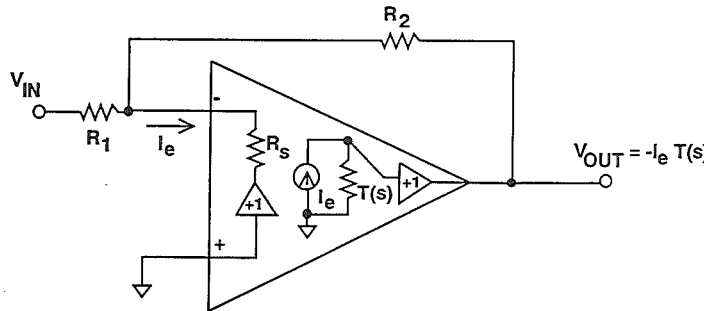
## Transimpedance (Current-Feedback) Op Amps

A new type of high-frequency op amp has recently become popular: the *transimpedance* or *current feedback* op amp. We shall not discuss the reasons for its popularity in this section, other than to mention that under certain conditions, it has superior high frequency (HF) performance to the older (voltage feedback) architecture. (See Reference 3.)

The equivalent circuit for a current feedback amplifier is shown in Figure 1.17. Like the voltage feedback op amp, the current feedback type has inverting and non-inverting inputs. It differs from the voltage feedback op amp in that the two inputs are not identical in struc-

ture. The non-inverting input of a current feedback amplifier is a high impedance node, just as that of a voltage feedback op amp, but the inverting input is a low impedance, current input node. The signal at the non-inverting input is applied to the inverting input through a unity-gain buffer. Ideally, the inverting input is held at the same potential as the non-inverting and has zero input impedance. In practice, the input impedance  $R_s$  is of the order of a few tens of ohms, and there is an offset between the two inputs. This is comparable to the offset of a voltage feedback op amp, and may only be a few tens or hundreds of microvolts.

### CURRENT FEEDBACK (TRANSIMPEDANCE) OP AMP EQUIVALENT CIRCUIT



$$\text{INVERTING SIGNAL GAIN} = - \left( \frac{R_2}{R_1} \right) \left( \frac{1}{1 + \frac{1}{LG}} \right) \quad \text{NON-INVERTING SIGNAL GAIN} = \left( 1 + \frac{R_2}{R_1} \right) \left( \frac{1}{1 + \frac{1}{LG}} \right)$$

$T(s)$  = OPEN LOOP TRANSIMPEDANCE GAIN

$$\beta_{cf} = \text{FEEDBACK FACTOR} = \frac{R_s \parallel R_1}{R_s \parallel R_1 + R_2}$$

$$A_{cf}(s) = \text{OPEN LOOP VOLTAGE GAIN} = \frac{T(s)}{R_s}$$

$$\text{LOOP GAIN} = LG = A_{cf}(s) \beta_{cf} = \frac{T(s) \{ R_s \parallel R_1 \}}{R_s \{ R_s \parallel R_1 + R_2 \}}$$

Figure 1.17

The current entering the inverting input is multiplied by the *transimpedance open loop gain*,  $T(s)$ , to yield the output voltage. The *feedback factor* of the current feedback amplifier is different from the voltage feedback amplifier because of the low inverting input impedance,  $R_S$ . Solving the feedback equation yields the transfer function shown in Figure 1.17. Although the

expression for the current feedback amplifier loop gain is different from a voltage feedback amplifier, it can be used in exactly the same manner in determining the accuracy of the amplifier closed loop gain at any specific frequency. Figure 1.18 shows a simplified schematic of the AD846, a typical current feedback op amp.

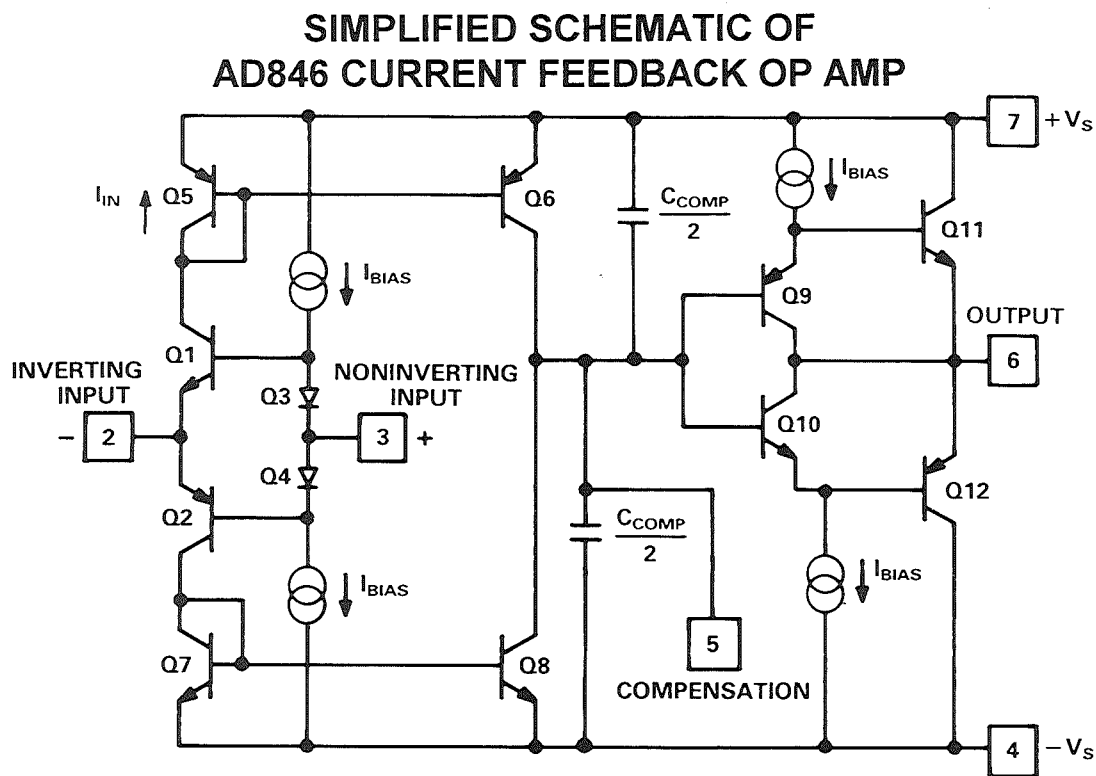


Figure 1.18

## Comparison Between Voltage Feedback and Current Feedback Op Amps

The inverting mode transfer functions for the voltage feedback amplifier and the current feedback amplifier are compared in Figure 1.19. Notice that for the voltage feedback amplifier, the frequency-dependent term,  $1/A(s)$ , is multiplied by the noise gain of the

circuit,  $(1 + R_2/R_1)$ . This implies that the closed loop bandwidth is inversely proportional to the noise gain; hence, the product of the noise gain and the closed loop bandwidth is constant, i.e. there is a constant gain-bandwidth product.

# COMPARISON OF VOLTAGE FEEDBACK AND CURRENT FEEDBACK INVERTER CLOSED LOOP GAIN EQUATIONS

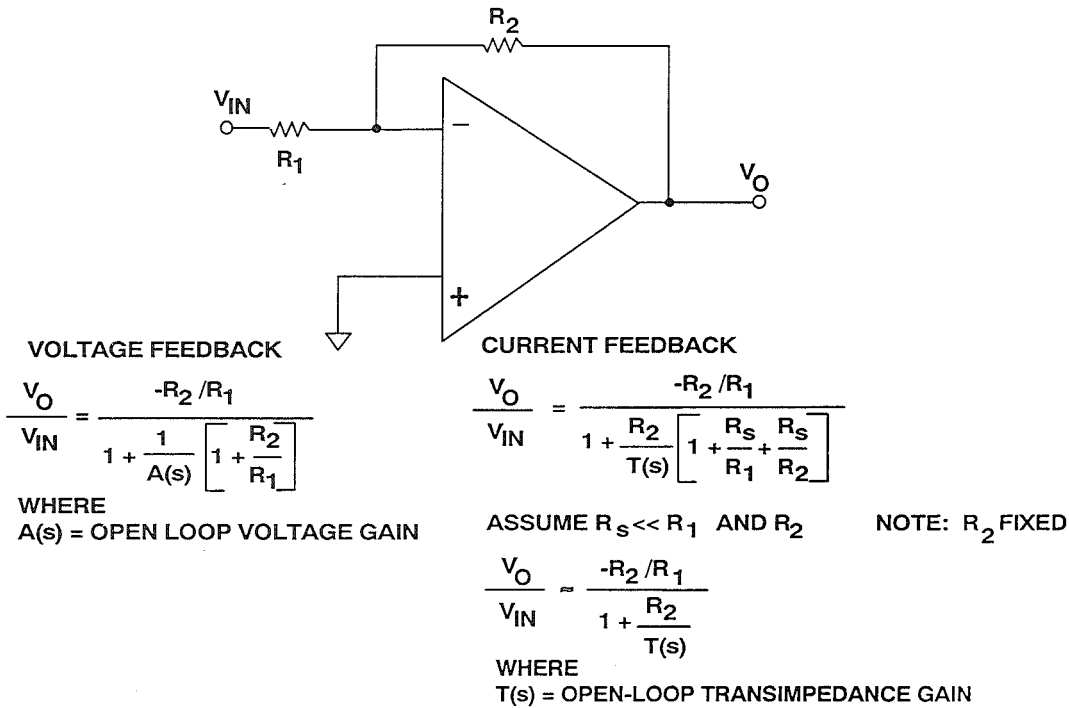


Figure 1.19

However, in the current feedback amplifier, if  $R_s \ll R_1$  and  $R_2$ , the closed loop bandwidth is relatively independent of the gain ( $R_2/R_1$ ) and depends only upon the feedback resistor,  $R_2$ . Furthermore, most current feedback amplifiers are optimized for maximum bandwidth with a particular value of  $R_2$ . This implies that the closed loop bandwidth of a current feedback amplifier will remain fairly constant regardless of closed loop gain, provided the gain is changed by varying only  $R_1$ . (Therefore, it is inappropriate to refer to the gain-bandwidth product of this type of amplifier). Increasing the feedback resistor,  $R_2$ , lowers the bandwidth proportionally, while decreasing the value may lead to instability.

The requirement of a fixed, low-value (typically 400Ω to 1000Ω) feedback resistor becomes a significant disadvantage when using a current feedback op

amp in the inverting mode at large gains. For example, with the AD9617 optimum feedback resistor  $R_2$  of 400Ω, the feedforward resistor  $R_1$  must be 40Ω to achieve an inverting gain of 10. Driving the low value feedforward resistor may become a significant problem. Therefore, the non-inverting configuration is generally preferable when using current feedback amplifiers at high gains.

There are several important consequences of this new structure: (1) the device does not have a “gain-bandwidth product”; (2) bias currents are comparatively large, unmatched, may flow in either direction (like a bias-compensated op amp, and for the same reason: the external bias current is the *difference* of two larger internal currents), and may vary differently with temperature; and (3) while the voltage noise may be low, the current noise at

the two inputs is quite high. Additionally, the two noise currents are neither equal nor correlated, and neither do they necessarily have the same  $1/f$  corner frequency.

These comments should not be interpreted as a condemnation of current feedback op amps, merely a warning that different considerations apply to their use than to the use of the classical voltage feedback amplifier. When properly used, they may offer wider

bandwidth, lower distortion, and lower voltage noise than a classical voltage feedback op amp. However, they are unstable with capacitive loads and capacitive feedback and may not be used in most classical active filter circuits. There is rarely any need to use current feedback amplifiers in DC or low frequency (LF) designs except perhaps as the output driver in a low noise, low distortion composite amplifier designed specifically for high current drive (Reference 2).

## **SUMMARY OF VOLTAGE FEEDBACK OP AMP CHARACTERISTICS**

- **Symmetrical Inputs**
- **Equalization of Source Resistances Generally Reduces Effects of Input Bias Currents (except where bias current cancellation techniques are used)**
- **Largest Noise Source may be Input Voltage Noise or Input Current Noise depending on Impedance Levels**
- **Flexible Feedback Networks Allow Many Tradeoffs**
- **Constant Gain-Bandwidth Product**
- **May be Used as Integrators in Active Filters**

**Figure 1.20**

## SUMMARY OF CURRENT FEEDBACK OP AMPS CHARACTERISTICS

- Non-Symmetrical Inputs (High Impedance Noninverting Input, Low Impedance Inverting Input)
- Input Bias Current Cancellation Schemes Don't Work because currents are poorly matched.
- Inverting Input Current Noise Usually Dominates
- Feedback Resistor Value Fixed for Optimum Performance
- Difficult to Use as Integrators (Oscillates with capacitive feedback)
- Bandwidth Remains Relatively Constant for Different Gains, therefore *Gain-Bandwidth Product* concept is meaningless
- Stray Capacitance on Inputs and Outputs will cause Peaking
- Offer no Advantage at DC or Low Frequencies

Figure 1.21

## EFFECTS OF OVERDRIVE ON OP AMP INPUTS

There are several important points to be considered about the effects of overdrive on op amp inputs. The first is, obviously, damage. The data sheet of an op amp will give "absolute maximum" input ratings for the device. These may be expressed in terms of the supply voltage, or may not, but, unless the data sheet expressly says otherwise, maximum ratings apply only when supplies are present, and inputs should be held near zero in the absence of supplies.

A common type of rating expresses input voltage in terms of the supply,  $V_{SS} \pm 0.3V$ . In effect, neither input may go more than 0.3V outside the supply rails, whether they are on or off. If current is limited to 5mA or less, it

generally does not matter if inputs do go outside  $\pm 0.3V$  *when the supply is off* (provided that no base-emitter reverse breakdown occurs). Problems may arise if the input is outside this range when the supplies are turned on - this can turn on parasitic SCRs in the device structure and destroy it within microseconds. This condition is called *latch-up*, and is much more common in digital CMOS than in linear processes used for op amps. If a device is known to be sensitive to latch-up, avoid the possibility of signals appearing before supplies are established. (When signals come from other circuitry using the same supply there is rarely, if ever, a problem.) Fortunately, most IC op amps are relatively insensitive to latch-up.



## INPUT STAGE OVERVOLTAGE

- INPUT SHOULD NOT EXCEED ABSOLUTE MAXIMUM RATINGS  
(Usually Specified With Respect to Supply Voltages)
- A Common Specification Requires the Input Signal  $< V_S \pm 0.3V$
- Input Voltage Should be Held Near Zero in the Absence of Supplies
- Input Stage Conduction Current Needs to be Limited  
(Rule of Thumb: 5mA)
- Avoid Reverse Bias Junction Breakdown in Input Stage  
Base-Emitter Junctions
- Differential and Common-Mode Ratings may Differ
- No Two Amplifiers are exactly the Same
- Some Op Amps Contain Input Protection (Voltage Clamps,  
Current Limits, or Both), but Absolute Maximum Ratings Must  
Still be Observed

Figure 1.22

**A SCHOTTKY DIODE CLAMP KEEPS THE  
INPUT (ALMOST) WITHIN THE SUPPLIES,  
AND A RESISTOR LIMITS INPUT CURRENT**

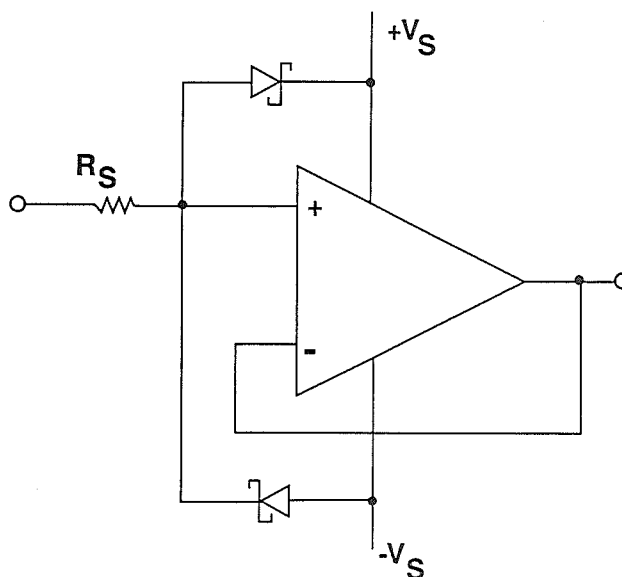


Figure 1.23

A common method of keeping the signal within the supplies is to clamp the signal to the supplies with schottky diodes as shown in Figure 1.23. This does not, in fact, limit the signal to  $\pm 0.3V$  at all temperatures, but if the schottky diodes are at the same temperature as the op amp, they will limit the voltage to a safe level, even if they do not limit it at all times to within the data sheet rating. This is easily accomplished if over-voltage is only possible at turn-on, and diodes and op amp will always be at the same temperature then. If the op amp may still be warm when it is repowered, however, steps must be taken to ensure that diodes and op amp are at the same temperature when this occurs.

Many op amps have limited common mode or differential input voltage ratings. Limits on common-mode are usually due to complex structures in very fast op amps and vary from device to device. Limits on differential input avoid a damaging reverse breakdown of the input transistors (especially super-beta transistors). This damage can occur even at very low current levels. Limits on differential inputs may

also be needed to prevent internal protective circuitry from over-heating at high current levels when it is conducting to prevent breakdowns - in this case, a few hundred microseconds of over-voltage may do no harm. One should never exceed any "absolute maximum" rating, but engineers understand the reasons for the rating so that they can make realistic assessments of the risk of permanent damage should the unexpected occur.

If an op amp is over-driven *within* its ratings, no permanent damage should occur, but some of the internal stages may saturate. Recovery from saturation is generally slow, except for certain "clamped" op amps specifically designed for fast over-drive recovery. Over-driven amplifiers may therefore be unexpectedly slow.

Because of this reduction in speed with saturation (and also output stages unsuited to driving logic), it is generally unwise to use an op amp as a comparator. Nevertheless, there are sometimes reasons why op amps may be used as comparators. The subject is discussed in Reference 3.

## INPUT STAGE OVERDRIVE

- Overdriving Op Amps (Within Absolute Maximum Ratings) does no Damage but may cause Saturation
- Saturation Recovery Times may be Long
- It is therefore Inadvisable to use Op Amps as Comparators (In General -- There may be Exceptions)

Figure 1.24

## OP AMP OUTPUT STAGES

The earliest IC op amp output stages were NPN emitter followers with emitter current sources or resistive pull-downs (see Figure 1.25). Naturally they were far faster with positive-going signals than with negative ones. While all modern op amps have push-pull output stages of some sort, many are still, to a greater or lesser degree, asymmetrical and have a greater slew rate in one direction than the other. This asymmetry, which generally results from the use of IC processes with better NPN than PNP transistors, may also result in an ability to approach one supply more closely than the other in terms of output voltage swing.

If a process can make relatively well-matched PNP and NPN transistors,

then its output limiting levels and slew rates will be reasonably well matched. However, an output stage using BJTs cannot swing completely to its rails, but only to within the transistor saturation voltage of the rails (see Figure 1.26). For small amounts of load current (less than  $100\mu\text{A}$ ), the saturation voltage may be as low as 5 to 10mV. For load currents of 10mA, the saturation voltage can increase to several hundred mV.

An output stage constructed of CMOS FETs can provide true rail-to-rail performance, but only under no-load conditions. If the output must source or sink current, the output swing is reduced by the voltage dropped across the FETs "on" resistance (typically  $100\Omega$ ).

OP AMP OUTPUT STAGES USING  
COMPLEMENTARY DEVICES ALLOW PUSH-PULL DRIVE

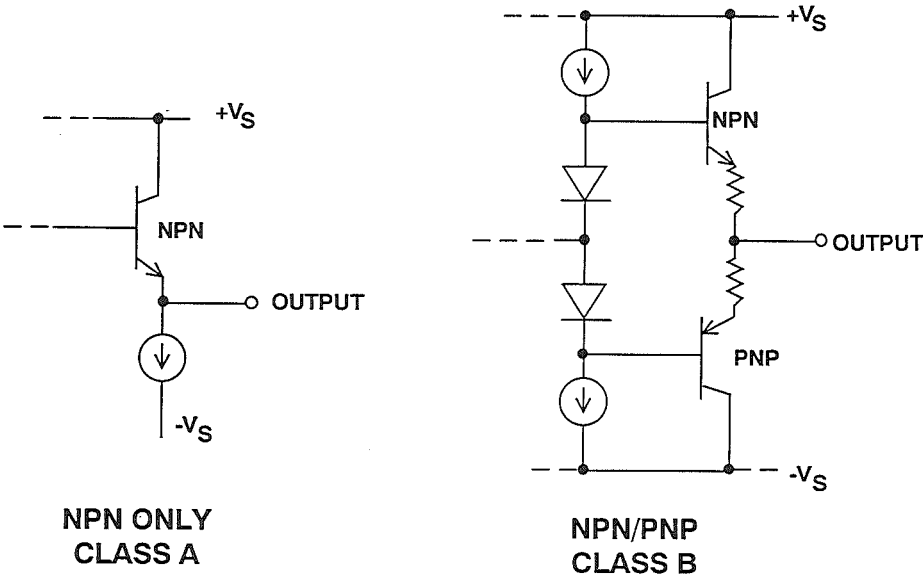


Figure 1.25

RAIL-TO-RAIL OUTPUT STAGES

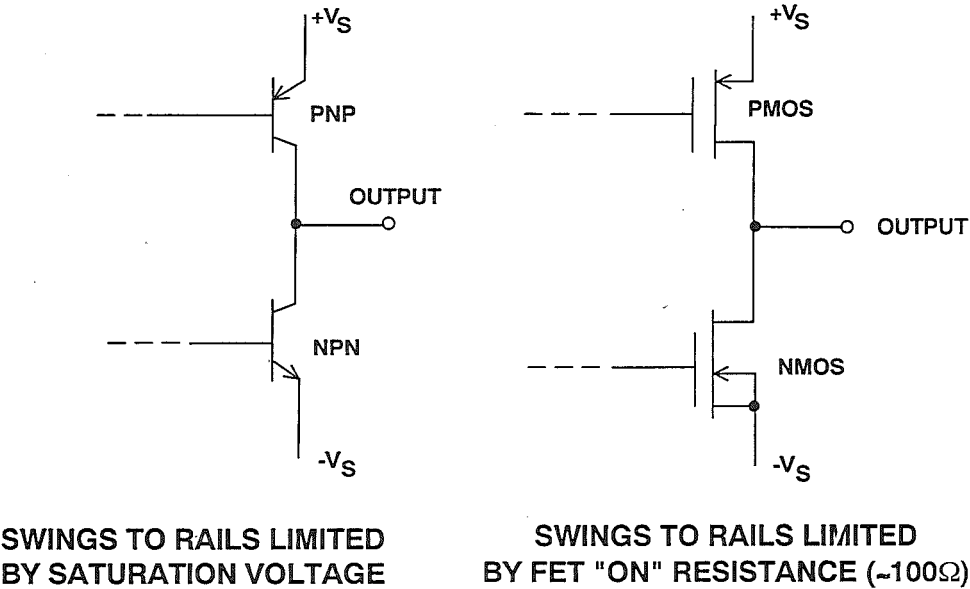


Figure 1.26

In many applications, it is only required that the output swing to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high

enough or is also grounded to that rail), but only slowly. An FET current source can replace the resistor and speed things up, but at a cost of increased complexity. CMOS and bipolar stages which will operate at the negative rail are shown in Figure 1.27.

## OUTPUT STAGES WHICH ALLOW "NEGATIVE RAIL ONLY" OPERATION ARE OFTEN SUFFICIENT

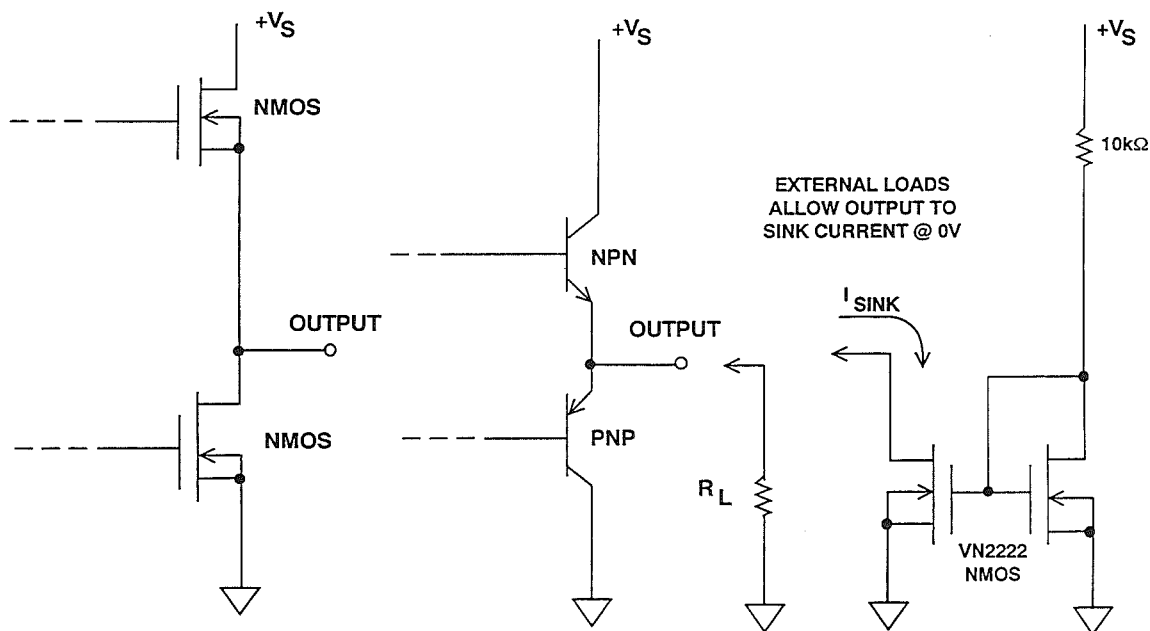


Figure 1.27

Low speed op amps generally have output stages which are protected against short circuits to ground or to either supply. Their output current is limited to a little more than 10mA. This has the additional advantage that it minimizes self-heating of the chip, and thus DC errors due to chip temperature differentials.

If an op amp is required with high precision and a large output current, it is advisable to use a separate output stage (within the loop) to minimize self-heating of the precision op amp. A simple medium power audio amplifier is often suitable. (There is an instrumen-

tation amplifier, not made by Analog Devices, which has a  $V_{OS}$  of  $50\mu V$  and an  $I_{out}$  of 50mA — but you can't have both at the same time!)

High speed op amps cannot have output currents limited to such a low value, since it would affect their slew rate and ability to drive low impedances. Most high speed op amps will source and sink between 50-100mA, and few are limited to less than 30mA. Although many high speed op amps have short circuit protection, junction temperatures may be exceeded (because of the high short circuit current) resulting in device damage for prolonged shorts.

## OP AMP OUTPUT STAGE PROTECTION

- Low Frequency op amps are generally protected against shorts to ground or either supply by a current limit of 10mA or greater.
- Op amps with high current outputs (including high speed op amps where current is needed to achieve high slew rate) are usually protected, but prolonged shorts may cause damage due to excessive junction temperatures.
- When high current *and* high precision are required, use a composite configuration with a precision op amp followed by a high current op amp (within the feedback loop). This avoids loss of accuracy due to non-uniform heating of the precision op amp chip.

Figure 1.28

## OP AMP SPECIFICATIONS

Although voltage feedback and current feedback op amps have similar error terms and specifications, the application of each part warrants discussing some

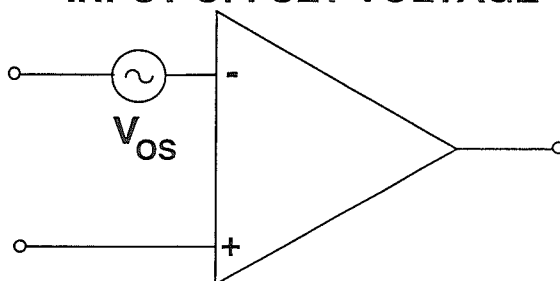
of the specifications separately. In the discussions to follow, this will be done where significant differences exist.

### Input Offset Voltage

Ideally, if both inputs of an op amp are at exactly the same voltage, then the output should be at zero volts. In practice, a small differential voltage must be applied to the inputs to force the output to zero. This is known as the “offset voltage”,  $V_{OS}$ . Input offset voltage is

modeled as a voltage source,  $V_{OS,in}$  series with the inverting input terminal of the op amp as shown in Figure 1.29. The corresponding output offset voltage (due to  $V_{OS}$ ) is obtained by multiplying the input offset voltage by the DC noise gain of the circuit  $(1 + R_2/R_1)$ .

## INPUT OFFSET VOLTAGE



- **Offset Voltage:** The differential voltage which must be applied to the input of an op amp to produce zero output.
- **Ranges:**
  - ◆ Chopper Stabilized Op Amps:  $< 1\mu V$
  - ◆ General Purpose Precision Op Amps:  $50 - 500\mu V$
  - ◆ Best Bipolar Op Amps:  $10-25\mu V$
  - ◆ Best FET Op Amps:  $50-1000\mu V$
  - ◆ High Speed Op Amps:  $100-2000\mu V$

Figure 1.29

Chopper stabilized op amps have a  $V_{OS}$  which is less than  $1\mu V$  (but, as mentioned above, are difficult to use because of noise). The best bipolar op amps (super-beta or bias stabilized) can have offsets as low as  $10\mu V$ , and the best FET types have about  $50\mu V$ . Generally, "precision" op amps will have  $V_{OS} < 0.5mV$ , although some high speed ones may be a little worse than this.

Input offset voltage is often measured by measuring the op amp's output offset voltage and dividing by the noise gain of the circuit (see Figure 1.30). This method will yield accurate results if the effects of input bias current on the total output offset voltage are negligible.

FET input op amps have low bias currents at room temperature, so this method works satisfactorily. In the case of significant bias currents where  $I_{b+}$  and  $I_{b-}$  are not equal (as in the case of current feedback op amps), an instrumentation amplifier connected to the op amp input terminals (through isolation resistors) should be used to provide the gain for the measurement (right-hand diagram in Figure 1.30). The offset voltage of the instrumentation amp (measured with S closed) must then be subtracted from the final measurement. Another circuit for measuring input offset voltage (independent of bias currents) is shown in Figure 1.36.

# MEASURING INPUT OFFSET VOLTAGE

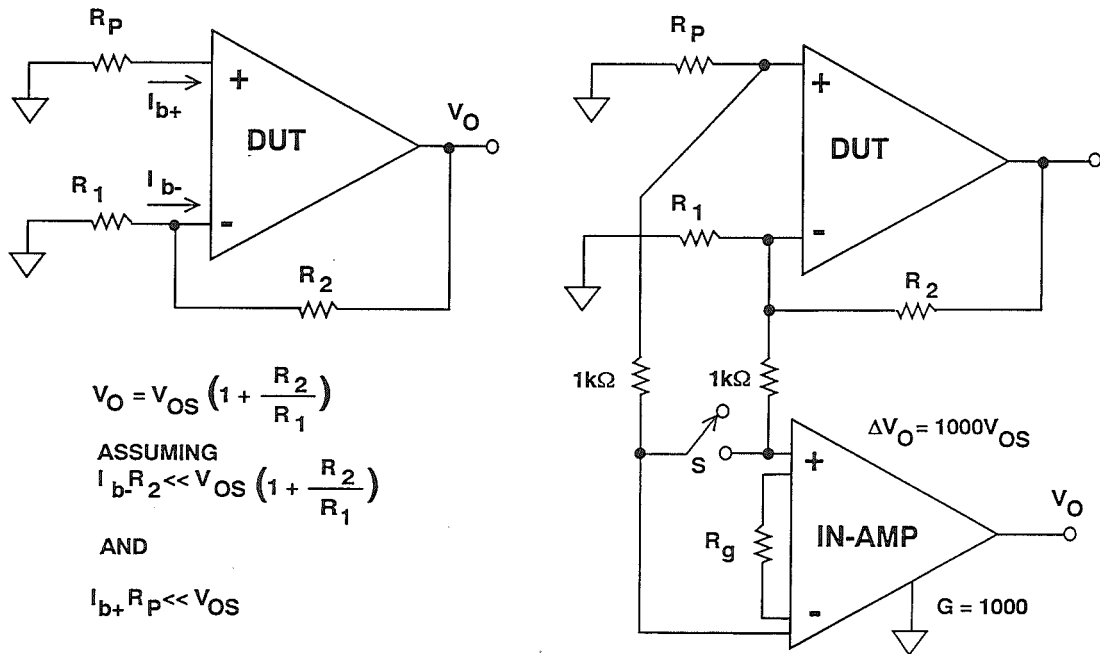


Figure 1.30

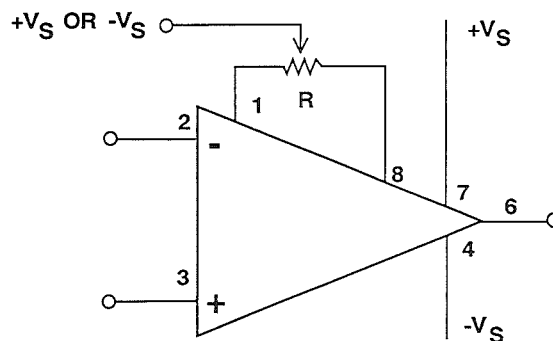
## Offset Adjustment

Many op amps have pins available for optional offset null. Generally, two pins are joined by a potentiometer, and the wiper goes to one of the supplies as shown in Figure 1.31. If the wiper is accidentally connected to the wrong supply, the op amp will probably be destroyed — this is a common problem when one type of op amp is replaced with another. The range of offset adjustment in a well-designed op amp is

no more than two or three times the maximum  $V_{OS}$  of the lowest grade device, in order to minimize the sensitivity of these pins. Nevertheless, the voltage gain of an op amp at its offset adjustment pins may actually be greater than the gain at its signal inputs! It is therefore very important to keep these pins free of noise. It is inadvisable to have long leads from an op amp to a remote potentiometer.



## OFFSET ADJUSTMENT PINS



- Wiper connection may be to either  $+V_S$  or  $-V_S$  depending on op amp
- R value depends on op amp,  $10\text{k}\Omega$  -  $100\text{k}\Omega$  typical
- Use to null out input offset voltage, not system offsets!
- There may be high gain from offset pins to output -- Keep them quiet!
- Nulling offset causes increase in offset temperature coefficient, approximately  $4\mu\text{V}/^\circ\text{C}$  for  $1\text{mV}$  offset null for FET inputs

Figure 1.31

As was mentioned above, the offset drift of an op amp with temperature will vary with the setting of its offset adjustment. The internal adjustment terminals should therefore be used only to adjust the op amp's own offset, not to correct any system offset errors, since this would be at the expense of increased temperature drift. The drift penalty for a FET input op amp is in the order of  $4\mu\text{V}/^\circ\text{C}$  for each millivolt of nulled offset voltage. It is generally better to control the offset voltage by proper selection of devices and device grades.

If an op amp does not have offset adjustment pins, and it is necessary to adjust the amplifier and system offsets, or if the offset adjustment is to be done with a DAC (which is not well-suited to interfacing with op amp offset adjustment pins), then offset correction may be performed in a number of ways.

Injecting current into the inverting input is the simplest method when using the op amp in the inverting mode (see Figure 1.32). The disadvantage of this method is that there is an increase in noise gain due to  $R_3$  and the potentiometer resistance. The resulting increase in noise gain may be reduced by making  $V_R$  large enough so that  $R_3$  can be made much greater than  $R_1$  and  $R_2$ .

The second circuit in Figure 1.32 shows how to create an output offset by injecting the offset current into the non-inverting input. This circuit results in no increase in noise gain, but requires the addition of  $R_p$ . If the op amp has matched input bias currents, then  $R_p$  should equal the parallel combination of  $R_1$  and  $R_2$  (for bias current cancellation). Otherwise,  $R_p$  should be less than  $50\Omega$ . It may be advisable to decouple  $R_p$  at HF.

## INVERTING OP AMP LEVEL SHIFTERS

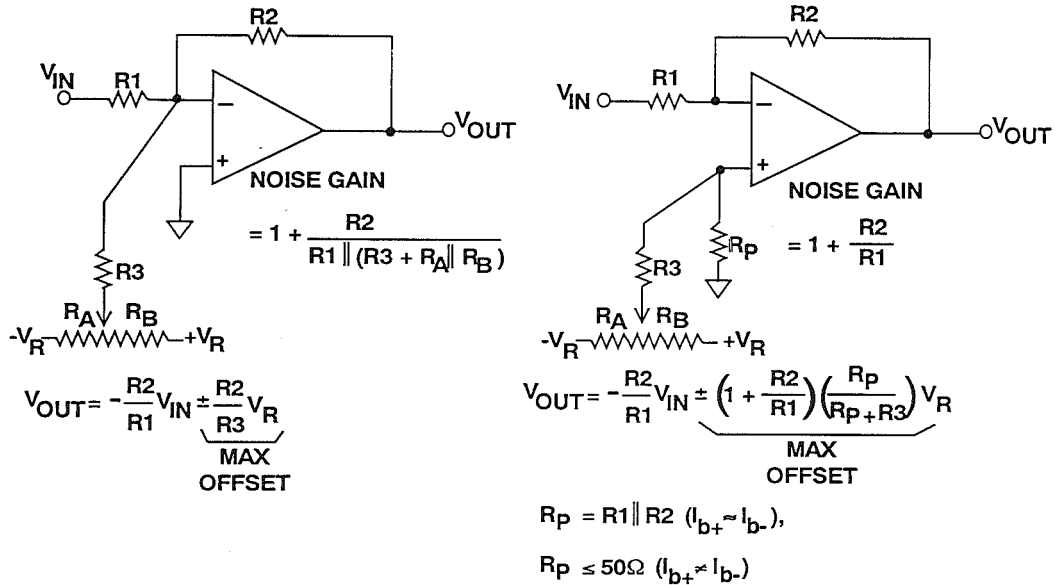


Figure 1.32

The circuit shown in Figure 1.33 can be used to level shift the output when using the op amp in the non-inverting mode. This circuit works well for small offsets where R3 can be made much greater than R1. Otherwise, the signal

gain will be affected as the offset potentiometer is adjusted. The gain may be stabilized, however, if R3 is connected to a fixed low impedance reference voltage source.

## NON-INVERTING OP AMP LEVEL SHIFTER

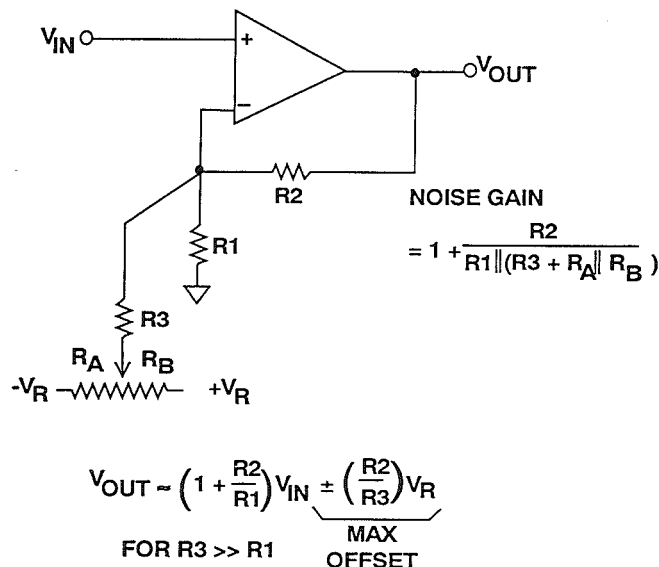


Figure 1.33

### Input Offset Voltage Drift and Aging Effects

$V_{OS}$  varies with temperature, and its temperature coefficient is known as  $TCV_{OS}$ . As we have mentioned, offset drift is affected by offset adjustments to the op amp, but when it has been minimized, it may be as low as  $30\text{nV}/^{\circ}\text{C}$  (typical value for OP-177E). More typical values for a range of general purpose precision op amps lie in the range  $1 - 10\mu\text{V}/^{\circ}\text{C}$ .

Most op amps have a specified value of  $TCV_{OS}$ , but some, instead, have a second value of maximum  $V_{OS}$  which is

guaranteed over the operating temperature range. Such a specification is less useful, because there is no guarantee that  $TCV_{OS}$  is constant or monotonic.

$V_{OS}$  changes as time passes. Aging is generally specified in  $\mu\text{V}/\text{month}$  or  $\mu\text{V}/1000\text{ hrs}$ , but this is misleading. Since aging is a "drunkard's walk" phenomenon it is proportional to the *square root* of the elapsed time. An aging rate of  $1\mu\text{V}/1000\text{ hr}$  becomes about  $3\mu\text{V}/\text{yr}$ , not  $9\mu\text{V}/\text{yr}$ .

## INPUT OFFSET VOLTAGE DRIFT ( $TCV_{OS}$ ) AND AGING

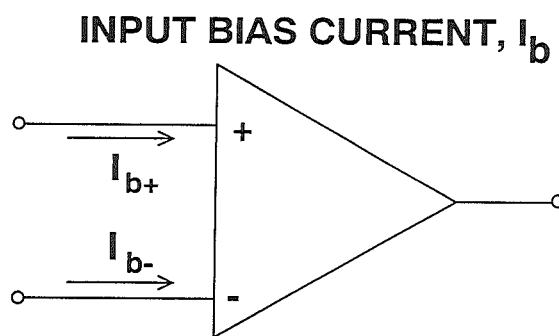
- Values may range from  $30\text{nV}/^{\circ}\text{C}$  (typical for OP-177E) to  $10\mu\text{V}/^{\circ}\text{C}$  or more
- Internal offset adjustments using null pins make drift worse
- Specification may be replaced by a specification of maximum  $V_{OS}$  over temperature -- this is less useful
- Aging in analog ICs is a "drunkard's walk" or "random walk" phenomenon, not linear. This means that the accumulated error is proportional to the *square root* of the elapsed time.
- $1\mu\text{V} / 1000\text{ hr} \approx 3\mu\text{V} / \text{year} \approx 9\mu\text{V} / 10\text{ year}$

Figure 1.34

## Input Bias Current, $I_b$

Ideally, no current flows into the input terminals of a voltage feedback op amp. In practice there is always a bias current,  $I_b$  (see Figure 1.35). Values of  $I_b$  range from 60fA (about one electron every three microseconds) in the AD549 electrometer to tens of microamperes in some high speed op amps. Op amps with simple input structures using BJT

or FET long-tailed pair have bias currents which flow in one direction. More complex input structures (bias-compensated and transimpedance op amps) may have bias currents which are the difference between two or more internal current sources and may flow in either direction.



- A very variable parameter
- $I_b$  can vary from 60 fA (1 electron every 3  $\mu$ s) to many  $\mu$ A depending on the device.
- Some structures have well-matched  $I_b$ , others do not.
- Some structures'  $I_b$  varies little with temperature, but FET op amp's  $I_b$  doubles with every 10°C rise in temperature.
- Some structures have  $I_b$  which may flow in either direction.

Figure 1.35

Bias current is a problem to the op amp user because it flows in impedances and produces voltages, which add to system errors. Consider a non-inverting unity gain buffer driven from a source impedance of 1M $\Omega$ . If  $I_b$  is 10nA, it will introduce an additional 10mV of error into the system. If the designer forgets  $I_b$  and uses capacitive coupling, the circuit will not work at all. If  $I_b$  is low enough, it may work for a while while the capacitor charges, giving even more

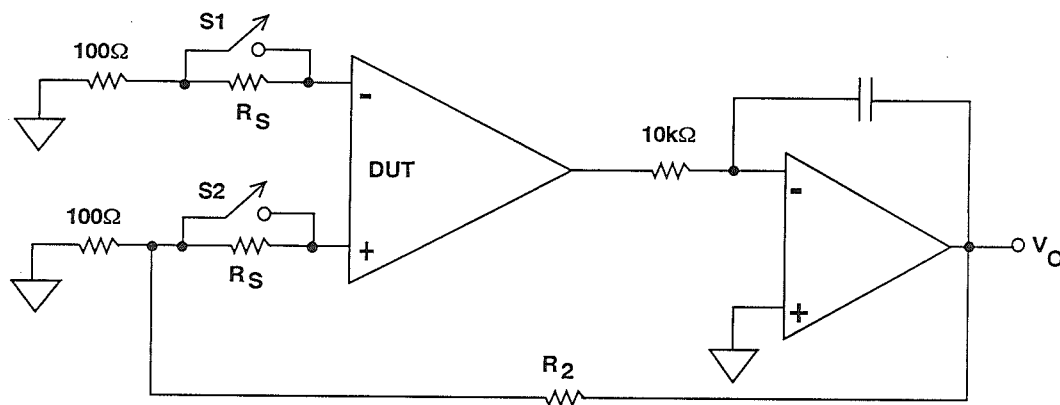
misleading results. If the capacitor is an electrolytic type, its leakage may be enough to pass the bias current - in some cases, so that we have a circuit which only works with *some* op amps and *some* capacitors.

Bias current (as well as input offset voltage) may be measured using the test circuit of Figure 1.36. A large resistance,  $R_s$ , is inserted in series with the input under test, creating an appar-

ent additional offset voltage equal to  $I_b R_S$ . If the actual  $V_{OS}$  has been measured and recorded, the change in apparent  $V_{OS}$  due to the change in  $R_S$  can be determined and  $I_b$  easily computed. The *offset current* may then be

calculated by taking the difference between the bias current on the inverting input and the bias current on the noninverting input. Typical  $R_S$  values vary from  $100\text{k}\Omega$  for bipolar op amps to  $1000\text{M}\Omega$  for some FET input devices.

## MEASURING INPUT BIAS CURRENT



$R_S \gg 100\Omega$  ( $100\text{k}\Omega$  TO  $1\text{G}\Omega$ )

S1 CLOSED TO TEST  $I_{b+}$

S2 CLOSED TO TEST  $I_{b-}$

BOTH CLOSED TO TEST  $V_{OS}$

BOTH OPEN TO TEST  $I_{OS}$

$$V_O = \left(1 + \frac{R_2}{100}\right) V_{OS} + \left(1 + \frac{R_2}{100}\right) I_{b+} R_S - \left(1 + \frac{R_2}{100}\right) I_{b-} R_S$$

Figure 1.36

Extremely low bias currents must be measured by integration techniques. The current is used to charge a capacitor, and the rate of change is measured. If the capacitor and general circuit leakage is negligible (this is very difficult to ensure when currents of under

$10\text{fA}$  are to be measured), the current may be calculated directly from the rate of change of the output of the test circuit (see Figure 1.37) when the switch which short-circuits the appropriate capacitor is opened.

## MEASURING LOW INPUT BIAS CURRENT

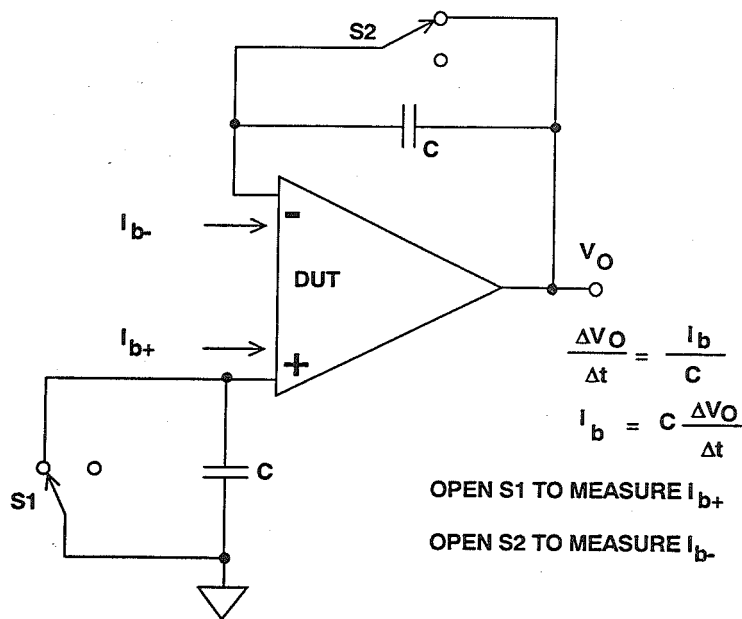


Figure 1.37

### Bias Current Cancellation (External to the Op Amp)

If the bias currents of an op amp are approximately equal (which is the case with simple bipolar op amps, but not bias compensated ones), then a bias compensation resistor,  $R_3$ , (where  $R_3 = R_1 \parallel R_2$ ) will introduce a voltage drop in the non-inverting input to compensate the drop in the parallel

combination of  $R_1$  and  $R_2$  in the inverting input (see Figure 1.38). If  $R_3$  is more than  $1\text{k}\Omega$  or so, it should be decoupled with a capacitor to prevent HF instability. This form of bias cancellation is useless where bias currents are not well-matched, and will, in fact, make matters worse unless they are.

## BIAS CURRENT CANCELLATION

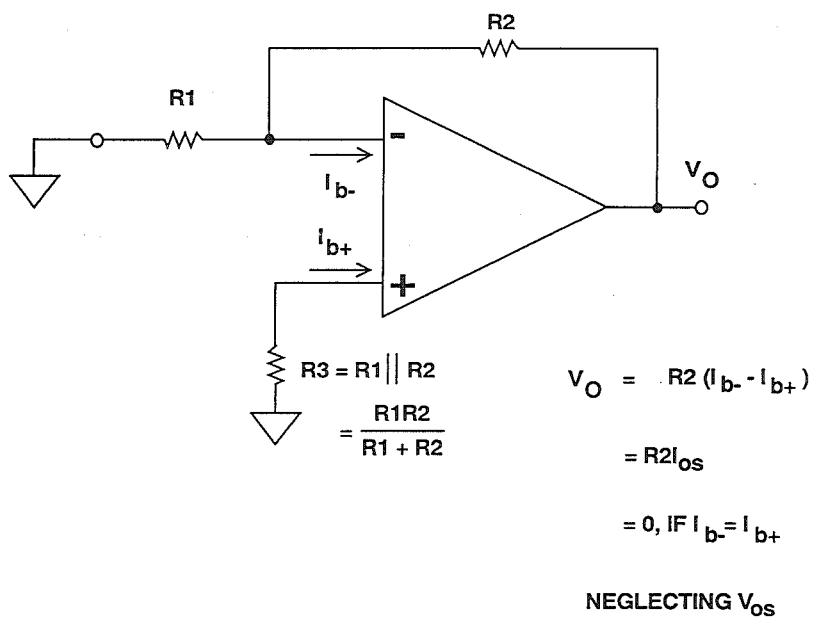


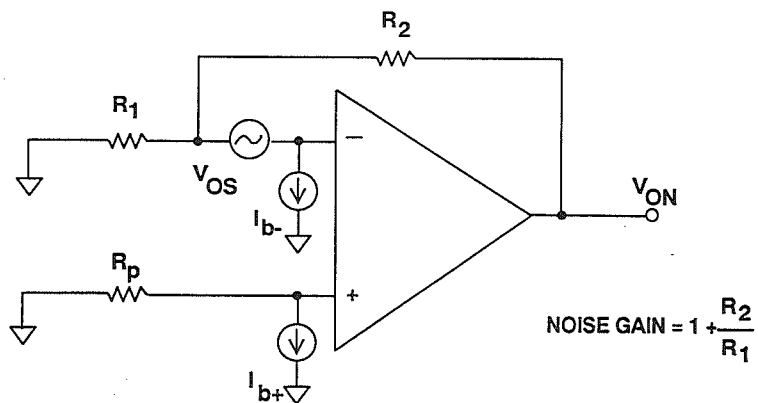
Figure 1.38

## Calculation of Total Output Offset Error Due to $I_b$ and $V_{os}$

The equations shown in Figure 1.39 are useful in reflecting all the offset and

bias current errors to the output of the op amp.

## MODEL FOR CALCULATING TOTAL OP AMP OUTPUT VOLTAGE OFFSET



$$V_O = \pm V_{OS} \left[ 1 + \frac{R_2}{R_1} \right] \pm I_{b+} R_p \left[ 1 + \frac{R_2}{R_1} \right] \pm I_{b-} R_2$$

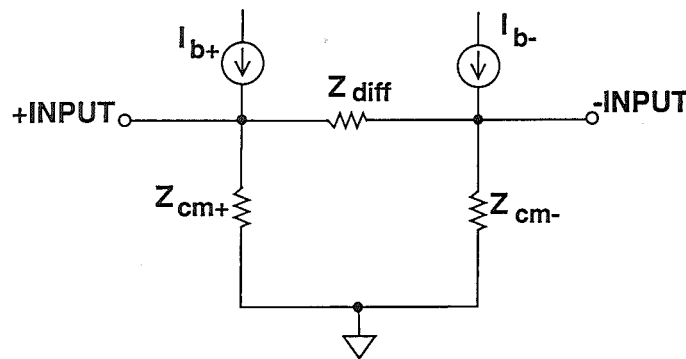
Figure 1.39

## Input Impedance

Voltage feedback operational amplifiers normally have both differential and common-mode input impedance specified. Transimpedance (current feedback) op amps normally specify the impedance to ground at each input. Different models may be used for differ-

ent voltage feedback op amps, but in the absence of other information, it is usually safe to use the model in Figure 1.40. In this model the bias currents flow into the inputs from perfect (infinite impedance) current sources.

### INPUT IMPEDANCE (VOLTAGE FEEDBACK)



- $Z_{cm+}$  and  $Z_{cm-}$  are the common-mode input impedance. The figure on the data sheet is for one, not both, but they are approximately equal.  $Z_{diff}$  is the differential input impedance.
- They are high resistance ( $10^5 - 10^{12}\Omega$ ) in parallel with a small shunt capacitance (sometimes as high as 25pF).
- In most practical circuits,  $Z_{cm-}$  is swamped by negative feedback.

Figure 1.40

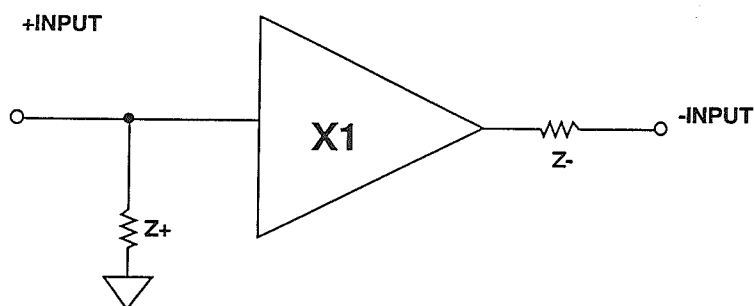
The common-mode input impedance specified on the data sheet ( $Z_{cm+}$  and  $Z_{cm-}$  in the diagram) is the impedance from either input to ground (NOT from both to ground). The differential input impedance ( $Z_{diff}$ ) is the impedance between the two inputs. They are usually resistive and high ( $10^5 - 10^{12}\Omega$ ) with some shunt capacitance (generally a few pF, sometimes as much as 20-25 pF). In most practical op amp circuits, the impedance at the inverting

input is reduced to a very low value by negative feedback and only  $Z_{cm+}$  and  $Z_{diff}$  are of any importance.

The model for a transimpedance (current feedback) op amp is even simpler and is shown in Figure 1.41.  $Z_+$  is resistive, generally with some shunt capacitance, and high ( $10^5 - 10^9\Omega$ ) while  $Z_-$  is reactive (L or C, depending on the device) but has a resistive component of 10 - 100 $\Omega$ , varying from type to type.



## INPUT IMPEDANCE (CURRENT FEEDBACK)



- $Z_+$  is high resistance ( $10^5 - 10^9 \Omega$ ) with little shunt capacitance.
- $Z_-$  is low and may be reactive (L or C) The resistive component is  $10 - 100 \Omega$

Figure 1.41

## Open-Loop Gain

The open-loop voltage gain of most voltage feedback op amps is high. Values of 50,000 to 100,000,000 are common. Some fast op amps have lower open-loop gain, but gains of less than a few thousand are usually unsatisfactory for high accuracy applications. The open loop gain is not stable with temperature and can vary quite widely from device to device of the same type, so it is important that it be reasonably high.

Since a voltage feedback op amp has voltage in and voltage out, its open loop gain is a ratio and dimensionless, and no unit is therefore necessary. However,

data sheets sometimes express gain in V/mV instead of V/V for the convenience of using smaller numbers.

Current feedback op amps have a current input and a voltage output, so the open loop *transimpedance gain* is expressed in volts per ampere or ohms (or  $k\Omega$  or  $M\Omega$ ). Values usually lie between hundreds of  $k\Omega$  and tens of  $M\Omega$ .

In many signal processing applications, AC specifications such as bandwidth, settling time, and distortion are more important than open-loop gain.

## OPEN-LOOP GAIN

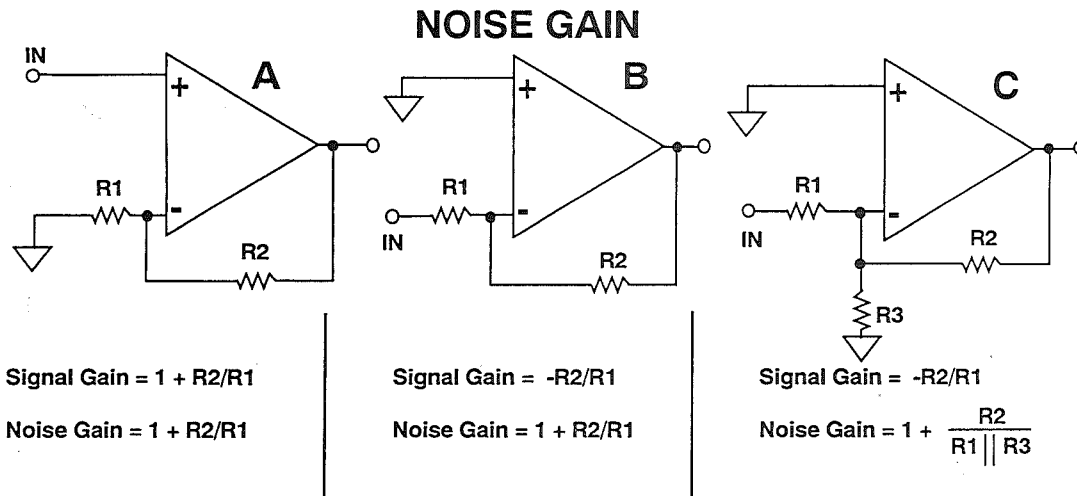
- Voltage Feedback Op Amps:
  - ◆ Volts Out / Volts In (Dimensionless)
  - ◆ Generally in the Range of 50,000 to 100,000,000 (94 to 160dB)
  - ◆ Sometimes Divided by 1,000 and expressed as Volts/millivolt.
- Transimpedance (Current Feedback) Op Amps:
  - ◆ Volts Out / Current In (Resistance)
  - ◆ Generally in the Range of 200k $\Omega$  to 50M $\Omega$

Figure 1.42

## Noise Gain

Consider an op amp and two resistors, R1 and R2, arranged as shown in Figure 1.43 (they need not be resistors, they could be complex impedances Z1 and Z2). If we ground R1 and apply a signal to the non-inverting input, we see a signal gain of  $1 + R2/R1$  (left-hand diagram, Figure 1.43). If we ground the

non-inverting input and apply the signal to R1, we see a signal gain of  $-R2/R1$  (center diagram, Figure 1.43). In both cases, the voltage noise of the op amp itself (as well as the input offset voltage) sees a gain of  $1 + R2/R1$ , which is known as the *noise gain* of the op amp.



- Voltage Noise and Offset Voltage of the op amp are reflected to the output by the Noise Gain.
- Noise Gain, not Signal Gain, is relevant in assessing stability.
- Circuit C has unchanged Signal Gain, but higher Noise Gain, thus better stability, worse noise, and higher output offset voltage.

Figure 1.43

The noise gain and the signal gain need not be equal, but it is the noise gain which is relevant in assessing stability. It is sometimes possible to alter the noise gain while leaving signal gain unaffected. Consider the inverting amplifier above: if we add a third resistor,  $R3$ , from the inverting input to

ground, the signal gain is unaffected, but the noise gain is increased to  $1 + R2/(R1 || R3)$  (right-hand diagram, Figure 1.43). This provides a means of stabilizing an unstable inverting amplifier - at the cost of worse signal-to-noise ratio, less loop gain, and increased sensitivity to input offset voltage.

## Closed-Loop Gain

Operational amplifiers are generally used in closed-loop applications where gain is determined by negative feedback. In the discussion of noise gain above, we assumed that the open loop gain was infinite, and the closed-loop gain was determined only by the resistor ratios. This is not actually the case.

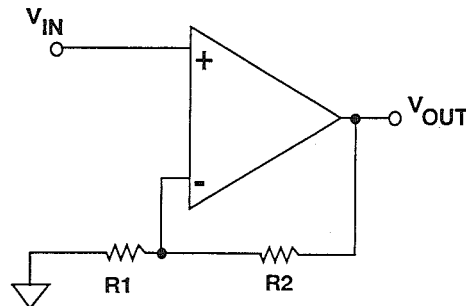
The expression for the gain of a closed-loop amplifier involves the open-loop gain. If  $G$  is the actual gain,  $N_G$  is the noise gain defined by the resistors  $R_1$  and  $R_2$ , and  $A$  is the open-loop gain of the amplifier, then

$$G = N_G - \frac{N_G^2}{N_G + A} = \frac{N_G}{\frac{N_G}{A} + 1}$$

Although this equation may be used to calculate low-frequency gain errors, it may also be used at higher frequencies, with  $R_1$  and  $R_2$  replaced by complex impedances  $Z_1$  and  $Z_2$ , and  $A$  by  $A(s)$  (the gain at the frequency of interest) to determine actual HF gain.

The same equation is applicable to both voltage feedback and current feedback op amps. In the case of a current feedback op amp, however,  $A$  is obtained by dividing the open loop transimpedance gain  $T_z$  by the inverting input impedance  $R_s$ , i.e.,  $A = T_z/R_s$ .

### CLOSED-LOOP GAIN IS AFFECTED BY FINITE OPEN-LOOP GAIN



$$N_G = 1 + \frac{R_2}{R_1}$$

$$\frac{V_{OUT}}{V_{IN}} = G = N_G - \frac{N_G^2}{N_G + A} = \frac{N_G}{\frac{N_G}{A} + 1}$$

■  $A$  = Open Loop Gain

■ For Current Feedback,  $A = T/R_s$ , where  
 $T$  = Open-Loop Transimpedance Gain  
 $R_s$  = Inverting Input Resistance

Figure 1.44

## Op Amp Frequency Response - Introduction

There are a number of issues to consider when discussing the frequency response of op amps. Some are relevant to both voltage- and current feedback types, some apply to one or the other, but not to both. Issues which vary with type are usually related to small-signal performance, while large-signal issues mostly apply to both.

A good working definition of "large-signal" is where the frequency limit is set by the slew rate measured at the output stage, rather than the pole(s) of the small signal response. We shall therefore consider large signal parameters applying to both types of op amp before we consider those parameters where they differ.

### OP AMP FREQUENCY RESPONSE

- Small-signal frequency response issues differ between voltage feedback and current feedback op amps
- Large signal issues are generally common to both
- The difference between small-signal and large-signal is that *slew rate* limits large-signal frequency response
- In general, the faster an op amp the more supply current it draws, and the more output current it may need to source

Figure 1.45

## Frequency Response - Slew Rate and Full-Power Bandwidth

The slew rate of an amplifier is the maximum rate of change of voltage at its output. It is expressed in V/s (or, more probably, V/ $\mu$ s). We have mentioned earlier why op amps might have different slew rates during positive- and negative going transitions, but for this analysis we shall assume that good fast op amps have reasonably symmetrical slew rates.

If we consider a sine wave with a pk-pk amplitude of  $2V_p$  and frequency  $f$ , the expression for the output voltage is:

$$v(t) = V_p \sin 2\pi f t \quad [1]$$

This has a maximum slew rate:

$$\left. \frac{dv}{dt} \right|_{\max} = 2\pi f V_p \quad [2]$$

We can thus see that the maximum frequency at which slew limiting *does not occur* is directly proportional to slew rate and inversely proportional to the amplitude of the signal. This allows us to define the "full-power bandwidth" (FPBW) of an op amp as the maximum frequency at which slew limiting does not occur at maximum output. This may be calculated by letting  $2V_p$  in equation [2] equal the maximum pk-pk swing of the amplifier,  $dV/dt$  equal the slew rate, and solving for  $f$ :

$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p \quad [3]$$

It is important to realize that both slew rate and full-power bandwidth can also depend somewhat on the power supply voltage being used and the load the amplifier is driving (particularly capacitive).

### SLEW RATE AND FULL-POWER BANDWIDTH

■ Slew Rate = Maximum rate at which the output voltage of an op amp can change

■ Ranges: A few volts/ $\mu$ s to several thousand volts/ $\mu$ s

■ For a sinewave,  $V_{\text{out}} = V_p \sin 2\pi f t$

$$dV/dt = 2\pi f V_p \cos 2\pi f t$$

$$(dV/dt)_{\max} = 2\pi f V_p$$

■ If  $V_p$  = full output span of op amp, then

$$\text{Slew Rate} = (dV/dt)_{\max} = 2\pi \cdot \text{FPBW} \cdot V_p$$

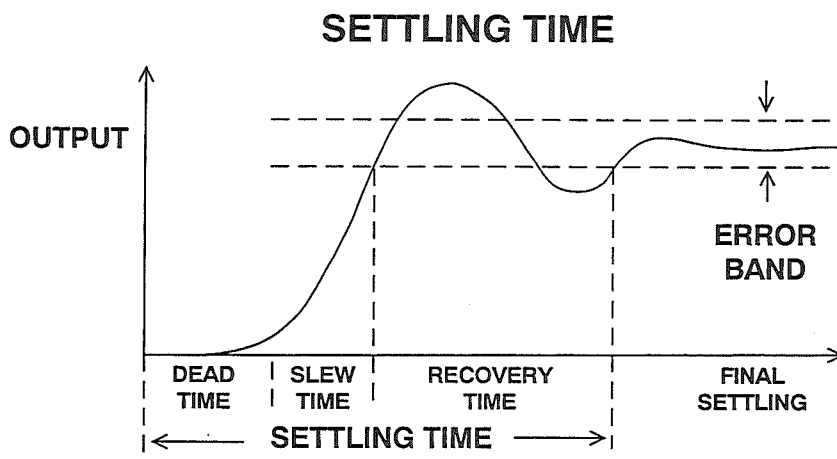
$$\text{FPBW} = \text{Slew Rate} / 2\pi V_p$$

Figure 1.46

## Frequency Response - Settling Time

The settling time of an amplifier is defined as the time it takes the output to respond to a step change of input and come within *and remain within* a defined error band, as measured relative to the 50% point of the input pulse (see Figure 1.47). There is no natural error band for an op amp (a DAC naturally has an error band of 1 LSB, or perhaps  $\pm 1\text{LSB}$ ), so one must be chosen and defined. What is chosen will depend on the performance of the op amp, but since the value chosen will vary from

device to device, comparisons are very difficult. This is true because settling is not linear, and many different time constants may be involved. Examples are early op amps using dielectrically isolated (DI) processes. These had very fast settling to 1% of full-scale, but they took almost forever to settle to 10-bits (0.1 %). Similarly, some very high precision op amps have thermal effects which cause settling to 0.001% or better to take tens of ms, although they will settle to 0.025% in a few  $\mu\text{s}$ .



- Error band is usually defined to be a percentage of the step 0.1%, 0.05%, 0.01%, etc.
- Settling time is non-linear; it may take 30 times as long to settle to 0.01% as to 0.1%.
- Manufacturers often choose an error band which makes the op amp look good.

Figure 1.47

Measuring fast settling time to high accuracy is difficult. Great care is required in order to generate fast, highly accurate, low noise, flat top pulses. Step voltages will overdrive most oscilloscope front ends when the input is set for high sensitivity. The test setup shown in Figure 1.48 is useful in making settling time measurements on op amps operating in the inverting

mode. The signal at the "false summing junction" represents the difference between the output and the input multiplied by the constant  $k$ , i.e. the ERROR signal. Schottky diode clamps help prevent scope overdrive and allows the use of high sensitivity. If  $R_1=R_2$ , then  $k=0.5$ . The error band at the ERROR output will be 5mV for 0.1% settling with a 10V input step.

## MEASURING SETTLING TIME USING A "FALSE SUMMING NODE"

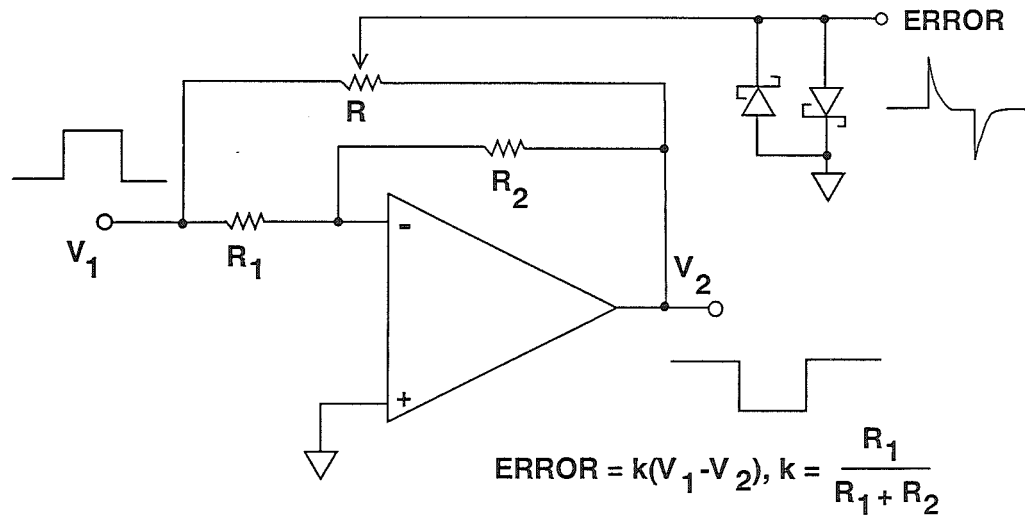


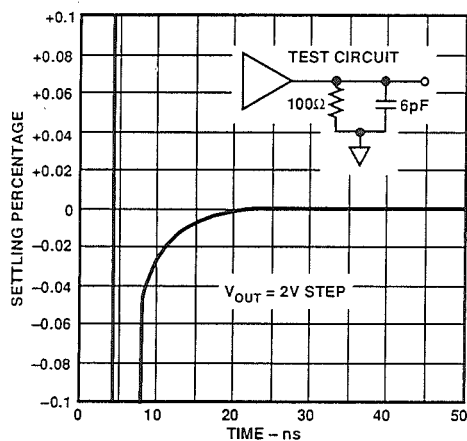
Figure 1.48

Certain digitizing scopes (such as the Data Precision Model 640 plug-in) can be used to measure the output waveform directly without overdrive. This allows measurements of settling time in both the inverting and non-inverting

modes. An example of the output step response to a flat pulse input for the AD9622 op amp is shown in Figure 1.49. Photos are shown for both short and long-term settling times.

## MEASURING SETTLING TIME DIRECTLY USING A DIGITIZING PLUG-IN

### SHORT TERM



### LONG TERM

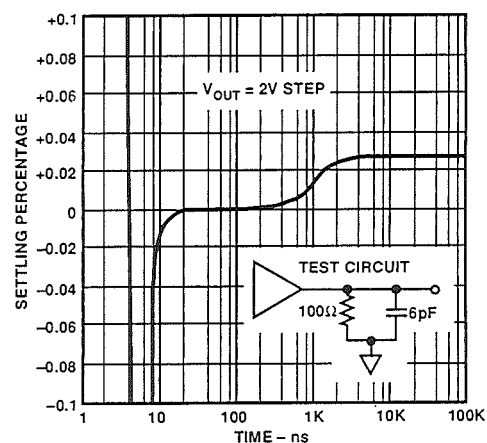


Figure 1.49



## Frequency Response - Capacitive Loads

When an op amp drives a capacitive load, its output stage is slowed down. This puts an additional pole in the frequency response and, since op amps take negative feedback from their output stage, may cause instability and oscillation. (An example of the way that capacitive loads often cause oscillations is shown by the way that so many voltage references oscillate when loaded with large capacitors. The buffer amplifiers in voltage references could be made stable under capacitive load, but too often they are not.)

Figure 1.50 shows two methods for stabilizing an op amp driving a capaci-

tive load. In each case a series resistor is used for compensation. The resistor is placed outside the feedback loop in the first method (this is commonly referred to as open-loop compensation). This introduces a gain error at the output load because of the resulting attenuator formed by  $R_L$  and  $R_S$ . The resistor is placed inside the feedback loop in the second method (in-loop or closed-loop compensation). DC feedback is taken from the load, but AC feedback from the op amp output. This introduces AC gain errors, but is simple and eliminates DC gain error. Both methods result in loss of total bandwidth.

### DRIVING CAPACITIVE LOADS

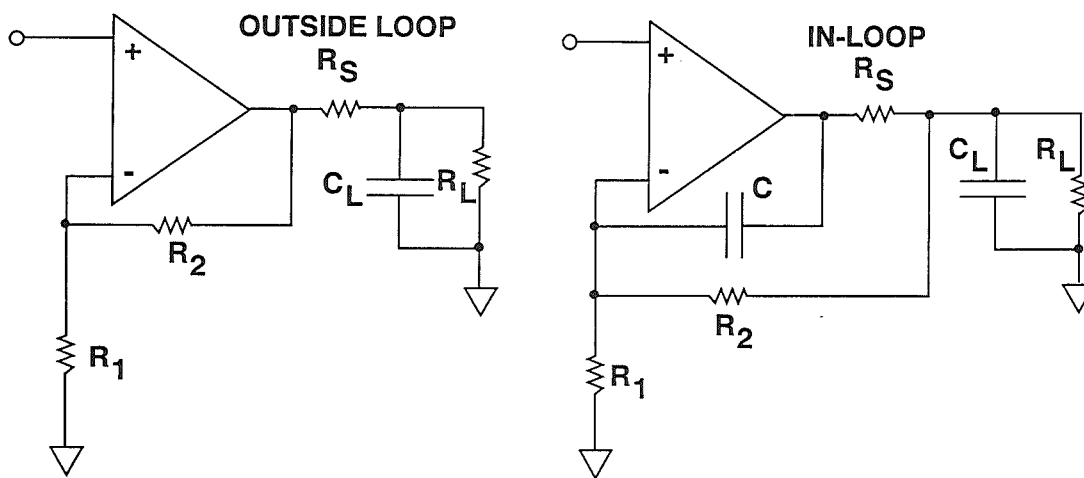
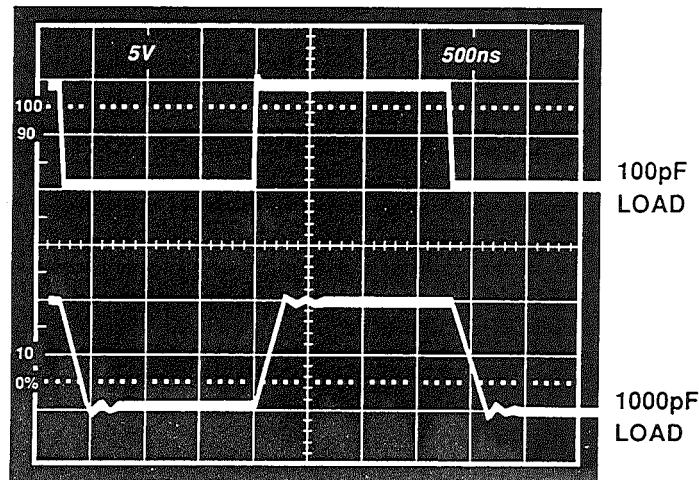


Figure 1.50

Another solution is to design an op amp whose load capacity contributes to the dominant pole of its overall response - as the load capacity increases the device slows down but remains stable. The AD817/AD847 family of op

amps uses this principle (see Reference 7). Pulse response for two capacitive loads is shown in Figure 1.51. Note that increasing the load capacitance from 100pF to 1000pF reduces the bandwidth proportionally.

### LOAD CAPACITANCE CONTRIBUTES TO DOMINANT POLE IN AD847 OP AMP



VERTICAL SCALE: 5V/div.  
HORIZONTAL SCALE: 500ns/div.

Figure 1.51

## Frequency Response - Voltage Feedback Op amps - Gain-Bandwidth Products

The open-loop frequency response of a voltage feedback op amp is shown in Figure 1.52. There are two possibilities: the left-hand diagram shows the most common, where a high DC gain drops at 6 dB/octave from quite a low frequency down to unity gain. This is a single pole response. The amplifier in the right-hand diagram has two poles in its

response - the gain drops at 6 dB/octave for a while and then drops at 12 dB/octave. The amplifier in the left-hand diagram is known as an *unconditionally stable* or *fully compensated* type and may be used with a noise gain of unity. They are stable with 100% feedback (including capacitance) from output to inverting input.

### FREQUENCY RESPONSE OF VOLTAGE FEEDBACK OP AMPS

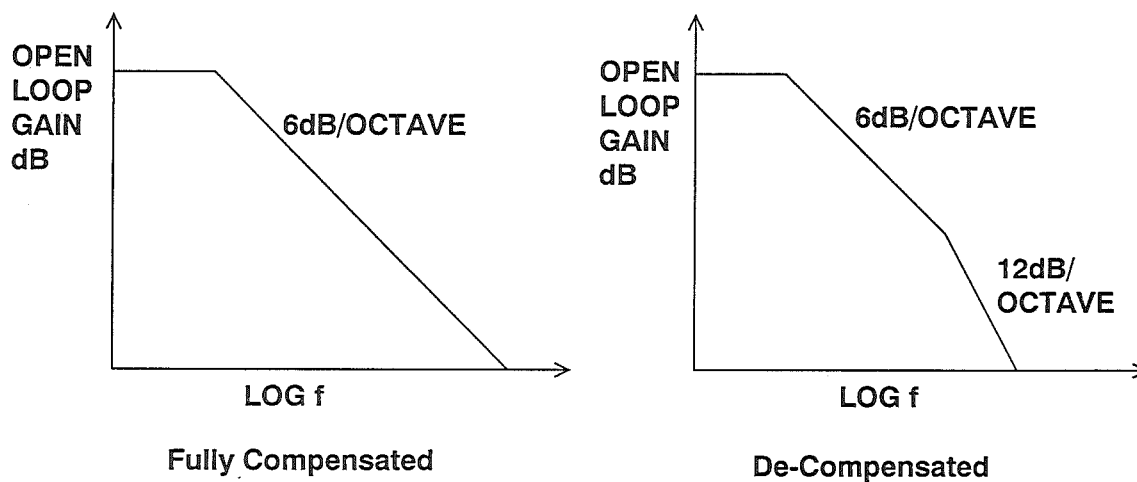


Figure 1.52

If the amplifier in the right-hand diagram is used with a noise gain which is lower than the gain at which the slope of the response increases from 6 to 12dB/octave, the phase shift in the feedback will be too great, and it will oscillate. Amplifiers of this type are characterized as “stable at gains  $\geq X$ ” where  $X$  is the gain at the frequency where the 6dB/12dB transition occurs. It is, of course, the noise gain which is

referred to, and it will generally be between 2 and 25. These *decompensated* op amps have higher gain-bandwidth products than fully compensated amplifiers, all other things being equal, and so are useful despite the slightly greater complication of designing with them. They can never be used with direct capacitive feedback from output to inverting input.

The 6dB/octave slope of the response of both types means that over the range of frequencies where it occurs, the product of the closed-loop gain and the 3dB closed-loop bandwidth at that gain is a constant - this is known as the *gain-bandwidth product* (GBW) and is a figure of merit for an amplifier. If an op amp has a GBW product of X MHz,

then its closed loop bandwidth at a noise gain of 1 will be X MHz, at a noise gain of 2 it will be X/2 MHz, and at a noise gain of Y it will be X/Y MHz (see Figure 1.53). Notice that the *closed-loop* bandwidth is the frequency at which the noise gain intersects the open-loop gain.

### GAIN-BANDWIDTH PRODUCT FOR VOLTAGE FEEDBACK OP AMPS

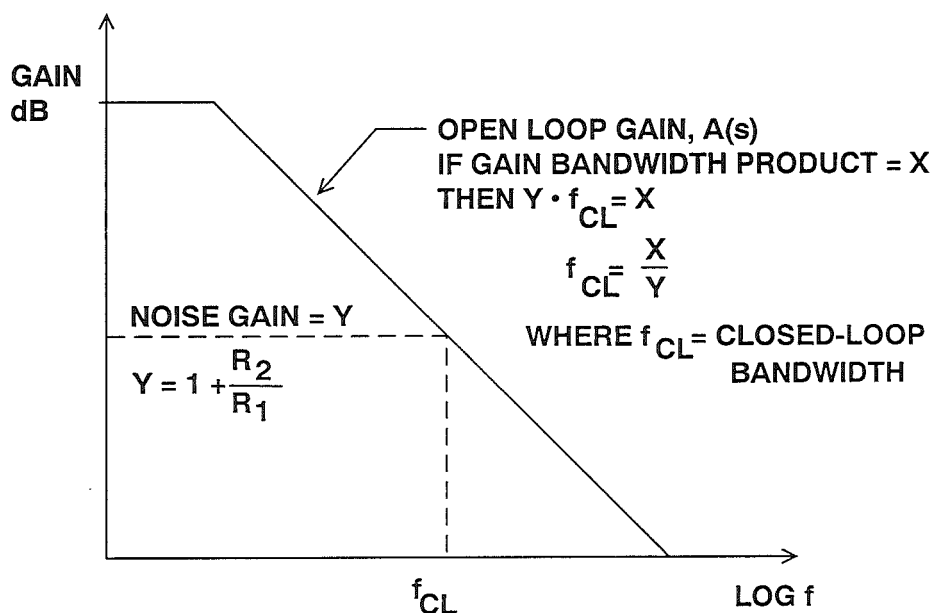


Figure 1.53

In the above example, we assumed that the feedback elements were resistive. This is not usually the case, especially when the op amp requires a feedback capacitor for stability. Figure 1.54 shows a typical example where there is capacitance, C1, on the inverting input of the op amp. The capacitance is the sum of the op amp internal capacitance and any external capacitance which may exist. This capacitance introduces a pole in the noise gain transfer function. Stability of the system is deter-

mined by the net slope of the noise gain and the open-loop gain where they intersect. For unconditional stability, the noise gain must intersect the open-loop gain with a net slope of less than 12dB/octave (20dB per decade). Adding the feedback capacitor, C2, introduces a zero in the noise gain transfer function which stabilizes the circuit. Notice that the closed-loop bandwidth,  $f_{CL}$ , is determined by the frequency at which the noise gain intersects the open-loop gain.

## BODE PLOT SHOWING NOISE GAIN FOR VOLTAGE FEEDBACK OP AMP WITH REACTIVE ELEMENTS

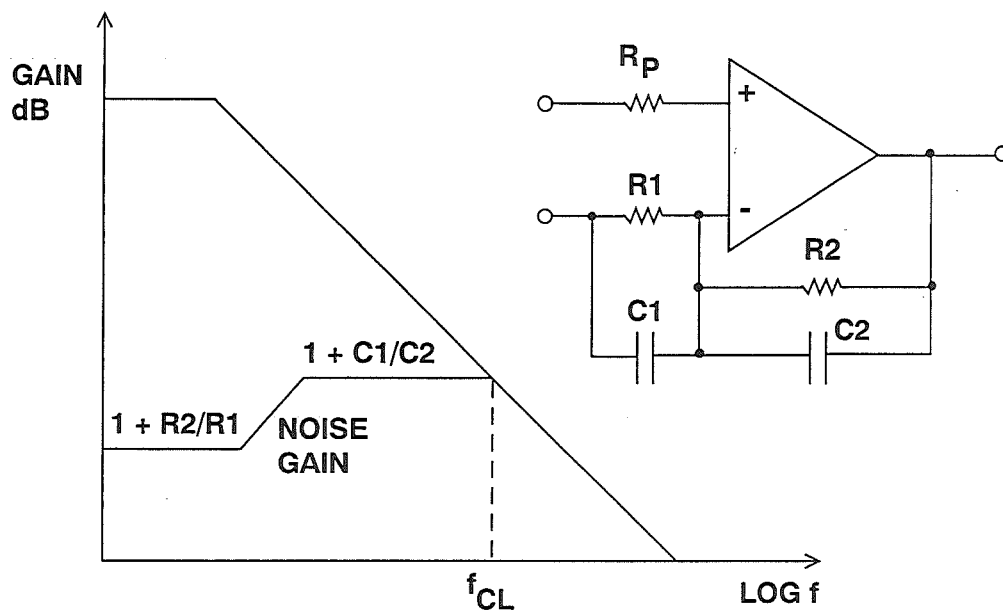


Figure 1.54

The Bode Plot of the noise gain is a very useful tool in analyzing op amp stability. Constructing the Bode plot is a relatively simple matter. Although it is

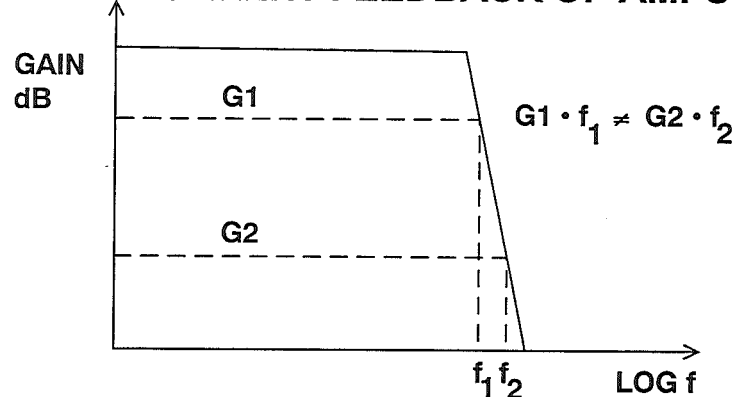
outside the scope of this section to carry the discussion of noise gain and stability further, the reader is referred to Reference 5.

## Frequency Response - Current Feedback Op amps

Current feedback op amps do not behave in the same way as voltage feedback types. They are rarely stable with capacitive feedback, or with a short circuit from output to inverting input. There is generally an optimum feedback resistance for maximum bandwidth (the value of this resistance may vary with supply voltage - consult individual device data sheets). If the feedback resistance is increased, the bandwidth is reduced. If it is reduced, the bandwidth increases, and the amplifier may become unstable.

But for a given value of feedback resistance ( $R_2$ ), the bandwidth is largely unaffected by the noise gain. It is therefore incorrect to refer to the gain-bandwidth product of a current feedback amplifier. If  $R_1$  is too large, its shunt capacitance affects gain, and if it is too small (comparable to the actual input resistance of the amplifier on its inverting input), the interaction of the two is troublesome.

## FREQUENCY RESPONSE FOR CURRENT FEEDBACK OP AMPS



- Feedback resistor fixed for optimum performance.  
Larger values reduce bandwidth, smaller values may cause instability.
- For fixed feedback resistor, changing gain has little effect on bandwidth.
- Current feedback op amps do not have a fixed gain-bandwidth product.

Figure 1.55

When used in the inverting mode, with the non-inverting input grounded, noise gains of little more than unity (signal gains  $\ll 1$ ) are possible with current feedback amplifiers. In the non-inverting mode, however, the minimum value of the resistor from the output to the inverting input reacts with stray capacitance on the inverting input to attenuate feedback at HF and produce gain peaking. General purpose current feedback amplifiers generally do

not have very flat frequency response when used in the non-inverting mode at low gains unless specifically designed for this application. The AD811 video op amp was optimized for bandwidth flatness (0.1dB from DC to 30MHz) for a gain of two and a resistive termination of 150Ω (75Ω source and load-terminated cable). However, a few pF of stray capacitance on the output will cause gain peaking even with this amplifier.

## FREQUENCY RESPONSE FOR CURRENT FEEDBACK OP AMPS

- Stray capacitance (either on inverting input or output or both) may cause gain peaking especially at low gains in non-inverting mode with minimum value of feedback resistor
- Bandwidth is relatively independent of gain for fixed feedback resistor
- High gains in inverting mode may be impractical because of low value feedforward resistor
- Current feedback op amps may be optimized for flat frequency response at low gains with no capacitive loading (AD811)

Figure 1.56

## Operational Amplifier Noise

This section discusses the noise generated within op amps, not external noise which they may pick up. External noise is important, and is discussed in detail in References 6 and 7, but in this section we are concerned solely with internal noise.

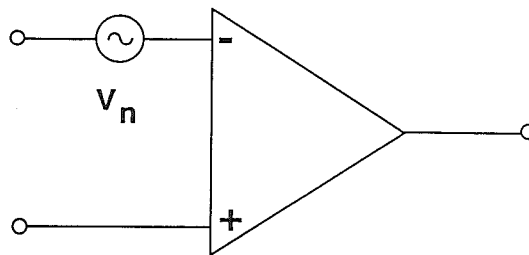
There are three noise sources in an op amp: a voltage noise which appears differentially across the two inputs, and a current noise in each input. These are effectively uncorrelated (independent of each other). In fact, there is a slight correlation between the two noise

currents, but it is too small to need consideration in practical noise analyses. In addition to these three internal noise sources, it is necessary to consider the Johnson noise of the external resistors which are used with the op amp.

All resistors have a Johnson noise of

$\sqrt{4kTBR}$ , where  $k$  is Boltzmann's Constant ( $1.38 \times 10^{-23} \text{ J/K}$ ),  $T$  is the absolute temperature,  $B$  is the bandwidth and  $R$  is the resistance. This is intrinsic - it is not possible to obtain resistors which do not have Johnson noise.

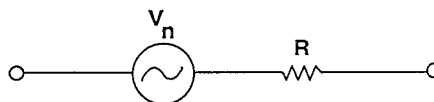
## INPUT VOLTAGE NOISE



- Input Voltage Noise is bandwidth dependent and measured in  $\text{nV}/\sqrt{\text{Hz}}$  (spectral density)
- Normal Ranges are  $1\text{nV}/\sqrt{\text{Hz}}$  to  $20\text{nV}/\sqrt{\text{Hz}}$

Figure 1.57

## JOHNSON NOISE OF RESISTORS



- ALL resistors have a voltage noise of  $\sqrt{4kTBR}$
- $T$  = Absolute Temperature =  $T(^{\circ}\text{C}) + 273.15$
- $B$  = Bandwidth (Hz)
- $k$  = Boltzmann's Constant ( $1.38 \times 10^{-23} \text{J/K}$ )
- A  $1000\Omega$  resistor generates  $4\text{nV}/\sqrt{\text{Hz}}$  @  $25^{\circ}\text{C}$

Figure 1.58



Uncorrelated noise voltages add in a "root sum of squares" manner; i.e., noise voltages  $V_1$ ,  $V_2$ ,  $V_3$  give a result of

$$\sqrt{V_1^2 + V_2^2 + V_3^2}.$$

Noise powers, of course, add normally. Thus, any noise voltage which is more than 4 or 5 times any of the others is dominant, and the others may generally be ignored. This simplifies noise assessment.

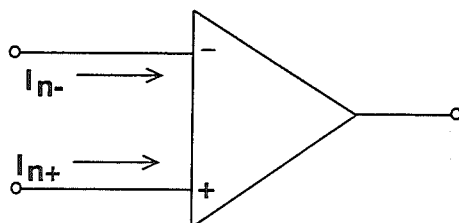
The voltage noise of different op amps may vary from under 1 nV/√Hz to 20 nV/√Hz, or even more. Bipolar op amps tend to have lower voltage noise than JFET ones, although it is possible to make JFET op amps with low voltage noise (such as the AD743/AD745), at the cost of large input devices and hence large (~20 pF) input capacitance. Voltage noise is normally specified on the

data sheet, and it is not possible to predict it from other parameters.

Current noise can vary much more widely, from around 0.1 fA/√Hz (in JFET electrometer op amps) to several pA/√Hz (in high speed bipolar op amps). It is not always specified on data sheets, but may be calculated in cases (like simple BJT or JFET input devices) where all the bias current flows in the input junction, because in these cases it is simply the Schottky (or shot) noise of the bias current. It cannot be calculated for bias-compensated or current feedback op amps, where the external bias current is the *difference* of two internal current sources. The shot noise spectral

density is simply  $\sqrt{2I_b q}$  amps/√Hz, where  $I_b$  is the bias current (in amps) and  $q$  is the charge on an electron ( $1.6 \times 10^{-19}$  C).

### INPUT CURRENT NOISE



- Normal Ranges: 0.1fA/√Hz to 10pA/√Hz
- In Voltage Feedback op amps the current noise in the inverting and non-inverting inputs is uncorrelated (effectively) but roughly equal in magnitude.
- In simple BJT and JFET input stages, the current noise is the shot noise of the bias current and may be calculated from the bias current.
- In bias-compensated input stages and in current feedback op amps, the current noise cannot be calculated.
- The current noise in the two inputs of a current feedback op amp may be quite different. It may not even have the same 1/f corner.

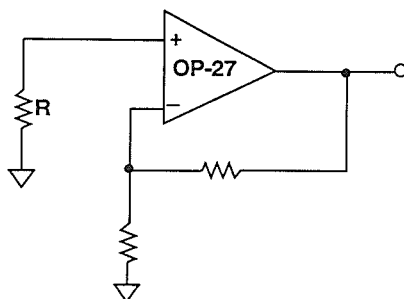
Figure 1.59

Current noise is only important when it flows in an impedance and generates a noise voltage. Therefore, the choice of a low noise op amp depends on the impedances around it. Consider an OP-27, a bias compensated op amp with low voltage noise ( $3\text{nV}/\sqrt{\text{Hz}}$ ), but quite high current noise ( $1\text{pA}/\sqrt{\text{Hz}}$ ). With zero source impedance, the voltage noise will dominate as shown in Figure 1.60. With a source resistance of  $3\text{k}\Omega$ , the current noise ( $1\text{pA}/\sqrt{\text{Hz}}$  flowing in  $3\text{k}\Omega$ ) will

equal the voltage noise, but the Johnson noise of the  $3\text{k}\Omega$  resistor is  $7\text{nV}/\sqrt{\text{Hz}}$  and so is dominant. With a source resistance of  $300\text{k}\Omega$ , the current noise increases a hundredfold to  $300\text{nV}/\sqrt{\text{Hz}}$ , while the voltage noise continues unchanged, and the Johnson noise (which is proportional to the *square root* of the resistance) only increases tenfold. Here, current noise is dominant.

## EFFECT OF SOURCE RESISTANCE ON TOTAL NOISE REFERRED TO INPUT

Example: OP-27  
Voltage Noise =  $3\text{nV}/\sqrt{\text{Hz}}$   
Current Noise =  $1\text{pA}/\sqrt{\text{Hz}}$   
( $T = 25^\circ\text{C}$ )



CONTRIBUTION FROM	VALUES OF R		
	0	$3\text{k}\Omega$	$300\text{k}\Omega$
AMPLIFIER VOLTAGE NOISE	3	3	3
AMPLIFIER CURRENT NOISE FLOWING IN R	0	3	300
JOHNSON NOISE OF R	0	7	70

RTI NOISE ( $\text{nV}/\sqrt{\text{Hz}}$ )  
Dominant Noise is Highlighted

Figure 1.60

The above example shows that the choice of a low noise op amp depends on the source impedance of the signal, and at high impedances, current noise always dominates.

For low impedance circuitry, amplifiers with low voltage noise, such as the OP-27, will be the obvious choice, since they are inexpensive, and their comparatively large current noise will not affect the application (see Figure 1.61). At

medium resistances, the Johnson noise of resistors is dominant, while at very high resistances, we must choose an op amp with the smallest possible current noise, such as the AD549 or AD645.

Until recently, BiFET amplifiers tended to have comparatively high voltage noise (though very low current noise), and were thus more suitable for low noise applications in high rather than low impedance circuitry. The AD645

and AD743/AD745 have very low values of both voltage and current noise. The AD645 specifications at 10kHz are 10nV/√Hz and 0.6fA/√Hz, and the AD743/AD745 specifications at

10kHz are 2.9nV/√Hz and 6.9fA/√Hz. These make possible the design of low-noise amplifier circuits which have low noise over a wide range of source impedances.

## DIFFERENT AMPLIFIERS ARE BEST AT DIFFERENT IMPEDANCE LEVELS

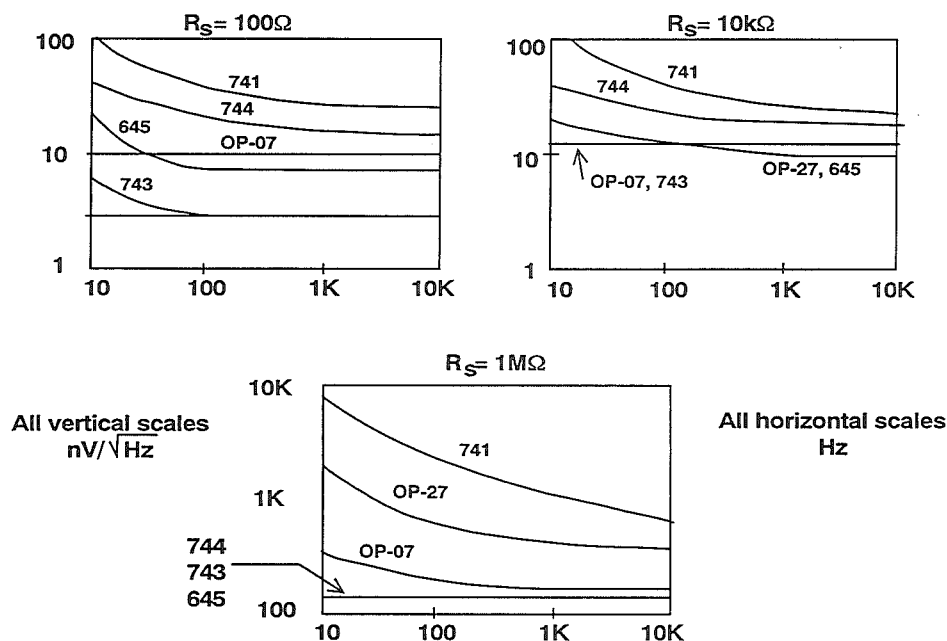


Figure 1.61

The *noise figure* of an amplifier is the amount (in dB) by which the noise of the amplifier exceeds the noise of a perfect noise-free amplifier in the same environment. The concept is useful in RF and TV applications, where 50Ω and 75Ω transmission lines and terminations are ubiquitous, but is useless for an op amp which may be used in a wide variety of electronic environments. Voltage noise spectral density and current noise spectral density are more useful specifications.

So far, we have assumed that noise is white (i.e., its spectral density does not

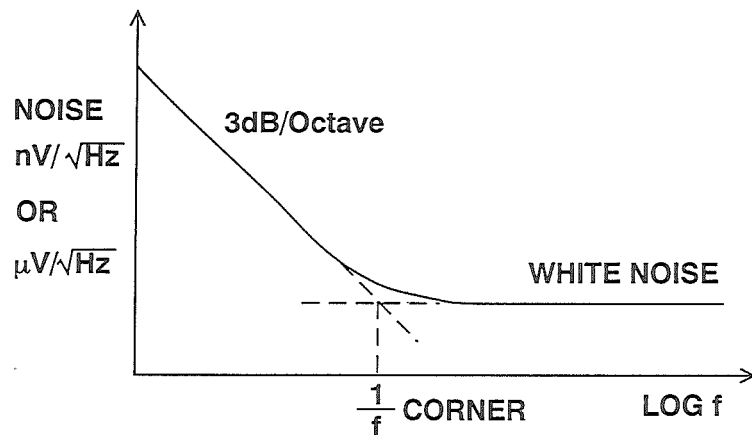
vary with frequency). This is true over most of an op amp's frequency range, but at low frequencies the noise spectral density rises at 3dB/octave as shown in Figure 1.63. The frequency at which it starts to rise is known as the 1/f corner frequency and is a figure of merit - the lower the better. The 1/f corner frequencies are not necessarily the same for the voltage noise and the current noise of a particular amplifier, and a current feedback op amp may have three 1/f corners: for its voltage noise, its inverting input current noise, and its non-inverting input current noise.

## NOISE FIGURE

- The *Noise Figure* of an amplifier in a particular circuit is the amount by which the noise of that circuit exceeds that of the same circuit when using a noise-free amplifier.
- Noise Figure is always specified at a particular source resistance (usually 50 or 75Ω)
- It is generally given in dB
- It is a somewhat useless concept for op amps, as they are used in too wide a range of environments

Figure 1.62

## FREQUENCY CHARACTERISTICS OF OP AMP NOISE



- 1/f Corner Frequency is a figure of merit for op amp noise performance (the lower the better)
- Typical Ranges: 2Hz to 2kHz
- Voltage Noise and Current Noise do not necessarily have the same 1/f corner frequency

Figure 1.63

The best low frequency low noise amplifiers have corner frequencies in the range 1-10Hz, while JFET devices and more general purpose op amps have values in the range to 100Hz. Very fast amplifiers, however, may make compromises in processing to achieve high

speed which result in quite poor 1/f corners of several hundred Hz or even 1-2kHz. This is generally unimportant in the applications for which they were intended, but may affect their use at audio frequencies.

## RMS Noise Considerations

As was discussed above, noise spectral density is a function of frequency. In order to obtain the RMS noise, the noise spectral density curve must be integrated over the bandwidth of interest.

In the 1/f region, the RMS noise in the bandwidth  $f_1$  to  $f_2$  is given by

$$e_{\text{rms}} = \sqrt{\int_{f_1}^{f_2} \frac{df}{f}} = k \sqrt{\ln \frac{f_2}{f_1}}$$

where  $k$  is the noise spectral density at 1Hz. The total 1/f noise in a given band

is a function of the ratio of the low and high band edge frequencies, since the actual frequency cancels out. It is necessary, however, that the upper band edge is still in the 1/f region for the above formula to be accurate.

In many cases, the low frequency noise is specified as a peak-to-peak value within the bandwidth 0.1 to 10Hz. This is measured by inserting a 0.1 to 10Hz bandpass filter between the op amp and the measuring device. The measurement is often presented as a scope photo with a time scale of 1s/div as shown in Figure 1.64 for the OP-213.

### THE 1/f NOISE IN THE BANDWIDTH 0.1Hz TO 10Hz IS LESS THAN 120nV PEAK-TO-PEAK FOR THE OP-213

SCALES

VERTICAL:  
20nV/div.

HORIZONTAL:  
1s/div.

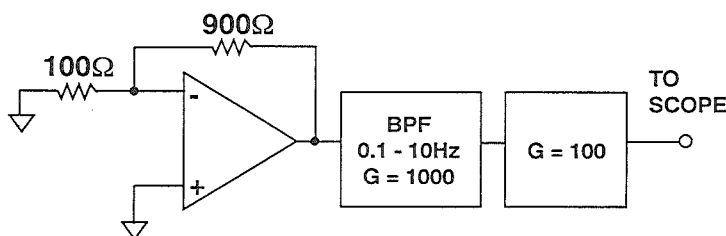
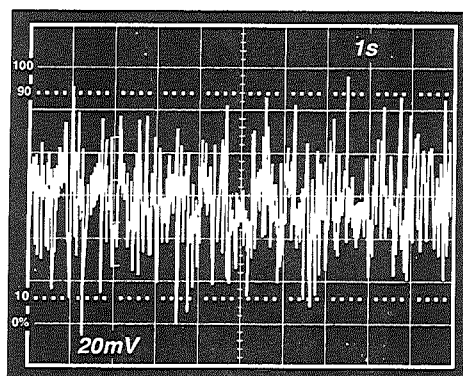


Figure 1.64

In practice, it is virtually impossible to measure noise within specific frequency limits with no contribution from outside those limits, since practical filters have finite rolloff characteristics. Fortunately, the measurement error introduced by a single pole lowpass filter is readily computed. The noise in the spectrum above the single pole filter cutoff frequency,  $f_c$ , extends the corner

frequency to  $1.57f_c$ . Similarly, a two pole filter has an apparent corner frequency of approximately  $1.2f_c$ . The error correction factor is usually negligible for filters having more than two poles. The bandwidth obtained after applying the correction factor is referred to as the *equivalent noise bandwidth* of the filter (see Figure 1.65).

## EQUIVALENT NOISE BANDWIDTH

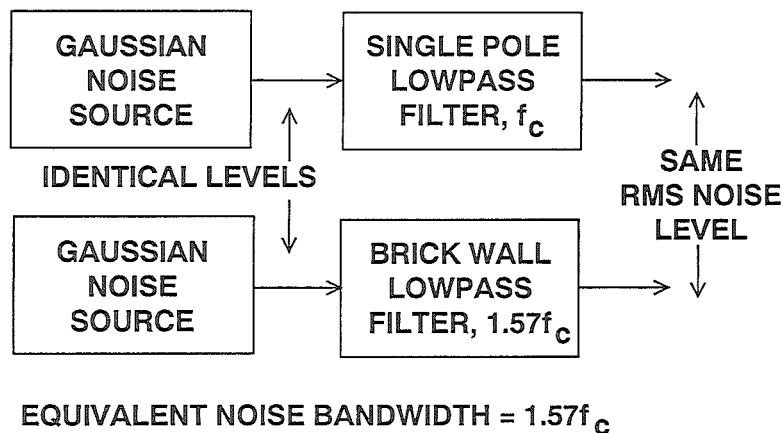


Figure 1.65

When computing RMS noise for wide bandwidth op amps,  $1/f$  noise becomes relatively insignificant. The dominant source of noise is *gaussian*, or white noise. This noise has a relatively constant noise spectral density over a wide range of frequencies. The RMS noise calculation is made by multiplying the noise spectral density by the square root of the equivalent noise bandwidth.

It is often desirable to convert RMS noise measurements into peak-to-peak. In order to do this, one must have some understanding of the statistical nature of noise. For Gaussian noise

and a given value of RMS noise, statistics tell us that the chance of a particular peak-to-peak value being exceeded decreases sharply as that value increases - but this probability never becomes zero. Thus, for a given RMS noise, it is possible to predict the percentage of time that a given peak-to-peak value will be exceeded, but it is not possible to give a peak-to-peak value which will never be exceeded (see Figure 1.66). Peak-to-peak noise specifications, therefore, must always be written with a time limit. A suitable one is 6.6 times the RMS value which is exceeded only 0.1% of the time.

## RMS TO PEAK-TO-PEAK RATIOS

Nominal Peak-to-Peak	% of the Time Noise will Exceed Nominal Peak-to-Peak Value
$2 \times \text{rms}$	32%
$3 \times \text{rms}$	13%
$4 \times \text{rms}$	4.6%
$5 \times \text{rms}$	1.2%
$6 \times \text{rms}$	0.27%
$6.6 \times \text{rms}^{**}$	0.10%
$7 \times \text{rms}$	0.046%
$8 \times \text{rms}$	0.006%

**\*\* Most often used conversion factor is 6.6**

Figure 1.66

### Total Output Noise Calculations

We have already pointed out that any noise source which produces less than one third to one fifth of the noise of some other source can be ignored. (Both noise voltages must be measured at the same point in the circuit.) To analyze the noise performance of an op amp circuit, we must assess the noise contributions of each part of the circuit and determine which are significant. To simplify the following calculations, we shall work with noise spectral densities, rather than actual voltages, to leave bandwidth out of the expressions (the noise spectral density, which is generally expressed in  $\mu\text{V}/\sqrt{\text{Hz}}$ , is equivalent to the noise in a 1 Hz bandwidth).

If we consider the circuit in Figure 1.67, which is an amplifier consisting of an op amp and three resistors ( $R_p$  represents the source resistance at node A), we can find six separate noise sources: the Johnson noise of the three resistors, the op amp voltage noise, and the current noise in each input of the op amp. Each has its own contribution to the noise at the amplifier output. (Noise is generally specified RTI, or *referred to the input*, but it is often simpler to calculate the noise at the output and then divide it by the *signal* gain (not the *noise* gain) of the amplifier to obtain the RTI noise).

## OP AMP NOISE MODEL SHOWING REACTIVE ELEMENTS

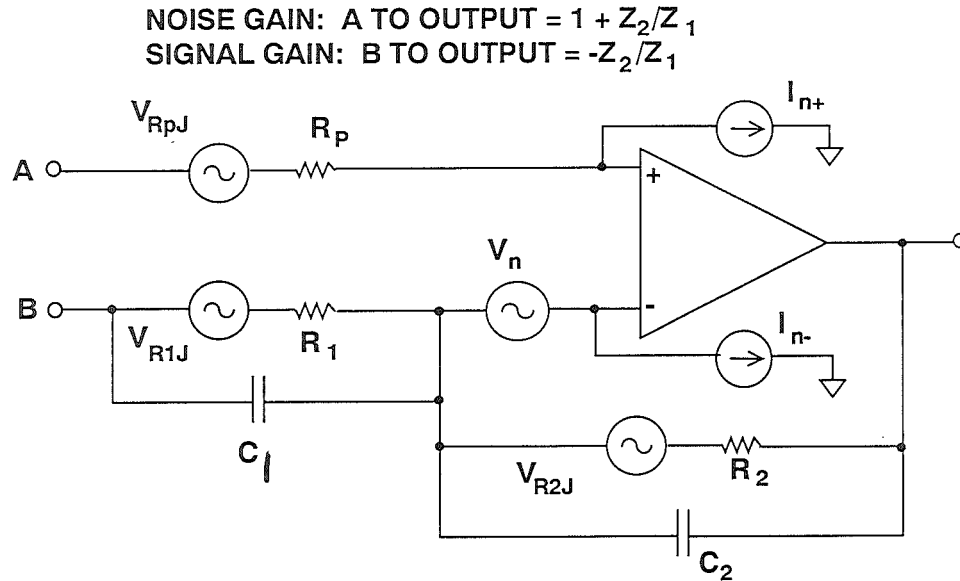


Figure 1.67

The circuit represents a second-order system, where capacitor  $C_1$  represents the source capacitance, stray capacitance on the inverting input, the input capacitance of the op amp, or any combination of these.  $C_1$  causes a breakpoint in the noise gain, and  $C_2$  is

the capacitor which must be added to obtain stability. Because of  $C_1$  and  $C_2$ , the noise gain is a function of frequency, and has peaking at the higher frequencies (assuming  $C_2$  is selected to make the second-order system critically damped).

A DC signal applied to input A (B being grounded) sees a gain of:

$$1 + R_2/R_1 = \text{DC Noise Gain} \quad [1a]$$

At higher frequencies, the gain from input A to the output becomes:

$$1 + C_2/C_1 = \text{AC Noise Gain} \quad [1b]$$

The closed-loop bandwidth  $f_{c1}$  is the point at which the Noise Gain intersects the open-loop gain.

A DC signal applied to B (A being grounded) sees a gain of:

$$-R_2/R_1 \quad [2a]$$

with a high frequency cutoff determined by  $R_2C_2$ :

$$\text{Bandwidth (B to Output)} = 1/2\pi R_2C_2 \quad [2b]$$



These are the non-inverting and inverting gains and bandwidths, respectively, of the amplifier.

The current noise of the non-inverting input,  $I_{n+}$ , flows in  $R_p$  and gives rise to a noise voltage of  $I_{n+}R_p$ , which is amplified by [1a, 1b], as are the op amp noise voltage,  $V_n$ , and the Johnson

noise of  $R_p$ , which is  $\sqrt{4kTR_p}$ . The Johnson noise of  $R_1$  is amplified by [2a] over a bandwidth of  $1/2\pi R_2 C_2$  [2b], and the Johnson noise of  $R_2$  is not amplified at all but is buffered directly to the output over a bandwidth of  $1/2\pi R_2 C_2$ . The current noise of the inverting input,  $I_{n-}$ , does not flow in  $R_1$ , as might be expected - negative feedback around the amplifier works to keep the potential at the inverting input unchanged, so that a current flowing from that pin is forced, by negative feedback, to flow in  $R_2$  only, resulting in a voltage at the amplifier output of  $I_{n-}R_2$  over a bandwidth of  $1/2\pi R_2 C_2$  (we could equally well consider the voltage caused by  $I_{n-}$  flowing in the parallel combination of  $R_1$  &  $R_2$  and then amplified by the noise gain of the amplifier (see below), but the results are identical — only the calculations are more involved).

If we consider these six noise contributions, we see that if  $R_p$  and  $R_2$  are low, then the effect of current noise and Johnson noise will be minimized, and the dominant noise will be the op amp's voltage noise. As we increase resistance, both Johnson noise and the voltage noise produced by noise currents will rise. If noise currents are low, then Johnson noise will take over from voltage noise as the dominant contributor. Johnson noise, however, rises with the square root of the resistance, while the current noise voltage rises linearly

with resistance, so ultimately, as the resistance continues to rise, the voltage due to noise currents will become dominant.

These noise contributions we have analyzed are not affected by whether the input is connected to node A or node B (the other being grounded or connected to some other low-impedance voltage source), which is why the non-inverting gain  $(1 + R_2/R_1)$ , which is seen by the voltage noise of the op amp,  $V_n$ , is known as the "noise gain" of the amplifier.

Calculating the total output RMS noise of the op amp requires multiplying each of the six noise voltages by the appropriate gain and integrating over the appropriate frequency as shown in Figure 1.68. The root-sum-square of all the output contributions then represents the total RMS output noise. Fortunately, this cumbersome exercise may be greatly simplified in most cases by making the appropriate assumptions.

The noise gain for a typical second-order system is shown in Figure 1.69. It is quite easy to perform the voltage noise integration in two steps, but notice that because of peaking, the majority of the output noise due to the input voltage noise will be determined by the high frequency portion where the noise gain is  $1 + C_1/C_2$ . This type of response is typical of second-order systems. The noise due to the inverting input current noise,  $R_1$ , and  $R_2$  is only integrated over the bandwidth  $1/2\pi R_2 C_2$ . The appropriate model for the second-order system (neglecting resistor noise) is shown in Figure 1.70.

## REFERRING ALL NOISE SOURCES TO THE OUTPUT

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFLECT TO OUTPUT	INTEGRATION BANDWIDTH
Johnson Noise in $R_p$ : $\sqrt{4kTR_p}$	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Non-Inverting Input Current Noise Flowing in $R_p$ : $I_{n+}R_p$	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Input Voltage Noise: $V_n$	Noise Gain as a Function of Frequency	Closed Loop BW (Signal BW from A to Output)
Johnson Noise in $R_1$ : $\sqrt{4kTR_1}$	$-R_2/R_1$ (Signal Gain from B to Output)	$1/2\pi R_2C_2$ (Signal BW from B to Output)
Johnson Noise in $R_2$ : $\sqrt{4kTR_2}$	1	$1/2\pi R_2C_2$ (Signal BW from B to Output)
Inverting Input Current Noise Flowing in $R_2$ : $I_{n-}R_2$	1	$1/2\pi R_2C_2$ (Signal BW from B to Output)

Figure 1.68

## NOISE GAIN AND INVERTING SIGNAL GAIN FOR SECOND-ORDER SYSTEM

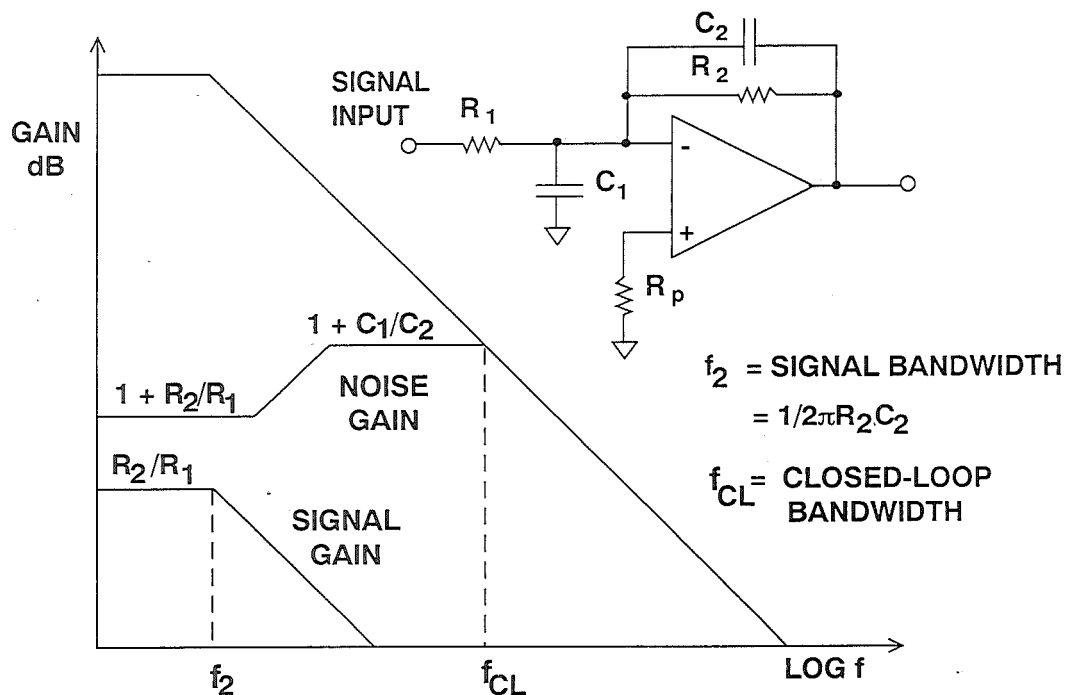
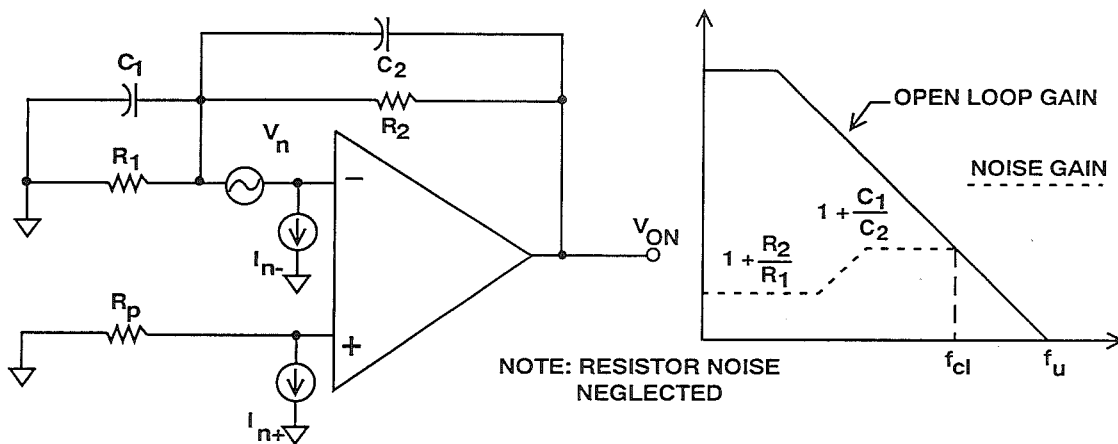


Figure 1.69

## NOISE MODEL FOR A TYPICAL SECOND-ORDER SYSTEM WHICH NEGLECTS RESISTOR NOISE



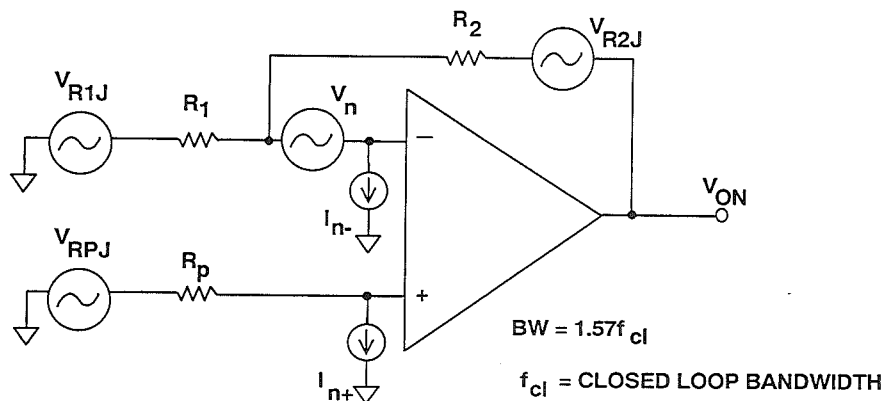
$$V_{ON} \sim \sqrt{V_n^2 \left[ 1 + \frac{C_1}{C_2} \right]^2 (1.57 f_{cl}) + I_{n-}^2 R_2^2 (1.57 f_2) + I_{n+}^2 R_p^2 \left[ 1 + \frac{C_1}{C_2} \right]^2 (1.57 f_{cl})}$$

Where  $f_u$  = Op Amp Unity Gain Bandwidth Frequency

$$f_{cl} = \text{Closed Loop Bandwidth} = \frac{f_u}{1 + \frac{C_1}{C_2}}, \quad f_2 = \text{Signal Bandwidth} = \frac{1}{2\pi R_2 C_2}$$

Figure 1.70

## OP AMP NOISE MODEL FOR A FIRST-ORDER CIRCUIT WITH CONSTANT NOISE GAIN



$$V_{ON} = \sqrt{BW \left[ I_{n-}^2 R_2^2 + I_{n+}^2 R_p^2 \left[ 1 + \frac{R_2}{R_1} \right]^2 + V_n^2 \left[ 1 + \frac{R_2}{R_1} \right]^2 + 4kTR_2 + 4kTR_1 \left[ \frac{R_2}{R_1} \right]^2 + 4kTR_p \left[ 1 + \frac{R_2}{R_1} \right]^2 \right]}$$

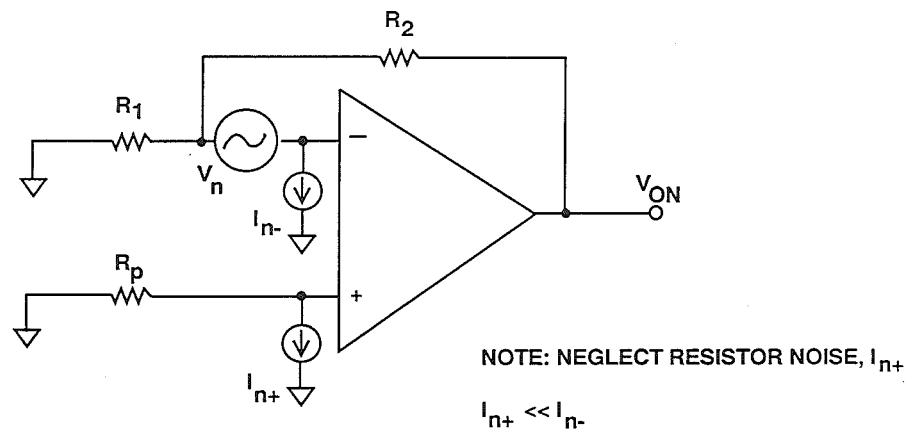
Figure 1.71

In high speed op amp applications, there are some further simplifications which can be made. The noise gain plot for a first-order system optimized for fast settling time is usually flat up to the closed-loop bandwidth frequency, with only a dB or so of gain peaking at the most. All noise sources may therefore be integrated over the closed-loop op amp bandwidth as shown in Figure

1.71. It is also safe to neglect resistor noise if feedback resistors are 1kΩ or less.

In high speed current feedback op amp circuits, the input voltage noise and the inverting input current noise are the dominant contributors to the output noise as shown in Figure 1.72.

### NOISE MODEL FOR HIGH SPEED CURRENT FEEDBACK CIRCUIT



$$V_{ON} = \sqrt{1.57 f_{cl}} \sqrt{V_n^2 \left[ 1 + \frac{R_2}{R_1} \right]^2 + I_{n-}^2 R_2^2}$$

$f_{cl}$  = CLOSED LOOP BANDWIDTH

Figure 1.72

### Op Amp Distortion

Dynamic range of an op amp may be defined in several ways. The most common ways are to specify Harmonic Distortion, Total Harmonic Distortion (THD), or Total Harmonic Distortion Plus Noise (THD + N).

calculated by taking the root sum of the squares of the first five or six harmonics of the fundamental. In many practical situations, however, there is negligible error if only the second and third harmonics are included.

The distortion component which makes up Total Harmonic Distortion is usually

## DEFINITIONS OF THD AND THD + N

- $V_S$  = Signal Amplitude (rms Volts)
- $V_2$  = Second Harmonic Amplitude (rms Volts)
- $V_n$  = nth Harmonic Amplitude (rms Volts)
- $V_{\text{noise}}$  = rms value of noise over measurement bandwidth

- $$\text{THD} + N = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2 + V_{\text{noise}}^2}}{V_S}$$

- $$\text{THD} = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_S}$$

Figure 1.73

It is important to note that the THD measurement does not include noise terms, while THD + N does. The noise in the THD + N measurement must be integrated over the measurement bandwidth. In audio applications, the bandwidth is normally chosen to be around 100kHz. In narrow-band applications, the level of the noise may be reduced by filtering. On the other hand, harmonics and intermodulation products which fall within the measurement bandwidth cannot be filtered, and therefore may limit the system dynamic range.

Consider the example of the simple wideband op amp circuit shown in Figure 1.74. The AD9622 is a high speed low distortion voltage feedback op amp optimized for use in a gain-of-two configuration. The input voltage noise of

3.5nV/√Hz is reflected to the output by multiplying by the noise gain, 2. The 7nV/√Hz is then integrated over the closed loop small signal bandwidth of the op amp, which is approximately 230MHz. This yields a total integrated output noise of 133μV RMS. The output noise due to the op amp input current noise and the thermal noise of the resistors is negligible in this example. The corresponding signal-to-noise ratio (neglecting distortion) for a 2V peak-to-peak sinewave output is 74.5dB. Under these conditions, however, the harmonic distortion of the AD9622 is approximately -75dBc at 2MHz. With no filtering, the dynamic range is thus equally limited by the noise and the distortion. If, however, the output of the op amp is filtered, the dynamic range is limited by the distortion.

## OUTPUT NOISE AND DISTORTION OF AD9622 WIDEBAND VOLTAGE FEEDBACK OP AMP

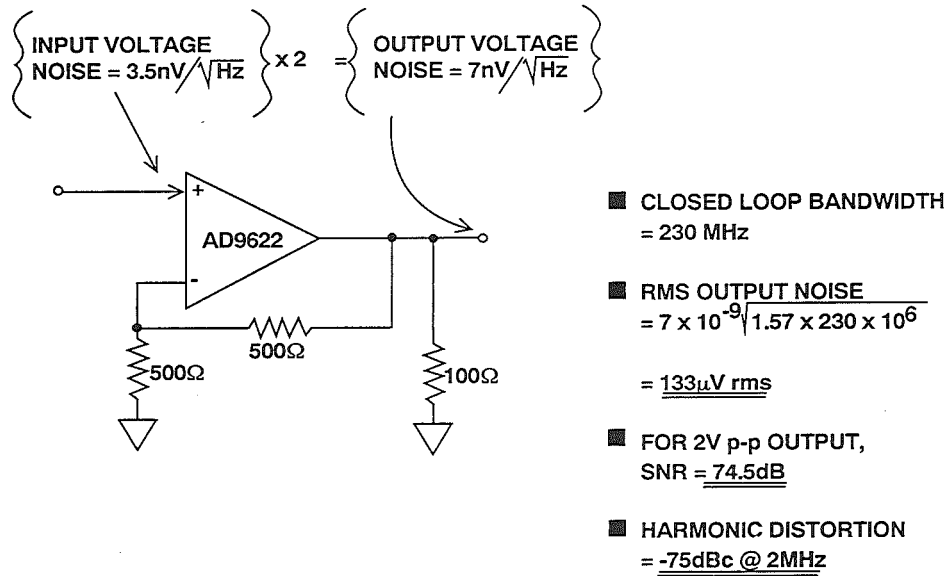


Figure 1.74

Rather than simply examining the THD produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones. As shown in Figure 1.75, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies,  $f_1$  and  $f_2$ , to a nonlin-

ear device. The second order products located at  $f_2 + f_1$  and  $f_2 - f_1$  are located far away from the two tones, and may be removed by filtering. The third order products located at  $2f_1 + f_2$  and  $2f_2 + f_1$  may likewise be filtered. The third order products located at  $2f_1 - f_2$  and  $2f_2 - f_1$ , however, are close to the original tones, and filtering them is difficult.

## SECOND AND THIRD-ORDER INTERMODULATION PRODUCTS FOR $f_1 = 5\text{MHz}$ , $f_2 = 6\text{MHz}$

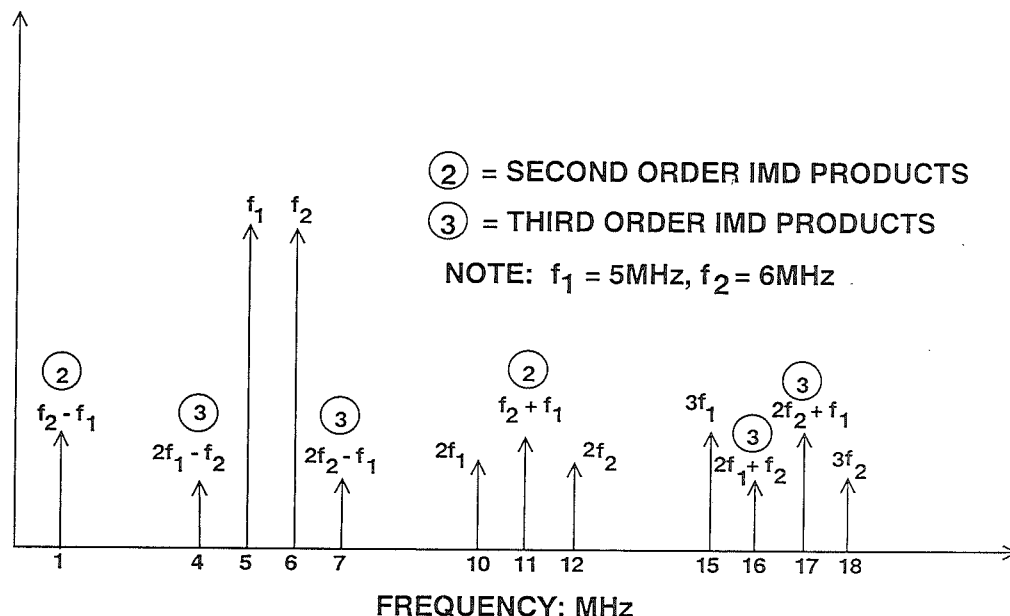


Figure 1.75

Intermodulation distortion products are of special interest in the RF area, and a major concern in the design of radio receivers. Third-order IMD products can mask out small signals in the presence of larger ones. Third order IMD is often specified in terms of the *third order intercept* point as shown in Figure 1.76. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third-order products (referenced to a single tone) is plotted as a function of input signal power. If the system non-linearity is approximated by a power series expansion, the second-order IMD amplitudes increase 2dB for every 1dB of signal increase. Similarly, the third-order IMD amplitudes increase 3dB for every 1dB of signal increase. With a low level two-tone input signal, and two data points,

draw the second and third order IMD lines as are shown in Figure 1.76, because one point and a slope determine each straight line.

Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress. But the second and third-order intercept lines may be extended to intersect the extension of the output signal line. These intersections are called the *second-* and *third order intercept points*, respectively. The values are usually referenced to the output power of the device expressed in dBm. Another parameter which may be of interest is the *1dB compression point*. This is the point at which the output signal is compressed by 1dB from the ideal input/output transfer function. This point is also shown in Figure 1.76.

## INTERCEPT POINTS, GAIN COMPRESSION, AND IMD

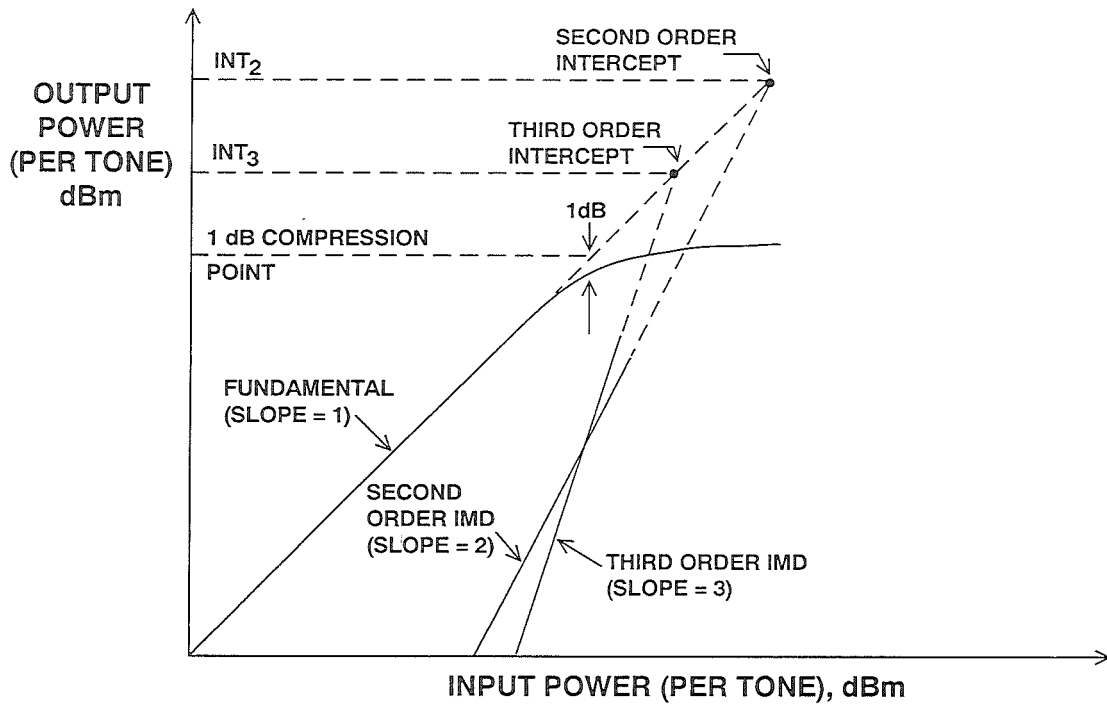


Figure 1.76

Knowing the third order intercept point allows calculation of the approximate level of the third-order IMD products as a function of output signal level. Figure

1.77 shows the third order intercept value as a function of frequency for the AD9622 voltage feedback amplifier.

## AD9622 THIRD ORDER IMD INTERCEPT VERSUS FREQUENCY

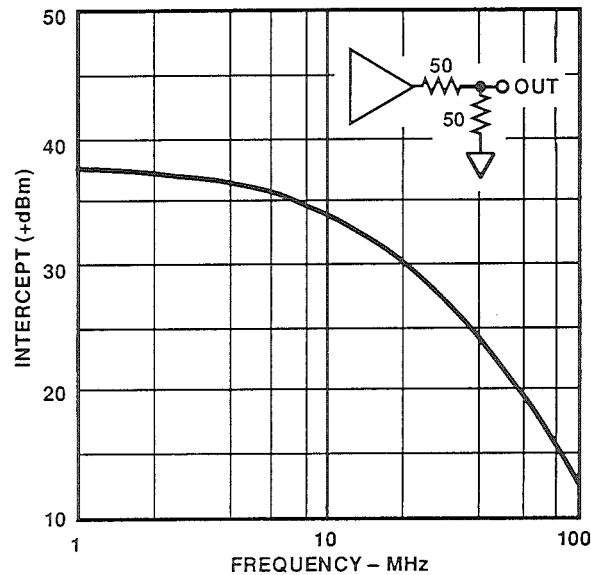


Figure 1.77



Assume the op amp output signal is 5MHz and 2V peak-to-peak into a 100Ω load (50Ω source and load termination). The voltage into the 50Ω load is therefore 1V peak-to-peak, corresponding to +4dBm. The value of the third order intercept at 5MHz is 36dBm. The difference between +36dBm and +4dBm is 32dB. This value is then multiplied

by 2 to yield 64dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be -64dBc (dB below carrier frequency), or at a level of -60dBm. Figure 1.78 shows the graphical analysis for this example.

### USING THE THIRD ORDER INTERCEPT POINT TO CALCULATE IMD PRODUCT FOR THE AD9622 OP AMP

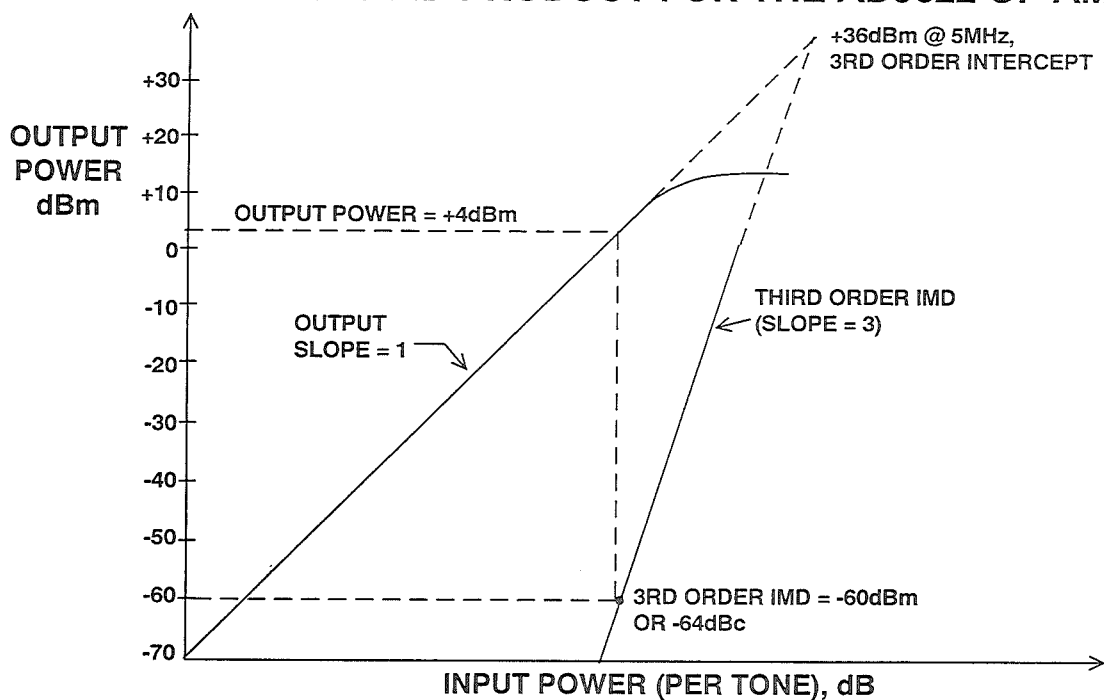


Figure 1.78

## Common-Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio (PSRR)

If a signal is applied equally to both inputs of an op amp, so that the differential input voltage is unaffected, the output should not be affected. In practice, changes in common-mode voltage will produce changes in output. The *common-mode rejection ratio* or CMRR is the ratio of the common-mode gain to the differential-mode gain of an op amp. For example, if a differential input change of  $Y$  volts will produce a change of 1V at the output, and a common-mode change of  $X$  volts produces a similar change of 1V, then the CMRR is  $X/Y$ . It is normally expressed in dB, and typical LF values are between 70 and 120dB. At higher frequencies, CMRR deteriorates — many op amp data sheets show a plot of CMRR versus frequency.

method shown in Figure 1.79 uses four precision resistors to configure the op amp as a differential amplifier, a signal is applied to both inputs, and the change in output is measured — an amplifier with infinite CMRR would have no change in output. The disadvantage inherent in this circuit is that the ratio match of the resistors is as important as the CMRR of the op amp. A mismatch of 0.1% between resistor pairs will result in a CMRR of only 66dB, no matter how good the op amp. Since most op amps have LF CMRRs of between 80 and 120dB, it is clear that this circuit is only marginally useful for measuring CMRR (although it does an excellent job in measuring its own resistance match!).

The common-mode rejection ratio can be measured in several ways. The

### SIMPLE COMMON-MODE REJECTION RATIO (CMRR) TEST CIRCUIT

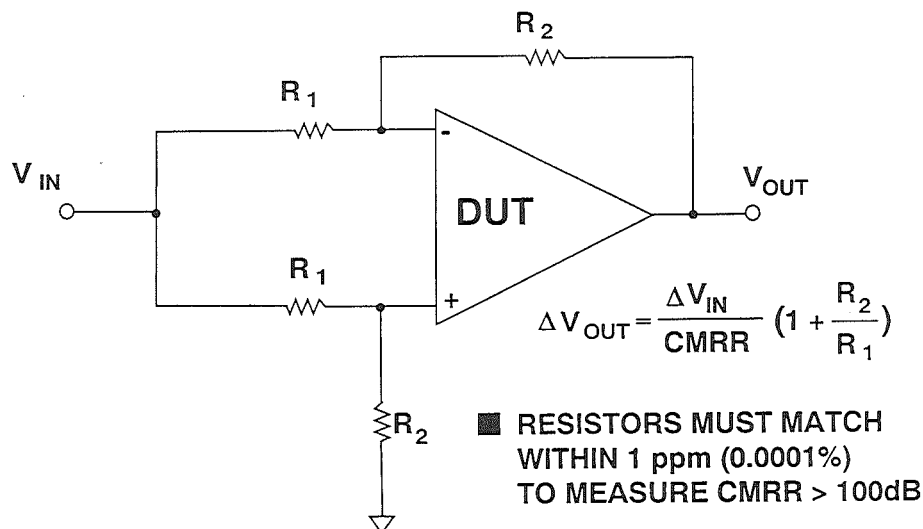


Figure 1.79

The slightly more complex circuit shown in Figure 1.80 measures CMRR without requiring accurately matched resistors. In this circuit, the common-mode voltage is changed by switching the power supply voltages. (This is easy to implement in a test facility, and the same circuit with different supply voltage connections can be used to measure

power supply rejection ratio). The power supply values shown in the circuit are for a  $\pm 15V$  op amp with a common-mode voltage of  $\pm 10V$ . Other supplies and common-mode ranges can be accommodated by changing the voltages appropriately. The amplifier A1 should have high gain, low  $V_{OS}$  and low  $I_b$ .

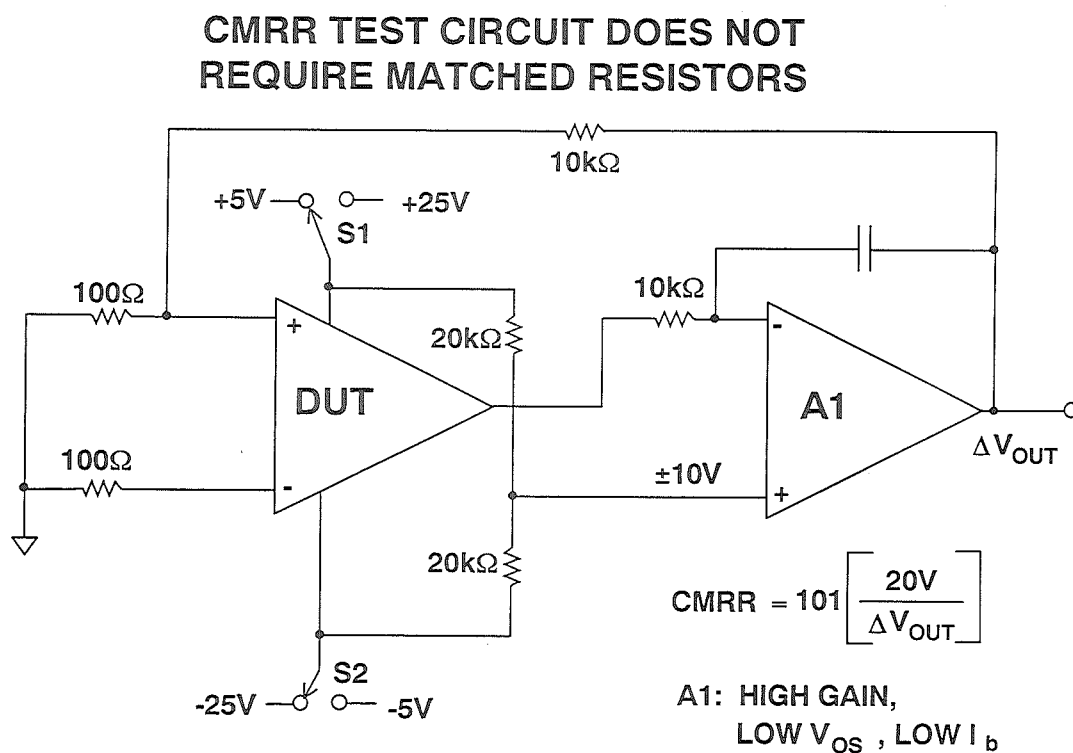


Figure 1.80

Finite CMRR produces a corresponding output offset voltage error in op amps configured in the non-inverting mode as shown in Figure 1.81. Op amps config-

ured in the inverting mode have no CMRR output error because both inputs are at ground or virtual ground, so there is no common-mode voltage.

## CALCULATING OUTPUT OFFSET ERROR DUE TO CMRR

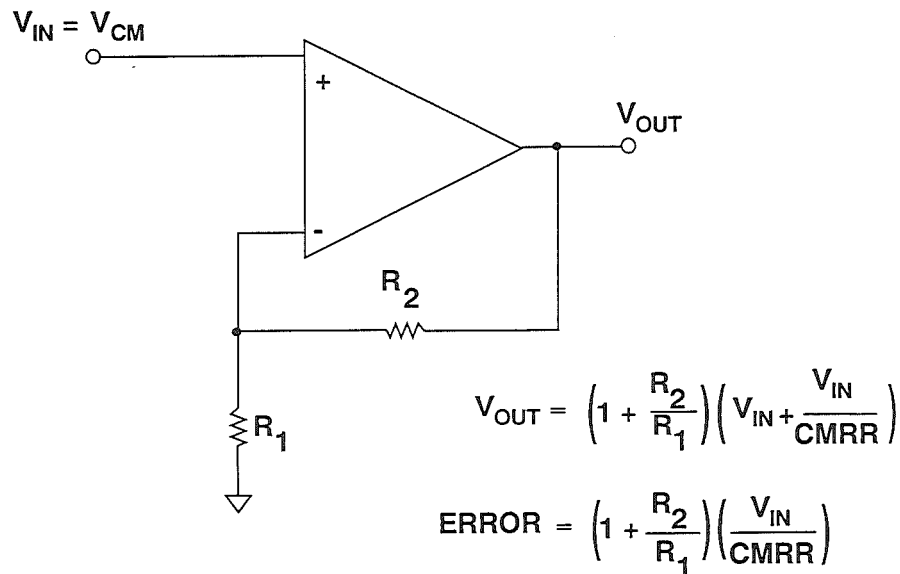


Figure 1.81

If the supply of an op amp changes, its output should not, but it does. The specification of *power supply rejection ratio* or PSRR is defined similarly to the definition of CMRR. If a change of X volts in the supply produces the same output change as a differential input change of Y volts, then the PSRR on that supply is X/Y. The definition of PSRR assumes that both supplies are altered equally in opposite directions - otherwise the change will

introduce a common-mode change as well as a supply change, and the analysis becomes considerably more complex. It is this effect which causes apparent differences in PSRR between the positive and negative supplies. The test setup used to measure CMRR may be modified to measure PSRR as shown in Figure 1.82. The voltages are chosen for a symmetrical power supply change of 1V. Other values may be used where appropriate.

## TEST SETUP FOR MEASURING POWER SUPPLY REJECTION RATIO (PSRR)

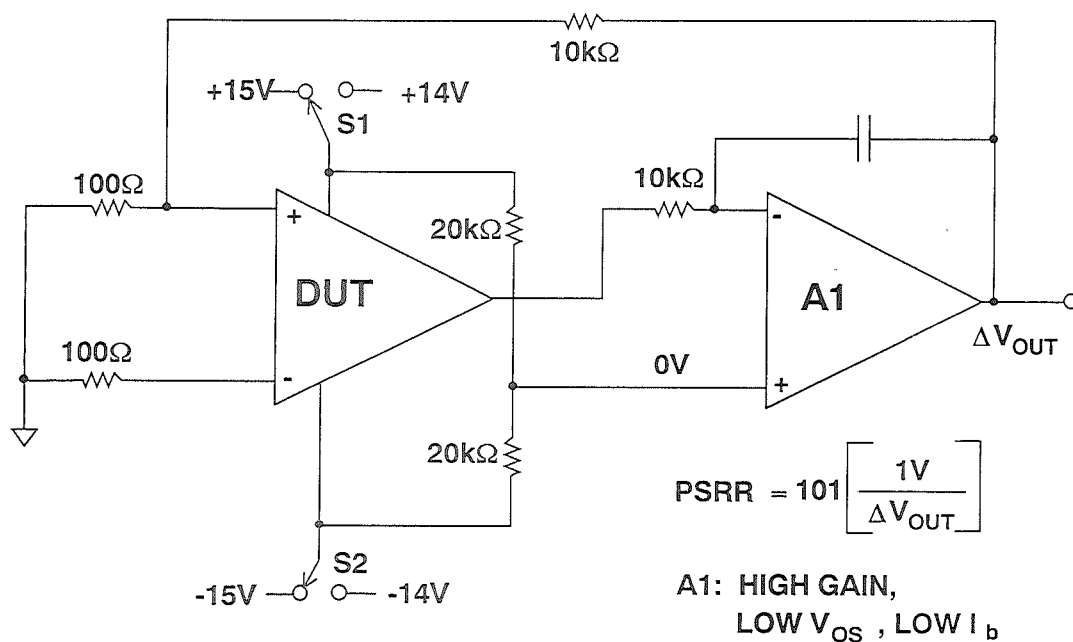


Figure 1.82

## BOTH CMRR AND PSRR ARE FREQUENCY DEPENDENT (DATA SHOWN FOR AD9617 OP AMP)

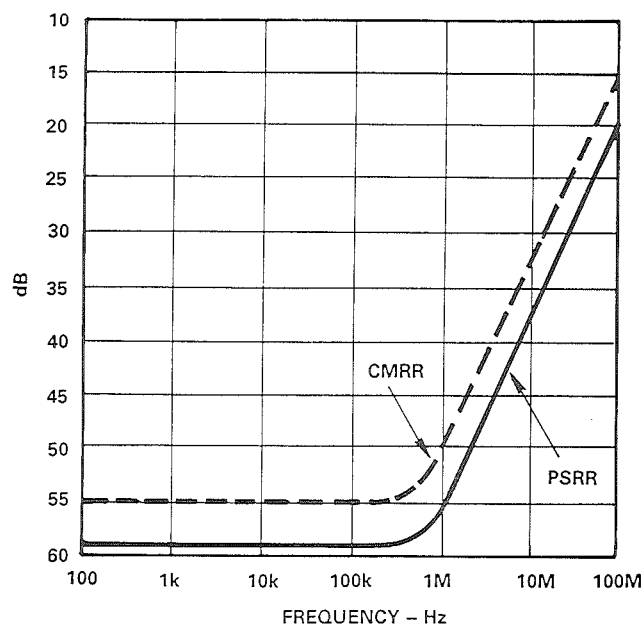


Figure 1.83

## Power Supplies and Decoupling

It is because the PSRR of op amps is frequency dependent that op amp power supplies must be well decoupled. At low frequencies, several devices may share a 10 - 50 $\mu$ F capacitor on each supply, provided it is no more than 10cm (PC track distance) from any of them. At

high frequencies, each IC must have every supply decoupled by a low inductance 0.1 $\mu$ F (or so) capacitor with short leads and PC tracks. These capacitors must also provide a return path for HF currents in the op amp load. (See Reference 8).

### PROPER LOW AND HIGH-FREQUENCY DECOUPLING TECHNIQUES FOR OP AMPS

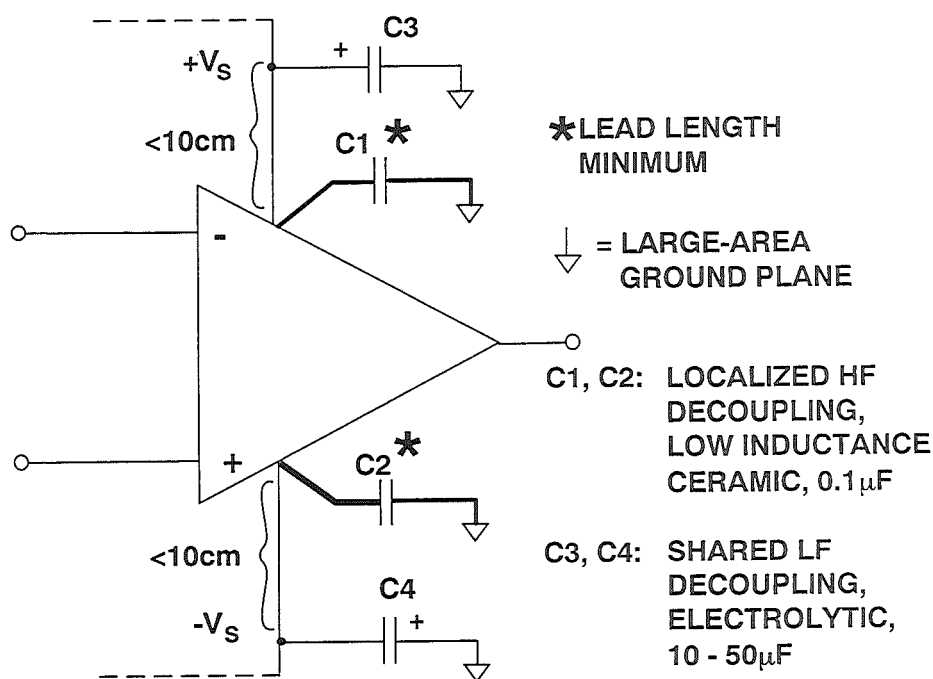


Figure 1.84

## Power Supplies and Power Dissipation

Op amps have no ground terminal. Specifications of power supply are quite often in the form  $\pm X$  Volts, but in fact it might equally be expressed as  $2X$  Volts. What is important is where the common-mode range and output swings lie relative to the supplies. This information may be provided in tabular form or as a graph. Graphs are usually more informative, but tables containing minima and maxima make worst case design easier.

Often data sheets will advise that an op amp will work over a range of supplies (from +3 to  $\pm 16.5$  V for example), and will then give parameters at several values of supply, so that users may extrapolate between them. If the minimum supply is quite high, it is usually because the device contains some structure which requires high voltage to function (a zener diode, for instance).

## POWER SUPPLIES

- Op Amp supplies can vary from +1.5V to  $\pm 25$ V
- Do not use an Op Amp outside the specified supply range
- Most data sheets show how performance varies with supply
- Every op amp should have its supply pins well decoupled at HF

Figure 1.85

Data sheets also give current consumption. Any current flowing into one supply pin will flow out of the other or out of the output terminal. When the output is open circuit, the dissipation is easily calculated from the supply voltage and current. When current flows in a load, it is easiest to calculate the total dissipation (remember that if the load is grounded to the center rail the load current flows from a supply to ground,

not between supplies), and then subtract the load dissipation to obtain the device dissipation.

The data sheet will normally give details of thermal resistances  $\theta_{ja}$  (junction-to-ambient),  $\theta_{jc}$  (junction-to-case), and maximum junction temperature ratings, from which dissipation limits may be calculated knowing ambient or case temperatures.

## OP AMP POWER DISSIPATION

- Fast op amps run hot and may require heat sinks
- Calculate no-load dissipation from the data sheet values
- Calculate total power dissipation (including the load)
- Subtract the load dissipation
- Check that the remaining total is within permitted limits
- Use  $\theta_{ja}$  and/or  $\theta_{jc}$  to calculate maximum operating junction temperature and check that it is within limits

Figure 1.86



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## SECTION 2

### SPECIAL PURPOSE AMPLIFIERS

2

- Instrumentation Amplifiers (In-Amps):  
Instrumentation Amplifier Configurations,  
Instrumentation Amplifier DC Error Sources,  
Instrumentation Amplifier Noise Sources
- Active Feedback Amplifiers
- Programmable Gain Amplifiers
- Isolation Amplifiers
- Comparators

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## LINEAR DESIGN SEMINAR

## SECTION 2

## SPECIAL PURPOSE AMPLIFIERS

*Walt Kester, Joe Buxton*

2

## INSTRUMENTATION AMPLIFIERS (IN-AMPS)

An instrumentation amplifier is a closed-loop gain block which has a differential input and an output which is single-ended with respect to a reference terminal. The input impedances are balanced and have high values, typically  $10^9\Omega$  or higher. Unlike an op amp, which has its closed-loop gain determined by external resistors connected between its inverting input and

its output, an in-amp employs an internal feedback resistor network which is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set by an internal (via pins) or external gain resistor, which is also isolated from the signal inputs. Typical in-amp gain settings range from 1 to 10,000.

## INSTRUMENTATION AMPLIFIER

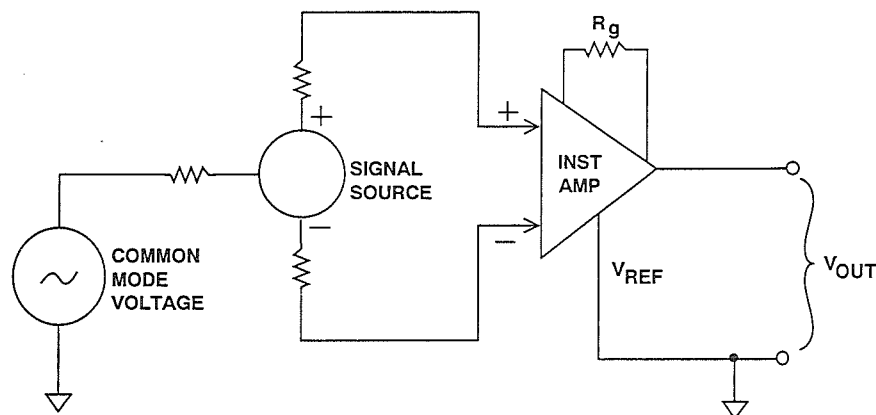
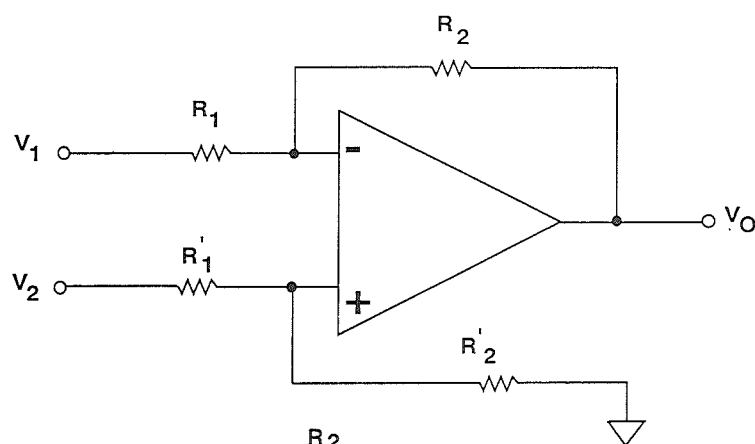


Figure 2.1

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals, while simultaneously rejecting volts of common-mode signal at its inputs. This requires that in-amps have very high common-mode rejection (CMR): typical values of CMR are 70dB to over 100dB, with CMR usually improving at higher gains. Op amps, connected as subtractors as shown in Figure 2.2, provide common-mode

rejection, but require closely matched external resistors. A mismatch of only 0.1% in the resistor ratios will reduce the CMR to approximately 66dB. Another problem with the simple op amp subtractor is that the input impedances are relatively low and are unbalanced between the two sides. (The input impedance seen by  $V_1$  is  $R_1$ , and the input impedance seen by  $V_1'$  is  $R_1' + R_2'$ .)

## OP-AMP SUBTRACTOR



$$\blacksquare \quad V_O = (V_2 - V_1) \frac{R_2}{R_1}$$

$$\blacksquare \quad \frac{R_2}{R_1} = \frac{R_2'}{R_1'} \quad \text{CRITICAL FOR HIGH CMR}$$

$$\blacksquare \quad \geq 0.1\% \text{ MISMATCH YIELDS } \leq 66\text{dB CMR}$$

Figure 2.2

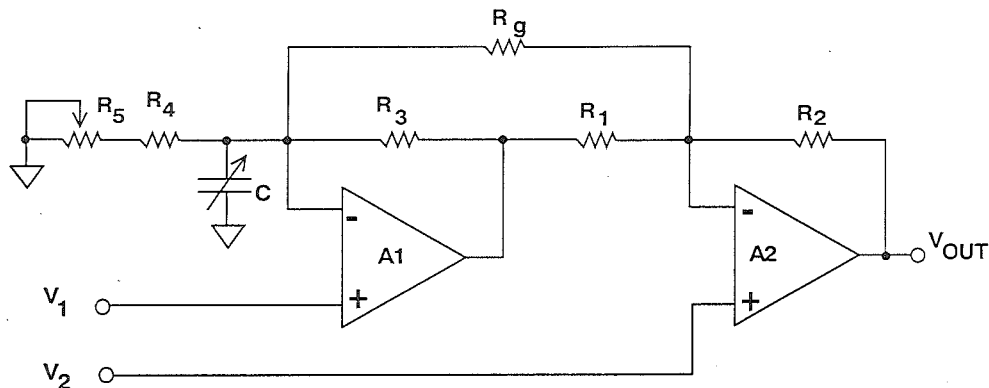
## Instrumentation Amplifier Configurations

Instrumentation amplifier configurations are based on op amps, but the simple subtractor circuit described above lacks the performance required for precision applications. An in-amp architecture which overcomes some of the weaknesses of the subtractor circuit uses two op amps as shown in Figure 2.3. The circuit gain may be trimmed with an external resistor,  $R_g$ . The input impedance is high, permitting the signal sources to have high and unbalanced output impedance. One major disadvantage of this design is that common-mode voltage input range must be traded off against gain. The amplifier A1 must amplify a common-mode signal by

If  $R_3 > (R_4 + R_5)$ , saturation of A1 will occur if the common-mode signal is too high, leaving no headroom to amplify the wanted differential signal. If  $R_3 < (R_4 + R_5)$ , low gains cannot be realized, and since the two amplifiers are operating at different closed-loop gains (and thus at different bandwidths), there will be generally poor AC common-mode rejection without the use of the AC CMR trim capacitor shown in the diagram. Resistor  $R_5$  allows DC CMR to be optimized. Best gain TC results when the resistors are ratio-matched. If  $R_g$  is external to a thin film array, this goal is compromised.

$$\frac{R_3 + R_4 + R_5}{R_4 + R_5}.$$

### TWO OP-AMP INSTRUMENTATION AMPLIFIER



$$\blacksquare \quad V_{OUT} = (V_2 - V_1) \left( 1 + \frac{R_2}{R_1} + \frac{2R_2}{R_g} \right)$$

$$\blacksquare \quad \text{FOR } R_1 = R_3 \text{ AND } R_2 = R_4 + R_5$$

$$\blacksquare \quad R_5 = \text{DC CMR TRIM}$$

$$\blacksquare \quad C = \text{AC CMR TRIM}$$

Figure 2.3



For true balanced high impedance inputs, three op amps may be connected to form the in-amp shown in Figure 2.4. The gain of the amplifier is set by the resistor,  $R_g$ , which may be internal, external, or pin-programmable. In this configuration, gain accuracy and CMR depend upon the ratio matching of  $R_3/R_2$  to  $R_3'/R_2'$ . CMR does not depend on the matching of  $R_1$  to  $R_2'$ , and gain may be adjusted by  $R_g$  without affecting the common-mode error signal. Thus, CMR will theoretically increase in direct proportion to gain. Furthermore, common-mode signals are only amplified by a factor of 1 regardless of gain

(no common-mode voltage will appear across  $R_g$ , hence, no common-mode current will flow in it because the input terminals of an op amp will have no significant potential difference between them). This means the large common-mode signals (within the op amp limits) may be handled at all gains. Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. These features explain the popularity of this type of instrumentation amplifier.

## "CLASSIC" THREE OP-AMP INSTRUMENTATION AMPLIFIER

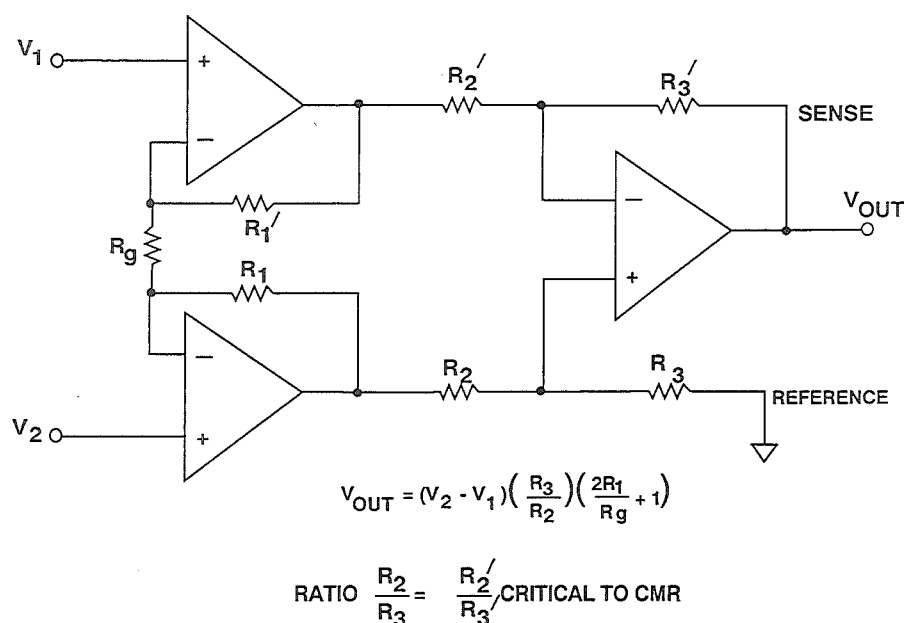


Figure 2.4

The classic three op amp configuration has been used in a number of monolithic IC instrumentation amplifiers. Besides offering excellent matching between the three internal op amps, thin-film laser trimmed resistors provide excellent

ratio matching and gain accuracy at much lower cost than using discrete op amps and resistor networks. The AD524 is an excellent example of monolithic in-amp technology, and a simplified schematic is shown in Figure 2.5.

## SIMPLIFIED SCHEMATIC OF THE AD524 IN-AMP

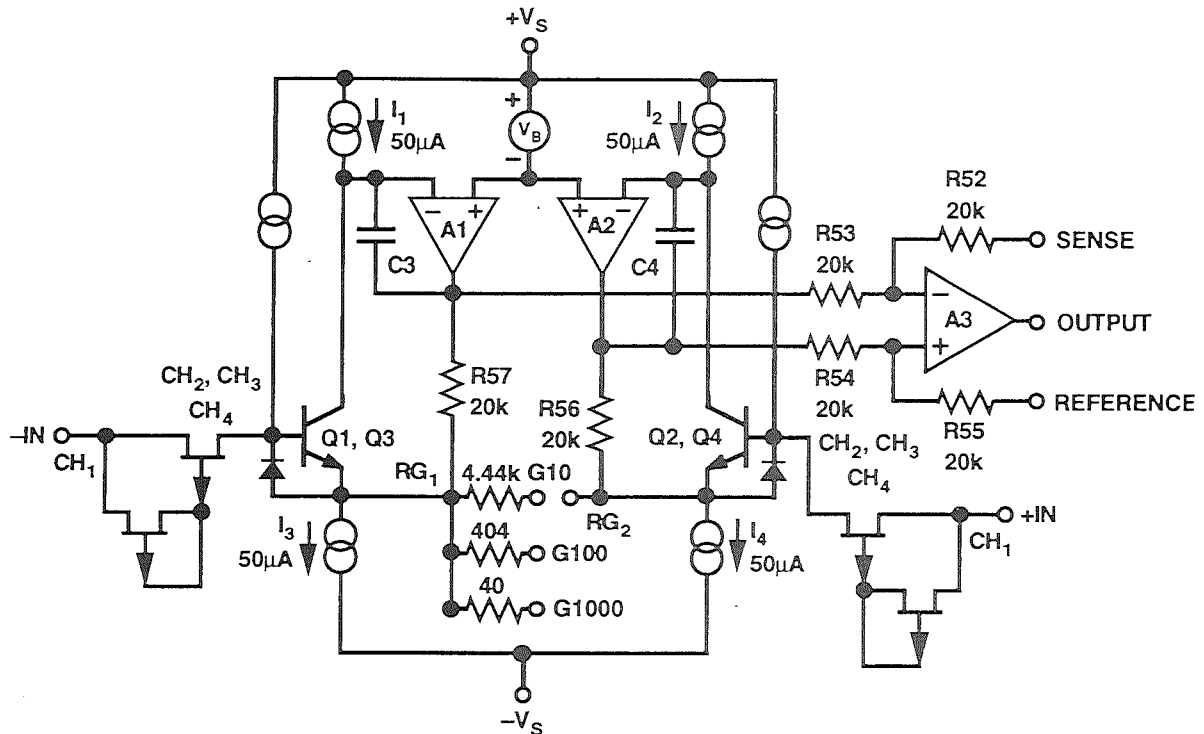


Figure 2.5

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of the full scale for the selected gain range. The same considerations discussed in Section 1 for op amps apply to in-amps. The manufacturer's "absolute maximum" input ratings for the device should be closely observed. As with op amps, many in-amps have absolute maximum input voltage specifications

equal to  $\pm V_S$ . Series resistors (for current limiting) and Schottky diode clamps may be used to prevent overload, if necessary. Some instrumentation amplifiers have built-in overload protection circuits in the form of series resistors (thin film) or series-protection FETs. In-amps such as the AMP-02 and the AD524 (see Figure 2.5) utilize series-protection FETs to minimize noise.

## INSTRUMENTATION AMPLIFIER INPUT OVERVOLTAGE CONSIDERATIONS

- Always observe absolute maximum data sheet specs!
- Schottky diode clamps to the supply rails will limit input to  $\pm V_S \pm 0.3V$  (This is not quite true, but near enough for safety)
- External resistors (or internal thin-film resistors) on inputs can limit input current.
- Some in-amps have series-protection input FETs for lower noise and higher input over voltages (up to  $\pm 60V$ , depending on device)

Figure 2.6

## Instrumentation Amplifier DC Error Sources

The DC and noise specifications for instrumentation amplifiers differ slightly from conventional op amps, so some discussion is required in order to fully understand the error sources.

The gain of an in-amp is set by a resistor. If the resistor is external to the in-amp (as for the AD620 shown in Figure 2.7), its value is either calculated from a formula or chosen from a table on the data sheet, depending on the desired

gain. In the case of the AD620, the internal resistors R1 and R2 are trimmed to an absolute value of  $24.7k\Omega$ . The gain formula is

$$G = \frac{49.4k\Omega}{R_g} + 1, \text{ and therefore}$$

$$R_g = \frac{49.4k\Omega}{G - 1}$$

## AD620 INSTRUMENTATION AMPLIFIER

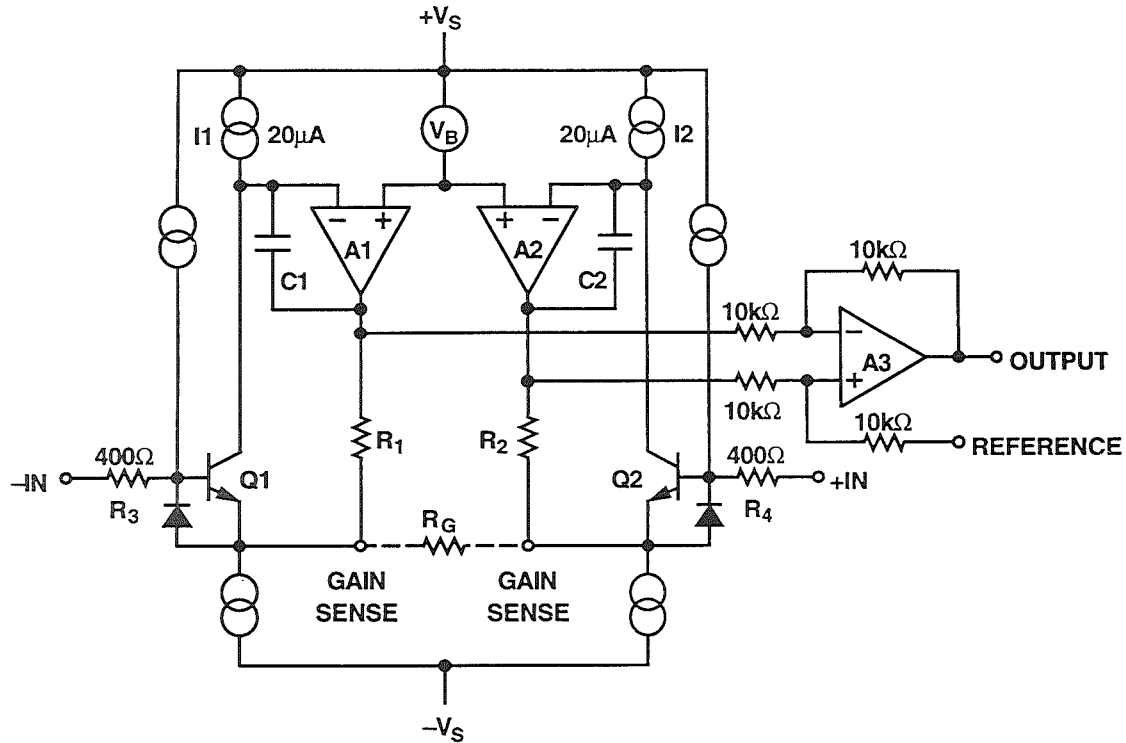


Figure 2.7

Absolute value laser wafer trimming allows the user to program gain accurately (to 0.15% at  $G=100$ ) with this single resistor. The absolute accuracy and temperature coefficient of this resistor directly affects the in-amp gain accuracy and drift. Gain accuracy and drift specifications for this type of in-amp assume a perfect external gain-setting resistor. Therefore, a low TC ( $<25\text{ppm}/^\circ\text{C}$ ) metal film resistor should be chosen, preferably with a 0.1% or better accuracy.

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many in-amps will work at higher gains, but the manufacturer will not guarantee a specific level of performance at these high gains. In practice, as the gain-setting resistor becomes smaller, any errors due to the resistance of the metal runs and bond wires become significant. These errors, along with an increase in

noise and drift, may make higher single-stage gains impractical.

In a pin-programmable in-amp such as the AD621, the gain setting resistors are internal, well matched, and the gain accuracy and gain drift specifications include their effects.

The *gain error* specification is the maximum deviation from the gain equation. Monolithic in-amps such as the AD624 have very low factory trimmed gain errors, with its maximum error of 0.05% at  $G = 1$  and 1% at  $G = 1000$  being typical for a high quality in-amp. Notice that the gain error increases with increasing gain. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of the external resistors and the temperature differences between individual resistors within the network all

contribute to the overall gain error. If the data is eventually digitized and presented to a digital processor, it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

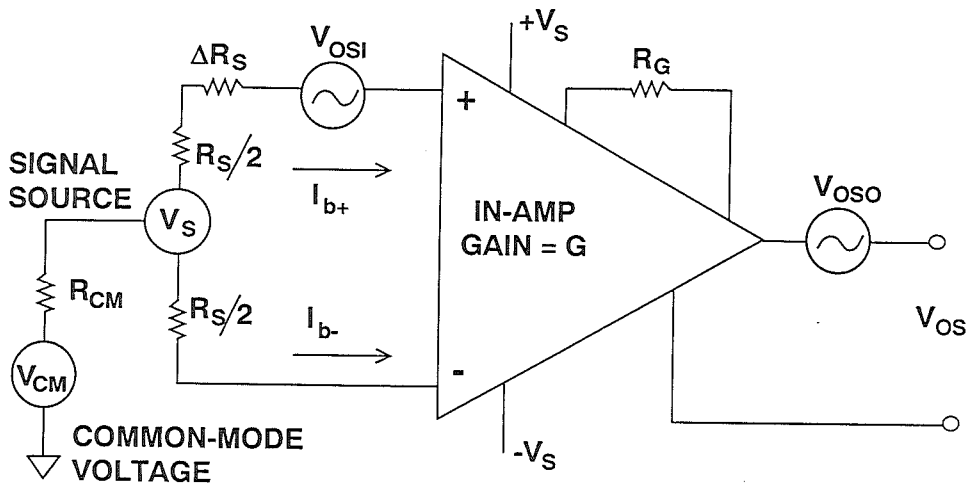
*Nonlinearity* is defined as the maximum deviation from a straight line on the plot of output versus input. The straight line is drawn between the end-points of the actual transfer function. Gain nonlinearity in a high quality in-amp is usually 0.01% or less, and is relatively insensitive to gain over the recommended gain range.

The total input offset voltage of an in-amp consists of two components (see Figure 2.8). Input offset voltage,  $V_{OSI}$ , is that component of input offset which is reflected to the output of the in-amp by the gain  $G$ . Output offset voltage,  $V_{OSO}$ , is independent of gain. At low gains, output offset voltage is dominant, while at high gains input offset dominates. The output offset voltage drift is nor-

mally specified as drift at  $G=1$  (where input effects are insignificant), while input offset voltage drift is given by a drift specification at a high gain (where output offset effects are negligible). The total output offset error, referred to the input (RTI), is equal to  $V_{OSI} + V_{OSO}/G$ . In-amp data sheets may specify  $V_{OSI}$  and  $V_{OSO}$  separately or give the total RTI input offset voltage for different values of gain.

Input bias currents also produce errors in in-amp circuits (see Figure 2.8). If the source resistance,  $R_S$ , is unbalanced by an amount,  $\Delta R_S$ , (often the case in bridge circuits), then there is an input offset voltage error due to the bias current equal to  $I_b \Delta R_S$  (assuming that  $I_{b+} \approx I_{b-} = I_b$ ). This error is reflected to the output, scaled by the gain  $G$ . The input offset current,  $I_{OS}$ , creates an input offset voltage error across the source resistance,  $R_S + \Delta R_S$ , equal to  $I_{OS}(R_S + \Delta R_S)$ , which is also reflected to the output by the gain,  $G$ .

### IN-AMP OFFSET VOLTAGE AND BIAS CURRENT MODEL



$$I_{OS} = |I_{b+} - I_{b-}|, V_{OS} = V_{OSO} + G \left[ V_{OSI} + I_b \Delta R_S + I_{OS} (R_S + \Delta R_S) \right]$$

Figure 2.8

In-amp common-mode error is a function of both gain and frequency as shown in Figure 2.9. It is customary to specify in-amp CMR for a 1k $\Omega$  source

impedance unbalance. The RTI error is obtained by dividing the common mode voltage,  $V_{cm}$ , by the common-mode rejection ratio, CMRR.

### COMMON-MODE REJECTION FOR THE AD620 INSTRUMENTATION AMPLIFIER, RTI, ZERO TO 1k $\Omega$ SOURCE IMBALANCE

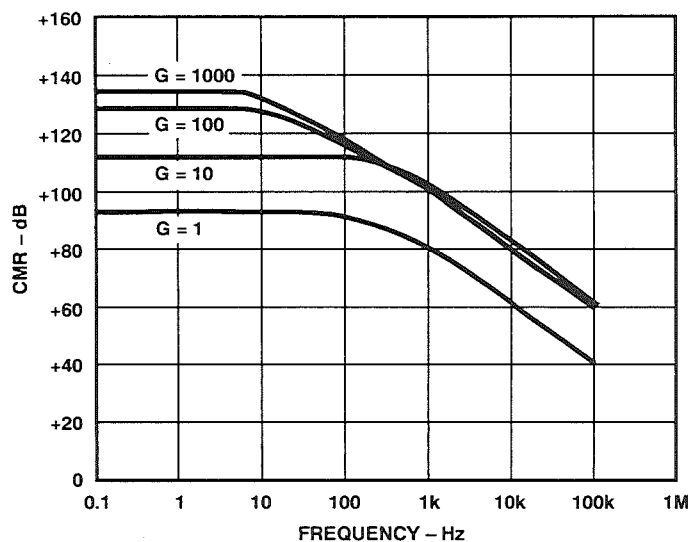


Figure 2.9

Power supply rejection (PSR) is also a function of gain and frequency (Figure 2.10). For in-amps, it is customary to specify the sensitivity to each power supply separately.

Now that all DC error sources have been accounted for, a worst case error budget can be calculated by reflecting all the sources to the in-amp input (Figure 2.11).

## POSITIVE AND NEGATIVE POWER SUPPLY REJECTION (PSR) FOR THE AD620 REFERRED TO INPUT

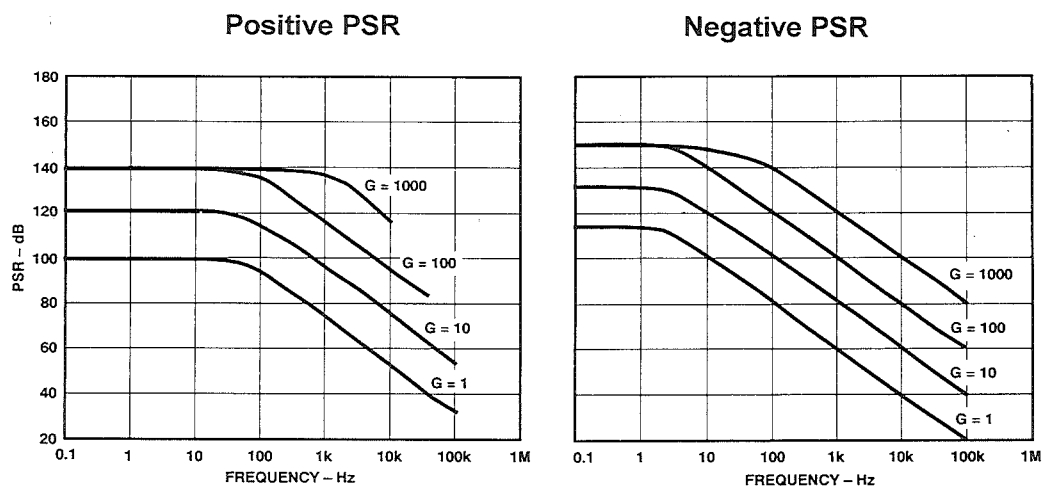


Figure 2.10

## INSTRUMENTATION AMPLIFIER DC ERRORS REFERRED TO THE INPUT

ERROR SOURCE	REFERRED TO INPUT (RTI) VALUE
Gain Accuracy (%)	Gain Accuracy $\times$ FS Input
Gain Nonlinearity (%)	Gain Nonlinearity $\times$ FS Input
Input Offset Voltage, $V_{osi}$	$V_{osi}$
Output Offset Voltage, $V_{oso}$	$V_{oso} / G$
Input Bias Current, $I_b$ Flowing in $\Delta R_s$	$I_b \Delta R_s$
Input Offset Current, $I_{os}$ Flowing in $R_s$	$I_{os} (R_s + \Delta R_s)$
Common Mode Input Voltage, $V_{cm}$	$V_{cm} / CMRR$
Power Supply Variation, $\Delta V_s$	$\Delta V_s / PSRR$

Figure 2.11

## Instrumentation Amplifier Noise Sources

Since in-amps are primarily used to amplify small precision signals, it is important to understand the effects of the associated noise sources. The in-amp noise model is shown in Figure 2.12. There are two sources of input voltage noise. The first is represented as a noise source,  $V_{ni}$ , in series with the input, as in a conventional op amp circuit. This noise is reflected to the output by the in-amp gain,  $G$ . The second noise source is the output noise,  $V_{no}$ , represented as a noise voltage in series with the in-amp output. The output noise is referred to the input by dividing by the gain,  $G$ .

There are four noise sources associated with the input noise currents  $I_{n+}$  and  $I_{n-}$ . Even though  $I_{n+}$  and  $I_{n-}$  are

usually equal ( $I_{n+} \approx I_{n-} = I_n$ ), they are uncorrelated, and therefore, the noise they each create must be summed in a root-sum-squares (RSS) fashion.  $I_{n+}$  flows through one half of  $R_s$ , and  $I_{n-}$  the other half. This generates two noise voltages, each having an amplitude,  $I_n R_s / 2$ . The third and fourth noise voltage is due to  $I_{n+}$  and  $I_{n-}$  flowing through the common-mode resistance,  $R_{cm}$ . There are two corresponding noise voltages generated, each having an amplitude of  $I_n R_{cm}$ . Each of these four noise sources is reflected to the output by the in-amp gain,  $G$ .

The total output noise,  $V_{on}$ , is calculated by combining all six noise sources in an RSS manner:

$$V_{on} = \sqrt{V_{no}^2 + G^2 \left( V_{ni}^2 + \frac{I_{n+}^2 R_s^2}{4} + \frac{I_{n-}^2 R_s^2}{4} + I_{n+}^2 R_{cm}^2 + I_{n-}^2 R_{cm}^2 \right)}$$

$$\text{Let } I_{n+} = I_{n-} = I_n,$$

$$V_{on} = \sqrt{V_{no}^2 + G^2 \left( V_{ni}^2 + \frac{I_n^2 R_s^2}{2} + 2I_n^2 R_{cm}^2 \right)}$$

The total noise, referred to the input (RTI) is simply the above expression divided by the in-amp gain,  $G$ .



# INSTRUMENTATION AMPLIFIER NOISE MODEL

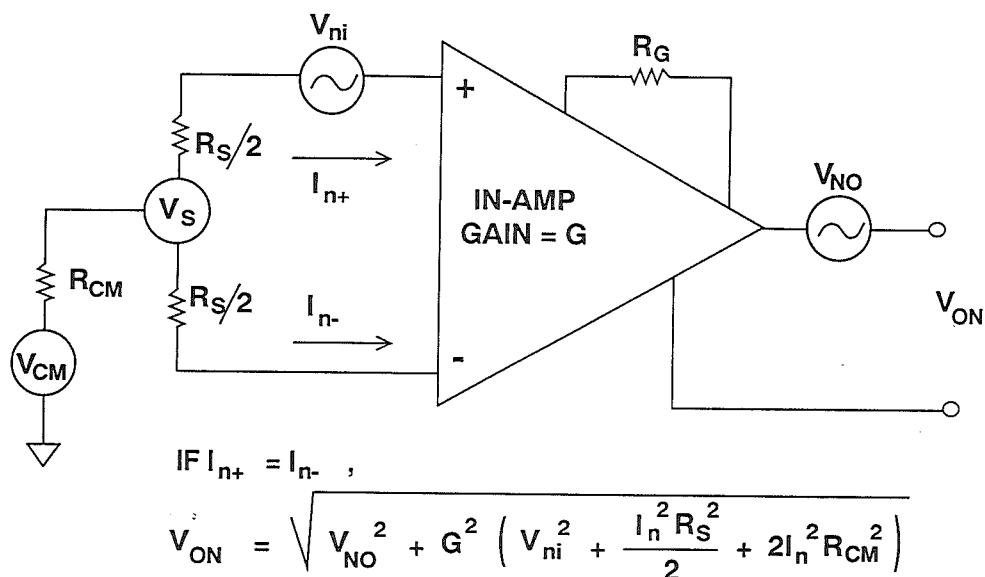


Figure 2.12

In-amp data sheets often present the total voltage noise RTI as a function of gain (Figure 2.13). This noise spectral density includes both the input ( $V_{ni}$ ) and output ( $V_{no}$ ) noise contributions. Figure 2.13 also shows the input current noise spectral density for the AD620. As in the case of op amps, the

total noise RTI must be integrated over the in-amp closed-loop bandwidth to compute the RMS value. The bandwidth may be determined from data sheet curves which show frequency response as a function of gain. Figure 2.14 shows such a curve for the AD620.

## AD620 IN-AMP INPUT VOLTAGE AND CURRENT NOISE

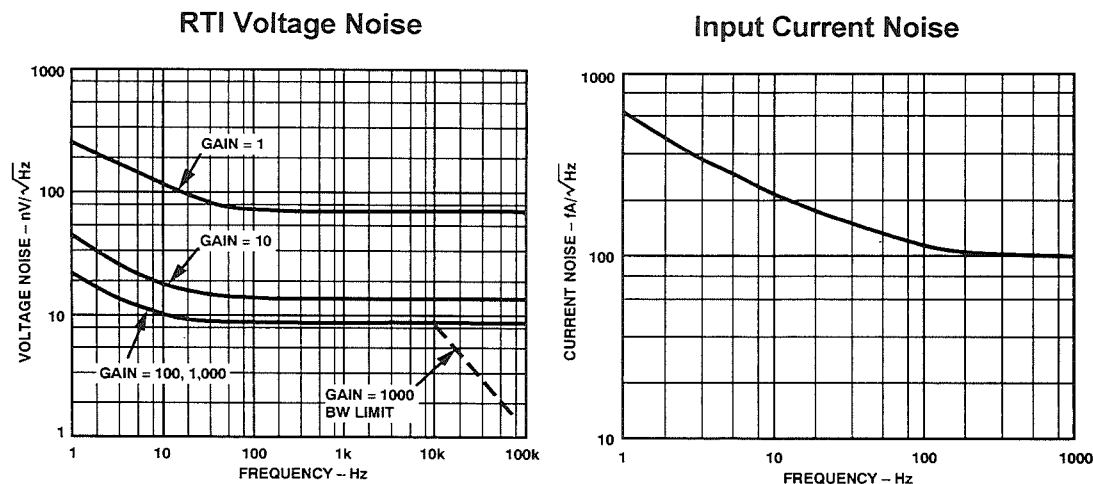


Figure 2.13

## AD620 IN-AMP FREQUENCY RESPONSE

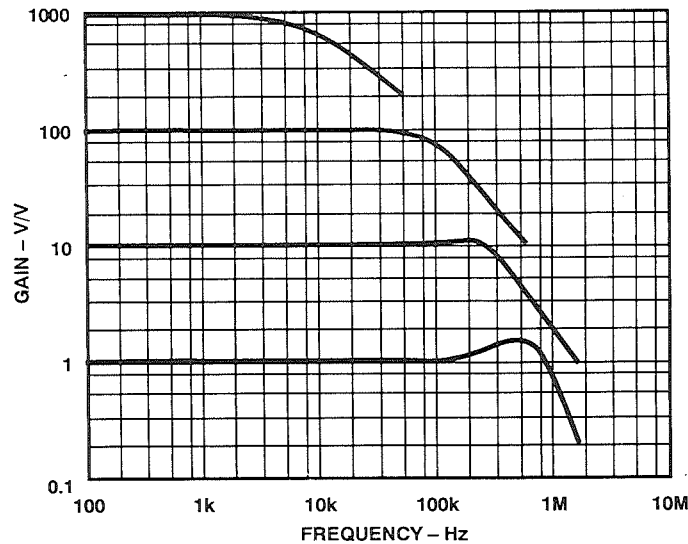


Figure 2.14

SUMMARY OF INSTRUMENTATION  
AMPLIFIER TYPICAL CHARACTERISTICS

- Balanced, High Impedance Inputs ( $>10^9\Omega$ )
- High Common Mode Rejection (CMR) : 70dB to  $>100\text{dB}$  @ 60Hz
- One Resistor Sets Gain (typically,  $G = 1$  to 10,000, 0.2% Accuracy )

External Resistor, User Selectable or

Pin-Programmable Internal Resistors

- Low Noise ( $<10\text{nV}/\sqrt{\text{Hz}}$  and  $100\text{fA}/\sqrt{\text{Hz}}$  @ 1kHz)
- Low Nonlinearity ( $< 0.01\%$ )
- Bandwidth: 500kHz to 1MHz
- Low Input Offset Voltage ( $100\mu\text{V}$ ) and Input Bias Current (1nA for Bipolar Input, 50pA for FET Input)

Figure 2.15

## ACTIVE FEEDBACK AMPLIFIERS

The AD830 represents Analog Devices' first amplifier product to embody a powerful new amplifier topology. Referred to as *active feedback*, the topology used in the AD830 provides inherent advantages in the handling of high-speed differential signals, differing system grounds, level shifting, and low distortion high frequency amplification. In addition, it makes possible the implementation of many functions not realizable with single op amp circuits, and is often superior to op amp based equivalent circuits. The AD830 is a versatile high-speed amplifier with excellent video performance, but it is not a general purpose in-amp with extremely low DC errors.

The AD830 topology, reduced to its elemental form, is shown in Figure 2.16. Nonideal effects such as nonlinearity, bias currents and limited input range are omitted from this model for simplicity. The key feature of this topology is the use of two, identical voltage-to-current converters,  $G_M$ , that make up input and feedback signal interfaces. They are labeled with inputs

$V_X$  and  $V_Y$ , respectively. These voltage-to-current converters' inputs are fully differential, highly linear, are high impedance, and have wide common-mode, small signal voltage ranges. The device can handle  $\pm 1V$  differential input signals in the linear mode. The inputs provide common-mode rejection, low distortion, and negligible loading on the source. The label,  $G_M$ , is meant to convey that the transconductance is a large signal quantity, unlike in the front end of most op amps which are not linear, except with minimal differential input. The two  $G_M$  stage current outputs,  $I_X$  and  $I_Y$ , sum together at the high impedance node, which is characterized by an equivalent resistance and capacitance connected to an "AC" ground. A unity voltage gain output stage follows the high impedance node to provide buffering. Relative to either input, the open loop gain,  $A_{OL}$ , is set by the transconductance,  $G_M$ , working into the resistance,  $R_p$ :  $A_{OL} = G_M \times R_p$ . The unity gain frequency,  $\omega_{odB}$ , for the open loop gain is established by the transconductance,  $G_M$ , working into the capacitance,  $C_C$ :  $\omega_{odB} = G_M / C_C$ .

### TOPOLOGY OF THE AD830 ACTIVE FEEDBACK AMPLIFIER

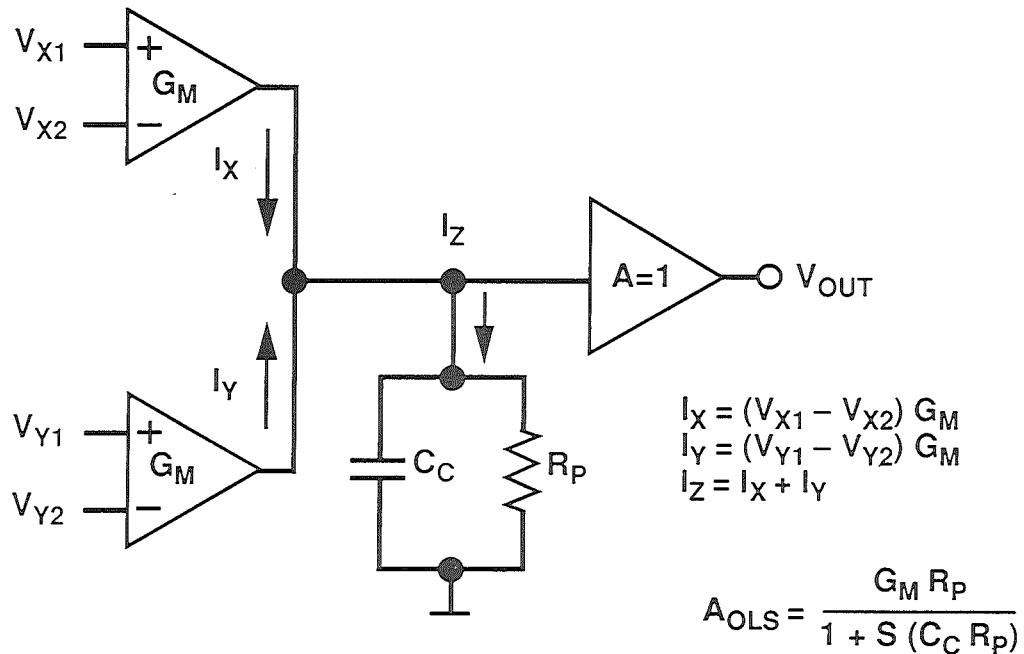


Figure 2.16

Precise amplification is accomplished through closed loop operation as shown in Figure 2.17. Voltage feedback is implemented via the Y  $G_M$  stage, where the output is connected to the  $-Y$  input for negative feedback. An input signal is applied across the X  $G_M$  stage, either fully differentially, or single-ended referred to common. It produces a current signal which is summed at the high impedance node with the output current from the Y  $G_M$  stage. Negative feedback nulls this sum to a small error current necessary to develop the output

voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y  $G_M$  output stage current to exactly equal the X  $G_M$  output current. Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input:  $V_Y = -V_X$ , or more precisely,  $V_{Y2} - V_{Y1} = V_{X1} - V_{X2}$ . This simple relationship provides the basis to analyze any function possible with the AD830, including any feedback situation.

# CLOSED LOOP CONNECTION FOR THE AD830 ACTIVE FEEDBACK TOPOLOGY

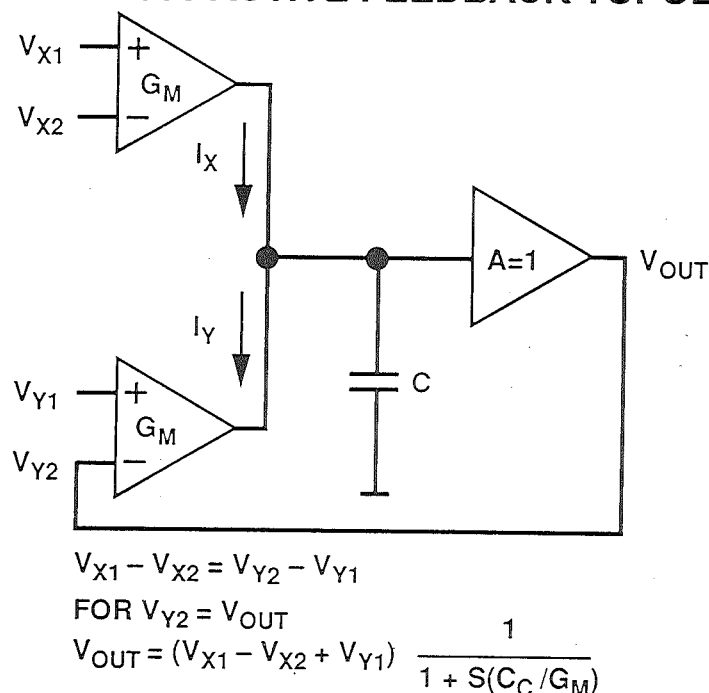


Figure 2.17

The bandwidth of the circuit is defined by the  $G_M$  and the capacitor,  $C_C$ . The highly linear  $G_M$  stages give the amplifier a single-pole response, excluding the output amplifier and loading effects. The bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830. In addition, the input impedance and CMRR are the same for either connection. This is very advantageous, and unlike the situation with a voltage or current feedback amplifier, where there is a distinct difference in performance between the inverting and noninverting gain stages. The practical importance of this cannot be overemphasized and is a key feature offered by the AD830 active feedback topology.

The AD830 is a flexible device which may be used in a number of configurations with excellent video performance. Figure 2.18 shows how the AD830 may be configured as an instrumentation amplifier. The input signal is connected differentially to the internal V-to-I converter #1. The gain is set via the feedback resistors,  $R_2$  and  $R_1$ , in the same manner as a noninverting op amp circuit. The polarity of the gain is established by the relative connections at input pins 1 and 2. Inverting gain is set by reversing the connections. As in a conventional voltage feedback op amp, the bandwidth decreases with increasing gain.

## GAIN-OF-N INSTRUMENTATION AMPLIFIER USING THE AD830

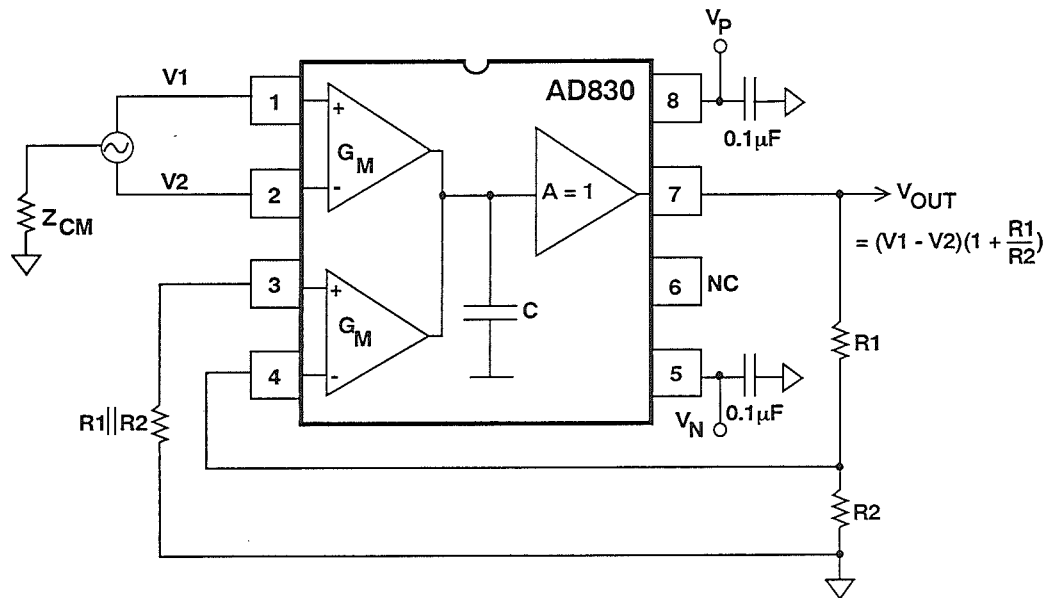


Figure 2.18

The video cable receiver/driver circuit shown in Figure 2.19 not only provides ground noise rejection, but also supplies a gain-of-two so that the AD830 output can drive a source and load terminated 75Ω cable without signal attenuation. The 499Ω resistors set the gain at 2, and the 249Ω resistor between pin 3

and ground cancels the offset due to the input bias currents. The signal from system "A" is received differentially by the AD830 and is reproduced relative to the ground in system "B". Common mode noise is rejected by the excellent CMRR of the AD830 (50dB at 10MHz).

## VIDEO CABLE RECEIVER/DRIVER USING THE AD830

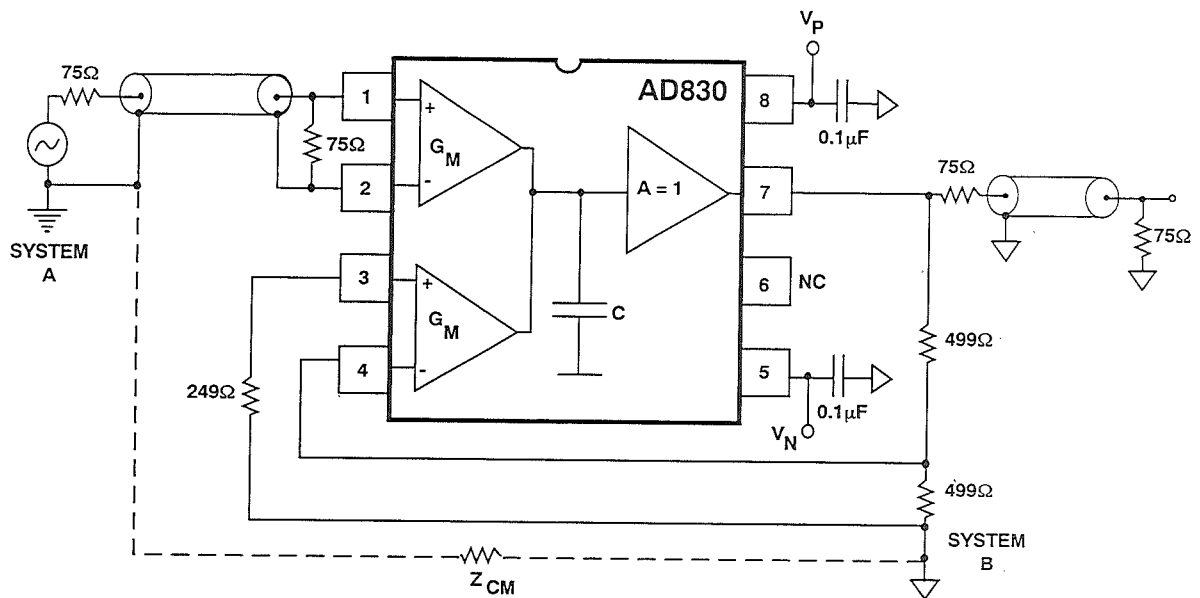


Figure 2.19

The video loop-through connection is a popular method of connecting several different pieces of equipment. High input impedance differential amplifiers connect to taps along the distribution cable. The cable is terminated in its characteristic impedance at the source and at the far end. The AD830 makes an ideal choice for this loop-through

amplifier because of its high input impedance and good common mode rejection at high frequencies. The high input impedance provides negligible loading on the cable. More significantly, the benign loading is maintained while the AD830 is powered down. Figure 2.20 shows a typical loop-through connection using the AD830.

## VIDEO LOOP-THROUGH CONNECTION USING THE AD830

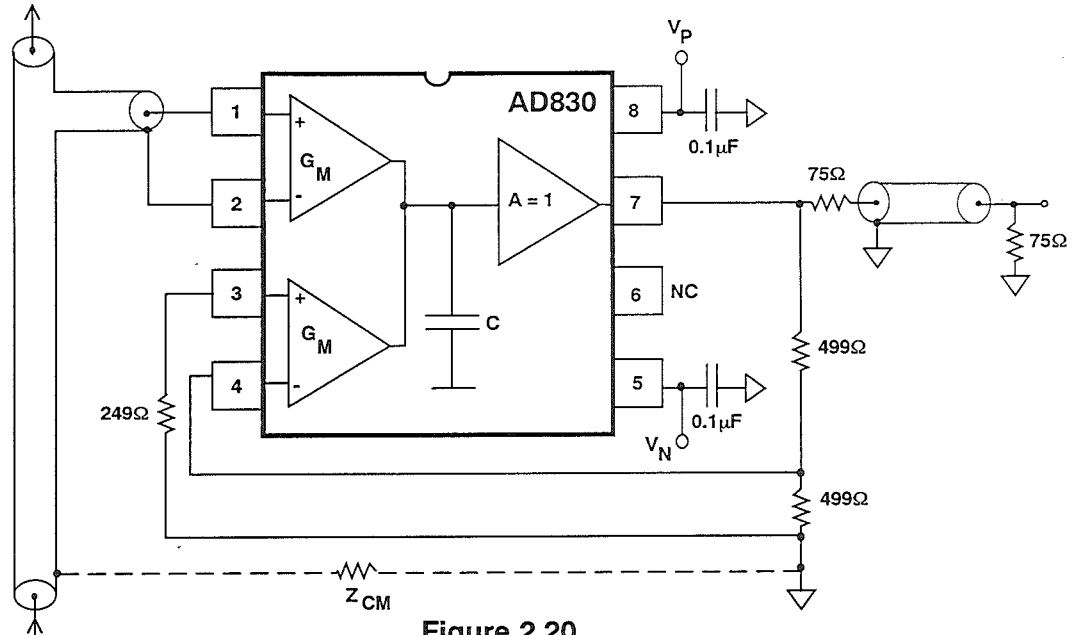


Figure 2.20

Key specifications for the AD830 are shown in Figure 2.21. CMRR and

frequency response are shown in Figure 2.22.

### AD830 ACTIVE FEEDBACK VIDEO DIFFERENCE AMPLIFIER KEY SPECIFICATIONS

- Common Mode Voltage Range:  $\pm 11.5V$  (for  $V_{SY} = \pm 15V$ )
- Differential Voltage Range:  $\pm 2V$
- CMRR: 60dB @ 4.43MHz, 50dB @ 10MHz
- Bandwidth: 50MHz
- Distortion: -60dBc @ 4.43Mhz
- Differential Gain: 0.1%, Differential Phase:  $0.1^\circ$

Figure 2.21



## AD830 CMR AND FREQUENCY RESPONSE (G = 1) FOR $\pm 5V$ AND $\pm 15V$ SUPPLIES

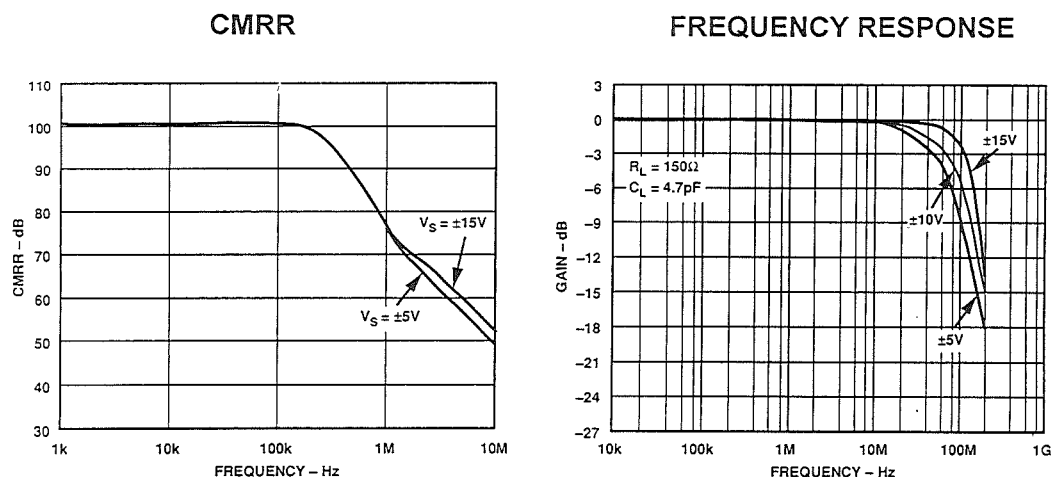


Figure 2.22

## PROGRAMMABLE GAIN AMPLIFIERS

Most systems with wide dynamic range need some method of adjusting the input signal level to the analog-to-digital-converter (ADC). The ADC compares the input signal to a fixed voltage reference ( $+5V$  or  $+10V$  are typical values). To achieve the rated precision of the converter, the maximum input should be fairly near its full scale voltage. However, transducers have a wide range of output voltages. High gain is needed for a small sensor

voltage, but with a large transducer output, a high gain will cause the amplifier or ADC to saturate. So some type of controllable gain device is needed. Such a device has a gain that is controlled by a DC voltage or, more commonly, a digital input. This device is known as a *programmable gain amplifier*, or PGA. Programmable gain amplifiers have a variety of applications, and Figure 2.23 lists some of them.

## PGA APPLICATIONS

- Instrumentation
- Photodiode Circuits
- Ultrasound Preamplifiers
- Sonar
- Wide Dynamic Range Sensors
- Driving ADCs
- Automatic Gain Control (AGC) Loops

Figure 2.23

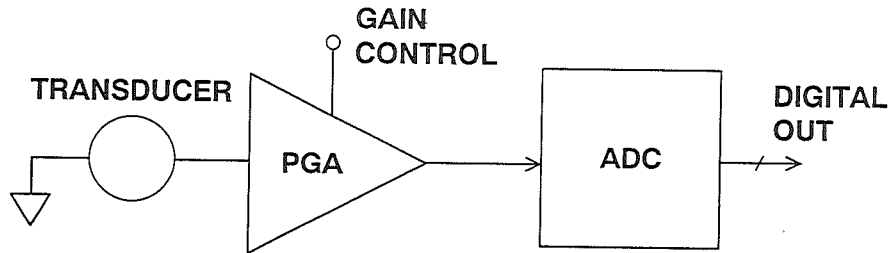
A PGA is usually located between a sensor and its ADC. Additional signal conditioning may take place before or after the PGA, depending on the application. For example, a photodiode needs a current to voltage converter between it and the PGA. In most other systems, it is better to place the gain first, and condition a larger signal. This reduces errors introduced by the signal conditioning circuitry.

To understand the benefits of variable gain, assume an ideal PGA with two settings, gains of one and two. The dynamic range of the system is in-

creased by 6dB. Increasing the gain to four results in a 12dB increase in dynamic range.

If the LSB of an ADC is equivalent to 10mV of input voltage, the ADC cannot resolve smaller signals, but when the gain of the PGA is increased to two, input signals of 5mV may be resolved. Thus, the processor can combine PGA gain information with the digital output of the ADC to increase its resolution by one bit. Essentially, this is the same as adding additional resolution to the ADC.

## PROGRAMMABLE GAIN AMPLIFIERS (PGAs)



- Used to Increase Dynamic Range of Circuit
- A PGA With a Gain From 1 To 2 Theoretically Increases the Dynamic Range by 6dB, A Gain of 1 To 4 Gives 12dB Increase, etc.

Figure 2.24

In practice, PGAs are not ideal, and their error sources must be studied. The most fundamental problem with PGA design is accurate gain programming. Electromechanical relays have minimal  $R_{ON}$ , but are otherwise unsuitable for gain switching. They are slow, large,

and expensive. Silicon switches, as discussed in the section on switches and multiplexers (Section 8 of this book), have quite large  $R_{ON}$ , which is both voltage- and temperature-variable, and stray capacities, which may affect the AC parameters of a PGA using them.

## PGA DESIGN ISSUES

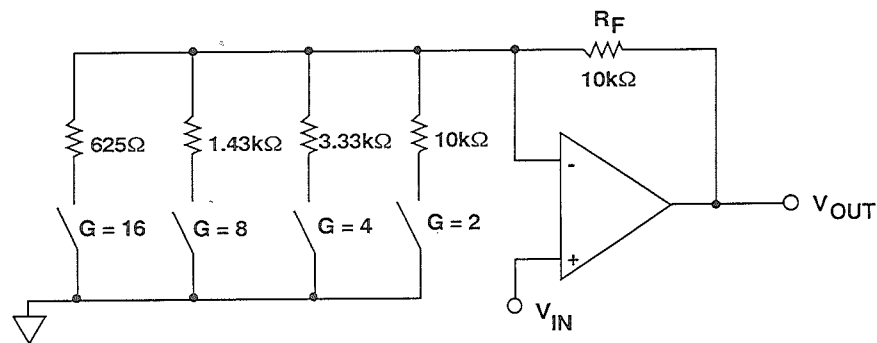
- How to Switch the Gain
- Effects of Switch On-Resistance
- Gain Accuracy
- Gain Linearity
- Bandwidth versus Frequency versus Gain
- Offset
- Temperature Effects on Gain and Offset
- Settling Time After Switching

Figure 2.25

To understand how  $R_{ON}$  can affect the performance of a PGA, let us consider a poor PGA design (Figure 2.26). An op amp is configured in the standard non-inverting gain circuit with 4 different gain setting resistors, each grounded by a switch. Most silicon switches have ON resistance in the range of  $100\Omega$ - $500\Omega$ . Even if the ON resistance were as low as  $25\Omega$ , the error for a gain of 16 would

be 2.4%, much worse than 8-bits. Furthermore,  $R_{ON}$  drifts over temperature, and varies from switch to switch. If the value of the feedback and gain setting resistors were increased, noise and offset would become a problem. The only way to achieve accuracy with this circuit is to replace silicon switches with relays which have virtually no ON resistance.

### HOW NOT TO BUILD A PGA



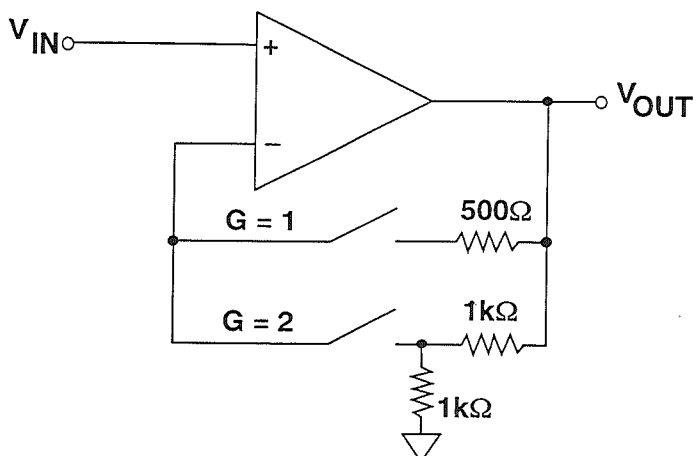
- Gain Accuracy Limited by Switch's On Resistance,  $R_{ON}$  and  $R_{ON}$  Modulation
- $R_{ON}$  Typically 100 - 500 $\Omega$  for a CMOS Or JFET Switch
- Even With  $R_{ON} = 25\Omega$ , There is a 2.4% Gain Error for  $A_V = 16$
- $R_{ON}$  Drift Over Temperature Limits Accuracy
- Only Solution is to Use Very Low  $R_{ON}$  Switches (Relays)

Figure 2.26

It is better to use a circuit where  $R_{ON}$  is unimportant. In Figure 2.27, the switch is placed in series with the inverting input of an op amp. Since the input impedance of an op amp is very

large, the  $R_{ON}$  of the switch is irrelevant. The gain is now determined by the external resistors. The  $R_{ON}$  may add a small offset error if the op amp bias current is significant.

## ALTERNATE CONFIGURATION MAKES THE EFFECTS OF $R_{on}$ NEGLIGIBLE



- $R_{on}$  is Not in Series With Gain Setting Resistors
- $R_{on}$  is Very Small Compared to Input Impedance
- Only a Slight Offset Error Occurs Due to the Bias Current Flowing Through the Switch

Figure 2.27

The AD526 amplifier uses this method of building a PGA and integrates it onto a single chip. The AD526 has 5 binary gain settings from 1 to 16, and its internal JFET switches are connected to the inverting input of the amplifier.

The gain resistors are laser trimmed. The maximum gain error is only 0.02%, far better than the 2.4% error in Figure 2.26. The linearity is also very good at 0.001%. The AD526 is controlled by a latched digital interface.

## AD526 MONOLITHIC SOFTWARE PROGRAMMABLE PGA

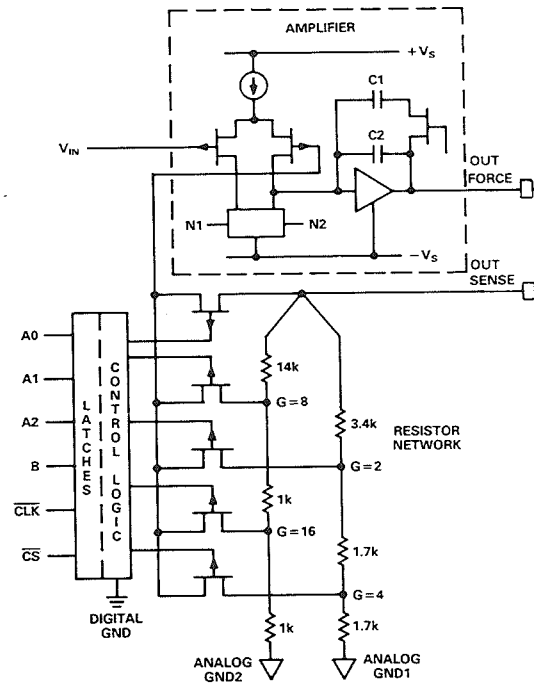


Figure 2.28

## AD526 SOFTWARE PROGRAMMABLE PGA KEY FEATURES

- Software Programmable Binary Gains From 1 to 16
- Low Bias Current JFET Input Stage
- Worst Case Gain Error is 0.02% (12 Bit Performance)
- Gain Nonlinearity is 0.001% Maximum
- Latched TTL Compatible Control Inputs

Figure 2.29

This same design can be used to build the discrete PGA shown in Figure 2.30. It uses a single op amp, a quad switch, and precision resistors. The low-noise AD797 replaces the JFET input op amp of the AD526, but almost any voltage feedback op amp could be used in this circuit. The ADG412 was picked for its low ON resistance of  $35\Omega$ .

The resistors were chosen to give gains of 1, 10, 100 and 1000, but if other gains are required, the resistor values may easily be altered. Ideally, a trimmed resistor network should be used both for initial gain accuracy and

for low drift over temperature. The 20pF capacitor ensures stability and holds the output voltage when the gain is switched. The control signal to the switches turns one switch off a few nanoseconds before the second switch turns on. During this break, the op amp is open-loop. If the capacitor was not used, the output would start slewing. Instead, the capacitor holds the output voltage during the switching. Since the time that both switches are open is very short, only 20pF is needed. For slower switches, a larger capacitor may be necessary.

### A VERY LOW NOISE PGA USING THE AD797 AND THE ADG412

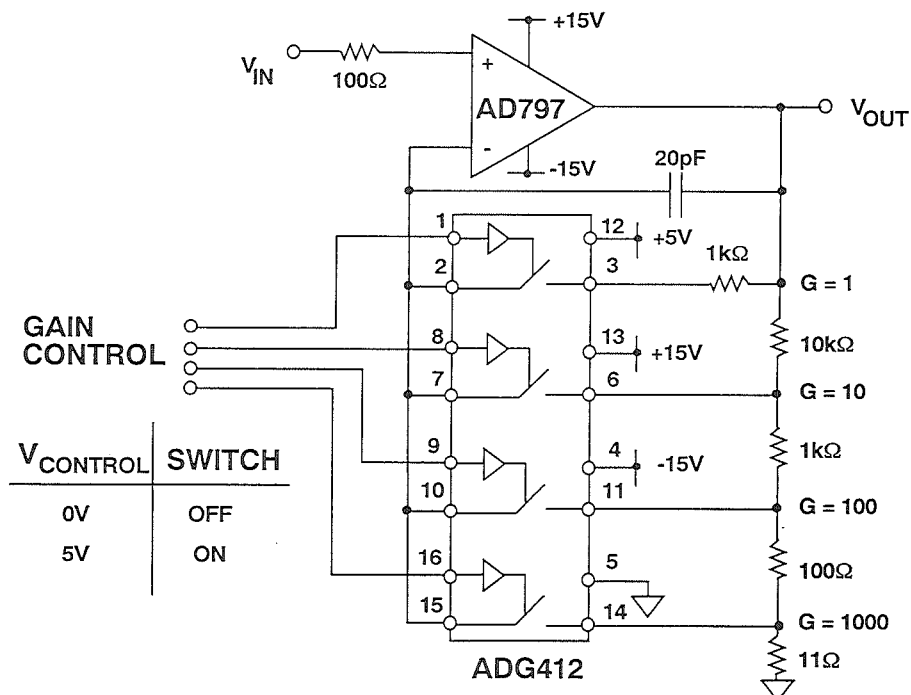


Figure 2.30

The PGA's input voltage noise spectral density is only  $1.65\text{nV}/\sqrt{\text{Hz}}$  at  $1\text{kHz}$ , only slightly higher than the noise performance of the AD797 alone. The increase is due to the noise of the ADG412, and the current noise of the AD797 flowing through the  $R_{\text{ON}}$  resistance. The noise was measured at a gain of 1000.

The accuracy of the PGA is important in determining the overall accuracy of a system. The AD797 has a bias current of  $0.9\mu\text{A}$ , which, flowing in  $35\Omega$   $R_{\text{ON}}$ , results in an additional offset error of  $31.5\mu\text{V}$  (Figure 2.31). Combined with the AD797 offset, the total  $V_{\text{OS}}$  becomes

$71.5\mu\text{V}$  (max). Offset temperature drift is affected by the change in bias current and  $R_{\text{ON}}$  resistance. Calculations show that the total temperature coefficient increases from  $0.6\mu\text{V}/^\circ\text{C}$  to  $1.6\mu\text{V}/^\circ\text{C}$ . These errors are small, and may not matter, but it is important to be aware of them. In practice, circuit accuracy and TC will be determined by the external resistors. Input characteristics such as common mode range and input bias current are determined solely by the AD797. The circuit could be converted to single supply simply by changing the op amp. The switches do not need to be changed.

## AD797 PGA ACCURACY

### ■ $R_{\text{ON}}$ Adds Additional Input Offset And Drift:

$$\Delta V_{\text{OS}} = I_{\text{b}} R_{\text{ON}} = (0.9\mu\text{A})(35\Omega) = 31.5\mu\text{V} \text{ (max)}$$

$$\text{Total } V_{\text{OS}} = 40\mu\text{V} + 31.5\mu\text{V} = 71.5\mu\text{V} \text{ (max)}$$

(Note:  $40\mu\text{V}$  is Due To The AD797B)

### ■ Temperature Drift Due To $R_{\text{ON}}$ :

$$\text{At } +85^\circ\text{C}, \Delta V_{\text{OS}} = (2\mu\text{A})(45\Omega) = 90\mu\text{V} \text{ (max)}, \text{TC} = 1\mu\text{V}/^\circ\text{C}$$

### ■ Temperature Coefficient Total:

$$\Delta V_{\text{OS}} / \Delta T = 0.6\mu\text{V}/^\circ\text{C} + 1.0\mu\text{V}/^\circ\text{C} = 1.6\mu\text{V}/^\circ\text{C} \text{ (max)}$$

(Note:  $0.6\mu\text{V}/^\circ\text{C}$  is due to the AD797B)

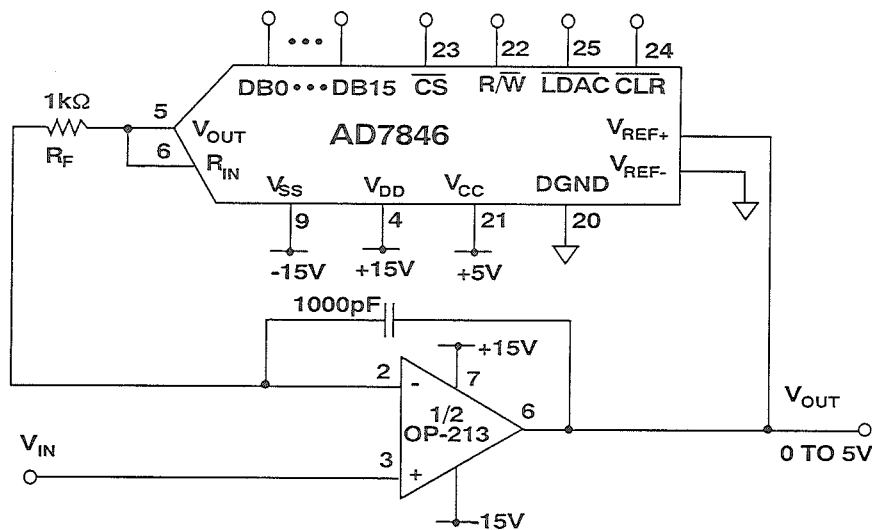
Figure 2.31



Another PGA configuration uses a DAC in the feedback loop of an op amp to adjust the gain under digital control (Figure 2.32). The digital code of the DAC controls its attenuation. Attenuating the feedback signal increases the closed-loop gain. A non-inverting PGA of this type requires a multiplying DAC with a voltage output (a multiplying DAC is a DAC with a wide reference voltage range *which includes zero*). For most applications of the PGA, the reference input must be capable of

handling bipolar signals. The AD7846 is a 16-bit converter that meets these requirements. In this application, it is used in standard 2-quadrant multiplying mode. The OP-213 is a low drift, low noise amplifier, but the choice of amplifier is flexible, and depends on the application. The input voltage range depends on the output swing of the AD7846, which is 3V less than the positive supply, and 4V above the negative supply. A 1000pF capacitor is used in the feedback loop for stability.

### ACCURATE BINARY GAIN PGA USES DAC IN OP-AMP FEEDBACK LOOP



■ Multiplying DAC in Feedback Loop Adjusts Gain

$$G = \frac{2^{16}}{\text{Decimal Value of Digital Code}}$$

Figure 2.32

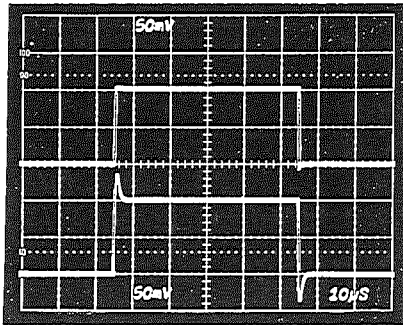
The gain of the circuit is set by adjusting the digital inputs of the DAC, according to the equation given in Figure 2.32. D0-15 represents the decimal value of the digital code. For example, if all the bits were set high, the gain would be  $65,536/65,535 = 1.000015$ . If the 8 least significant bits are set high and the rest low, the gain would be  $65,536/255 = 257$ .

square wave input. The bandwidth is a fairly high 4MHz. However, this does reduce with gain, and for a gain of 256, the bandwidth is only 600Hz. If the gain-bandwidth product were constant, the bandwidth in a gain of 256 should be 15.6kHz; but the internal capacitance of the DAC reduces the bandwidth to 600Hz.

Figure 2.33 shows the small signal response at a gain of 1 with a 100mV

## BINARY GAIN PGA PERFORMANCE

## SMALL SIGNAL RESPONSE



Top Trace: Input, 50mV/div.  
 Bottom Trace: Output, 50mV/div.  
 Horizontal Scale: 10µs/div.

Bandwidth ( $G=+1$ ) = 4MHz

Bandwidth ( $G=+256$ ) = 600Hz

Nonlinearity ( $G=+1$ ) = 0.001%

Offset = 100µV

Noise = 50nV/√Hz

Gain Accuracy ( $G=+1$ ) = 0.003%

Gain Accuracy ( $G=+256$ ) = 0.1%

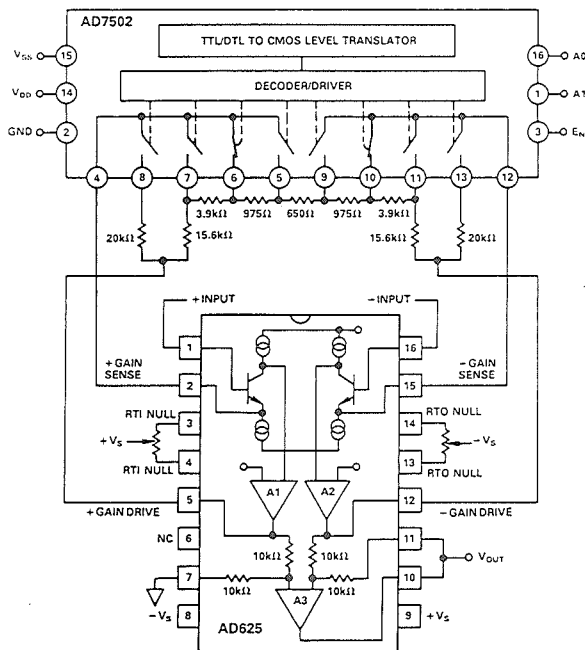
Figure 2.33

The gain accuracy of the circuit is determined by the resolution of the DAC and the gain setting. At a gain of 1, all bits are on, and the accuracy is determined by the DNL specification of the DAC, which is  $\pm 1$  LSB maximum. Thus, the gain accuracy is equivalent to 1LSB in a 16-bit system, or 0.003%. However, as the gain is increased, fewer of the bits are on. For a gain of 256, only bit 8 is turned on. The gain accuracy is still dependent on the  $\pm 1$  LSB of DNL, but now that is compared to only the lowest 8 bits. Thus, the gain accuracy is reduced to 1 LSB in a 8-bit system, or 0.4%. If the gain is increased above 256, the gain accuracy is reduced further. The designer must determine

an acceptable level of accuracy. In this particular circuit, the gain was limited to 256.

There are often applications where a PGA with differential inputs is needed, instead of the single ended types discussed so far. The AD625 combines an instrumentation amplifier topology with gain switching capabilities to accomplish 12-bit gain accuracy (Figure 2.34). An external switch is needed to switch between different gain settings. In the example shown, resistors were chosen for gains of 1, 4, 16, and 64. Other features of the AD625 are 0.001% nonlinearity, wide bandwidth, and very low input noise.

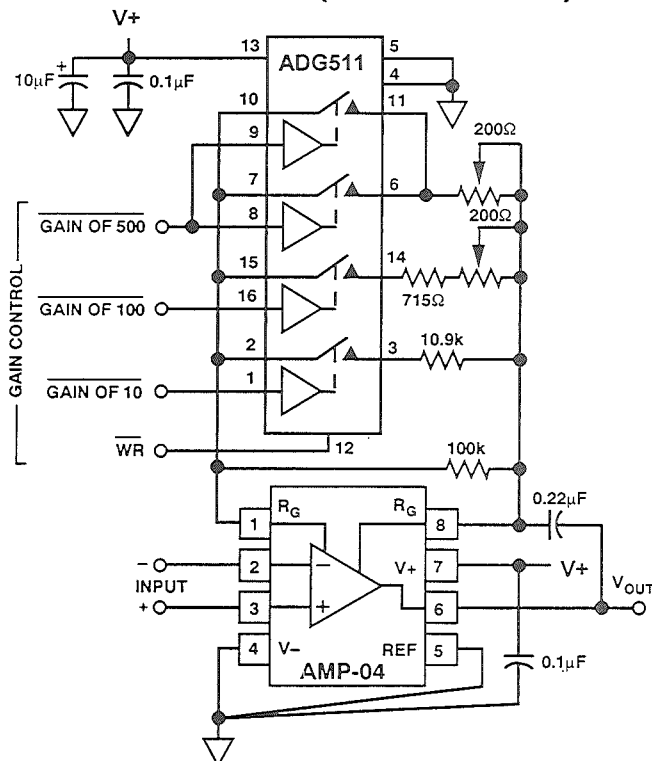
## A SOFTWARE PROGRAMMABLE GAIN AMPLIFIER



- $G = 1, 4, 16, 64$
- Differential Input Stage
- 12 Bit Gain Accuracy
- Nonlinearity =  $\pm 0.001\%$  ( $G = 1$  to 256)
- Low Noise: 4nV/ $\sqrt{\text{Hz}}$
- 25MHz Gain-Bandwidth Product

Figure 2.34

## SINGLE SUPPLY (+5V TO +10V) INSTRUMENTATION PGA



- $G = 100\text{k}\Omega/\text{R}_G$
- R<sub>G</sub> Is a Combination of Switch R<sub>ON</sub> and the External Resistor
- Trim Required at High G Due to Uncertainty Of R<sub>ON</sub>
- Relays Can Be Used to Avoid Trim

Figure 2.35

Non-inverting PGA circuits using an op amp are easily adaptable to single supply operation, but the instrumentation amplifier topology does not lend itself to single supply applications. However, the AMP-04 can be used with an external switch to produce the single supply instrumentation PGA shown in Figure 2.35. This circuit has selectable gains of 1, 10, 100, and 500, which are controlled by an ADG511. The ADG511 was chosen as a single supply switch with a low  $R_{ON}$  of  $45\Omega$ . The gain of this circuit is dependent on the  $R_{ON}$  of the switches. Trimming is required at the higher gains to achieve accuracy. At a gain of 500, two switches are used in parallel, but their resistance causes a 10% gain error in the absence of adjustment.

Certain ADCs (AD7710, AD7711, AD7712, AD7713) have built in PGAs. Circuit design is much easier because an external PGA and its control logic are not needed. Furthermore, all the errors of the PGA are included in the specifications of the ADC, making error calculations simple. The PGA gain is controlled over the same serial interface as the ADC, and the gain setting is factored into the conversion, saving additional calculations to determine input voltage. This combination of ADC and PGA is very powerful and enables the realization of a highly accurate system, with a minimum of circuit design.

### THE AD7710 ADC HAS A BUILT-IN PGA WITH GAIN CONTROLLED BY A SERIAL INTERFACE

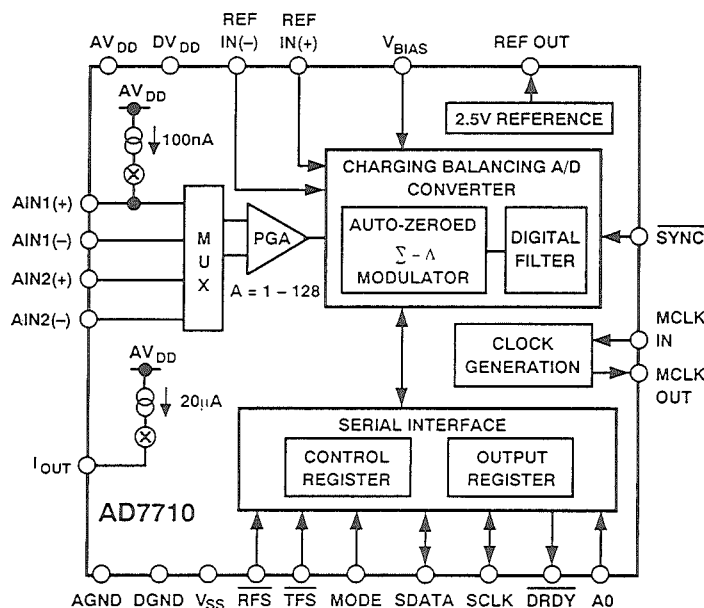


Figure 2.36

## ISOLATION AMPLIFIERS

There are many applications where it is desirable, or even essential, for a transducer to have no direct ("galvanic") electrical connection with the system to which it is supplying data, either in order to avoid the possibility of dangerous voltages or currents from one half of the system doing damage in the other, or to break an intractable ground loop. Such a system is said to be "isolated", and the arrangement which passes a signal without galvanic connections is known as an "isolation barrier".

The protection of an isolation barrier works in both directions, and may be needed in either, or even in both. The obvious application is where a sensor may accidentally encounter high volt-

ages, and the system it is driving must be protected. It is equally possible that a sensor may need to be isolated from accidental high voltages arising downstream, in order to protect its environment: examples include the need to prevent the ignition of explosive gases by sparks at sensors and the protection from electric shock of patients whose ECG, EEG or EMG is being monitored. The ECG case is interesting, as protection may be required in *both* directions: the patient must be protected from accidental electric shock, but if the patient's heart should stop, the ECG machine must be protected from the very high voltages (>7.5 kV) applied to the patient by the defibrillator which will be used to attempt to restart it.

### WHERE IS ISOLATION USED?

- Transducer is at a High Potential Relative to other Circuitry (or may become so under fault conditions)
- Transducer may not Carry Dangerous Voltages, Irrespective of Faults in other Circuitry (e.g. Patient Monitoring and Intrinsically Safe Equipment for use with Explosive Gases)
- To Break Ground Loops

Figure 2.37

Just as interference, or *unwanted* information, may be coupled by electric or magnetic fields, or by electro-magnetic radiation, these phenomena may be used for the transmission of *wanted* information in the design of isolated systems. The most common isolation amplifiers use transformers, which exploit magnetic fields, and another common type uses small high voltage capacitors, exploiting electric fields.

Opto-isolators, which consist of an LED and a photocell, provide isolation by using light, a form of electro-magnetic radiation. Different isolators have differing performance: some are sufficiently linear to pass high accuracy analog signals across an isolation barrier, with others the signal may need to be converted to digital form before transmission, if accuracy is to be maintained.

## TECHNIQUES FOR ISOLATION

- Electric Field → Capacitive Signal Coupling
- Magnetic Field → Transformer Coupling
- Electromagnetic → Optical Coupling
- Sometimes a Technique will not have Adequate Linearity--  
In Such Cases There are two Possibilities:
  - ◆ Voltage-Frequency Conversion / Transmission /  
Frequency-Voltage Conversion
  - ◆ Analog-Digital Conversion Before Transmission  
Across the Isolation Barrier

Figure 2.38

Transformers are capable of analog accuracy of 12-16 bits and bandwidths up to several hundred kHz, but their maximum voltage rating rarely exceeds 10kV, and is often much lower. Capacitively coupled isolation amplifiers have lower accuracy, perhaps 12-bits maximum, lower bandwidth, and lower voltage ratings - but they are cheap. Optical isolators are fast and cheap,

and can be made with very high voltage ratings (although 4 - 7kV is one of the more common ratings), but they have poor linearity, and are not usually suitable for direct coupling of precision analog signals

Linearity and isolation voltage are not the only issues to be considered in the choice of isolation systems. Power is

essential. Both the input and the output circuitry must be powered, and unless there is a battery on the isolated side of the isolation barrier (which is possible, but rarely convenient), some form of isolated power must be provided. Systems using transformer isolation can easily use a transformer (either the signal transformer or another one) to provide isolated power, but it is impractical to transmit useful amounts of power by capacitive or optical means. Systems using these forms of isolation must make other arrangements to obtain isolated power supplies - this is a powerful consideration in favor of choosing transformer isolated isolation amplifiers: they almost invariably include an isolated power supply.

The isolation amplifier has an input circuit that is galvanically isolated from the power supply and the output circuit. In addition, there is minimal capacitance between the input and the rest of the device. Therefore, there is no possibility for DC current flow, and minimum AC coupling. Isolation amplifiers are intended for applications requiring safe, accurate measurement of low frequency voltage or current (up to about 100kHz) in the presence of high common-mode voltage (to thousands of volts) with high common mode rejection. They are also useful for line-receiving of signals transmitted at high impedance in noisy environments, and for safety in general-purpose measure-

ments, where DC and line-frequency leakage must be maintained at levels well below certain mandated minima. Principle applications are in electrical environments of the kind associated with medical equipment, conventional and nuclear power plants, automatic test equipment, and industrial process control systems.

In the basic two-port form, the output and power circuits are not isolated from one another. In the three-port isolator shown in Figure 2.39, the input circuits, output circuits, and power source are all isolated from one another. The figure shows the circuit architecture of a self-contained isolator, the AD210. An isolator of this type requires power from a two-terminal DC power supply. An internal oscillator (50kHz) converts the DC power to AC, which is transformer-coupled to the shielded input section, then converted to DC for the input stage and the auxiliary power output. The AC carrier is also modulated by the amplifier output, transformer-coupled to the output stage, demodulated by a phase-sensitive demodulator (using the carrier as the reference), filtered, and buffered using isolated DC power derived from the carrier. The AD210 allows the user to select gains from 1 to 100 using an external resistor. Bandwidth is 20kHz, and voltage isolation is 2500V RMS (continuous) and  $\pm 3500V$  peak (continuous).

## AD210 3-PORT ISOLATION AMPLIFIER

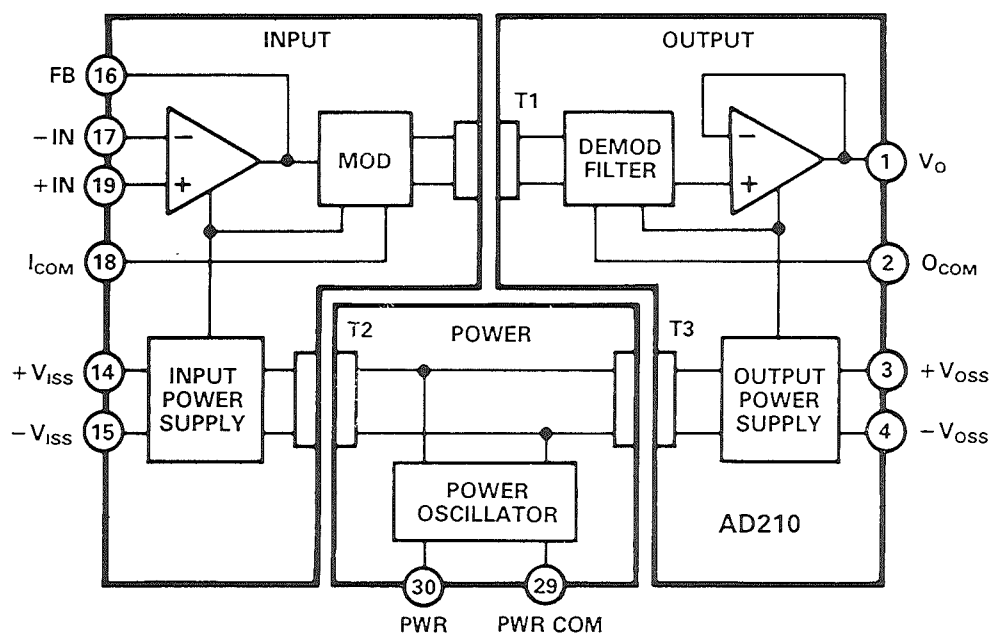


Figure 2.39

The AD210 is a 3-port isolation amplifier: the power circuitry is isolated from both the input and the output stages and may therefore be connected to either - or to neither. It uses trans-

former isolation to achieve 3500V isolation with 12-bit accuracy. Key specifications for the AD210 are summarized in Figure 2.40.

## AD210 ISOLATION AMPLIFIER KEY FEATURES

- Transformer Coupled
- High Common-Mode Voltage Isolation:
  - 2500V RMS Continuous
  - ± 3500V Peak Continuous
- Wide Bandwidth: 20kHz (Full-Power)
- ± 0.012% Maximum Non-Linearity
- Input Amplifier: Gain 1 to 100
- Isolated Input and Output Power Supplies, ± 15V @ ± 5mA

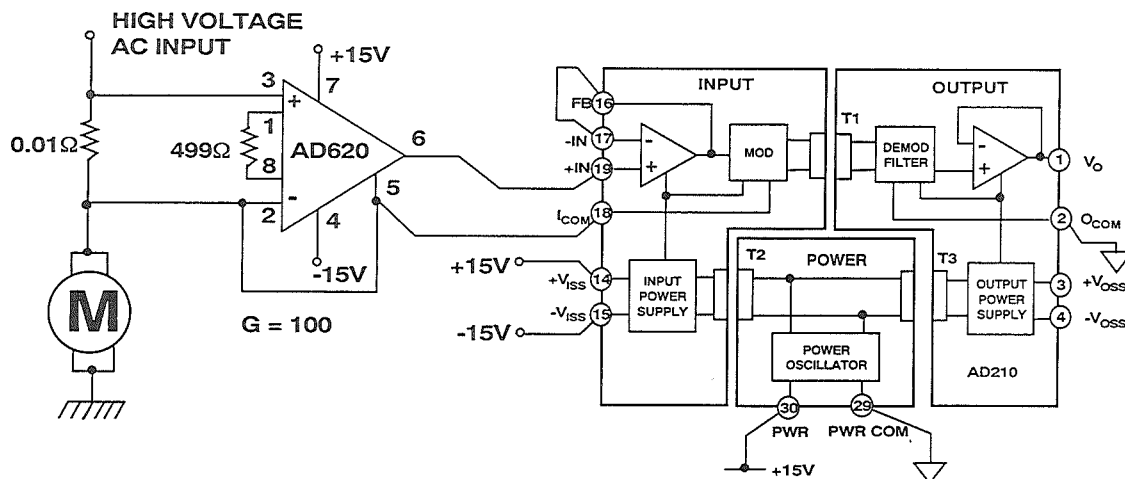
Figure 2.40



A typical isolation amplifier application using the AD210 is shown in Figure 2.41. The AD210 is used with an AD620 instrumentation amplifier in a current-sensing system for motor control. The input of the AD210, being isolated, can be connected to a 110 or 230 V power line without any protection, and the isolated  $\pm 15$  V powers the AD620, which senses the voltage drop in a small current sensing resistor. The 110 or

230V RMS common-mode voltage is ignored by the isolated system. The AD620 is used to improve system accuracy: the  $V_{OS}$  of the AD210 is 15mV, while the AD620 has  $V_{OS}$  of  $30\mu\text{V}$  and correspondingly lower drift. If higher DC offset and drift are acceptable, the AD620 may be omitted, and the AD210 used directly at a closed loop gain of 100.

## MOTOR CONTROL CURRENT SENSING



- High Accuracy/Low-Drift of AD620
- AD620 Powered By AD210
- Floating, Isolated, Senses Up To 2000V

Figure 2.41

Optical isolators using optical fibers may be made with isolation voltages of tens of MV. More general purpose devices consist of an LED and a photo-cell, electrically isolated, but in a single package, and having a breakdown voltage in the range 3.5 - 10kV. The

coupling between the two elements is not linear, so they cannot be used in simple analog isolation amplifiers, although they will carry digital signals, and hence the results of A/D or V/F conversion very efficiently.

## FOR HIGHER VOLTAGE BARRIERS USE OPTO-ISOLATORS

- Uses Light for Transmission Over a High Voltage Barrier
- An LED is the Transmitter, and a Photodiode or Phototransistor is the Receiver
- High Voltage Isolation is in the Range of 5000V to 7000V
- Usually Not Linear -- Best for Digital or Frequency Information

2

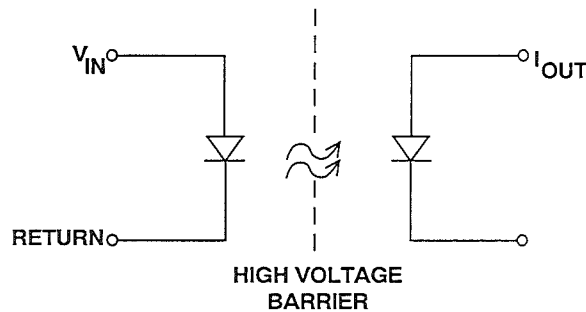


Figure 2.42

Voltage-Frequency Converters (VFCs) are valuable in systems requiring isolation. The analog signal is converted to a frequency in a VFC and may then be transmitted across an isolation barrier by very simple means, with no risk of non-linearity, and greatly reduced susceptibility to noise. At the receiver, there are two options: the

signal may be applied to a counter for a fixed period and the count read by a digital processor, the combination of VFC and counter acting as an ADC, or the frequency may be converted back to a voltage in a Frequency-Voltage Converter (FVC). FVC and VFCs are discussed in detail in Section 5 of this book (Data Converters).

## ISOLATION USING VOLTAGE-TO-FREQUENCY (V/F) CONVERTERS

- Converts a DC Voltage to a Frequency
- Frequency Information is Immune to Offsets and Noise
- V/F Output Can Be Transmitted Over Non-Linear Transmission Media
- Long Distance Transmission Over Twisted Pair or Fiber Optic Links
- A Frequency-to-Voltage (F/V) Converter is Used as the Receiver
- Accuracy is Determined by the V/F and F/V Conversion Process

Figure 2.43

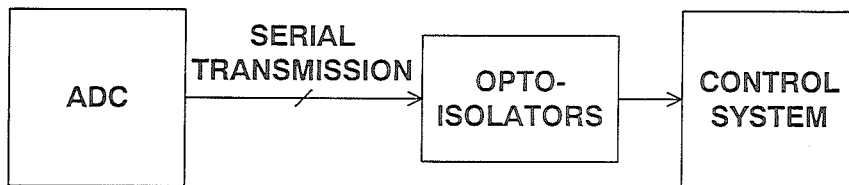
Despite the preceding discussion of analog isolation techniques, there is no doubt that the most accurate technique is analog-to-digital conversion *before* transmission across the isolation barrier (VFC-FVC is, after all, one version of this technique). If the signal will eventually be required in digital form, the technique is particularly attractive, especially as there is no serious limit on the distance the data may be transmitted (Figure 2.44).

In the past, the limitations of ADCs may have discouraged this approach, but inexpensive, modern, high-resolu-

tion, low-power ADCs with serial data output, and inexpensive digital opto-isolators may make the technique attractive, even when the output signal required is analog, and a digital-to-analog conversion is necessary after transmission.

Despite evolution in the techniques available, the need for galvanic isolation will remain for the foreseeable future. Each technique has its advantages and disadvantages, and engineers must choose the most appropriate technique for the particular application.

### FOR HIGH ACCURACY ISOLATION, DIGITIZE FIRST



- Accuracy Limited Only By ADC
- Digital Transmission Relatively Immune To Noise

Figure 2.44

## ISOLATING TRANSDUCERS SUMMARY

TECHNOLOGY	ADVANTAGES	DISADVANTAGES
AD20x-Family Transformer Coupled	Fully Self-Contained 3-Port Isolation High Linearity Wide Bandwidth (20kHz)	Lower Breakdown Voltage
Capacitive Coupling	Cheap	Lower Breakdown Voltage Low Resolution Separate Power Needed
Opto-Isolators	High Voltage Immunity	Separate Power Needed External Amplifiers Required Poor Linearity
V/F and F/V Isolation	High Linearity Long Distance Transmission High Noise Immunity	Separate Power Needed DC Inputs Only
Digitize First	Highest Accuracy Best Linearity High Noise Immunity Long Distance Transmission	Separate Power Needed

Figure 2.45

## COMPARATORS

A comparator is similar to an op amp and is specifically designed to compare the voltages between its two inputs. The comparator operates open-loop, providing a two-state logic output voltage. These two states represent the sign of the net difference between the two inputs (including the effects of the comparator input offset voltage). Therefore, the comparator's output will be a

logic "1" if the differential input signal exceeds the offset voltage,  $V_{OS}$ , and a logic "0" for the opposite case. A comparator is normally used in applications where some varying signal level is compared to a fixed level (usually a voltage reference). Since it is, in effect, a 1-bit analog-to-digital converter (ADC), the comparator is a basic element in all ADCs.

## COMPARATORS

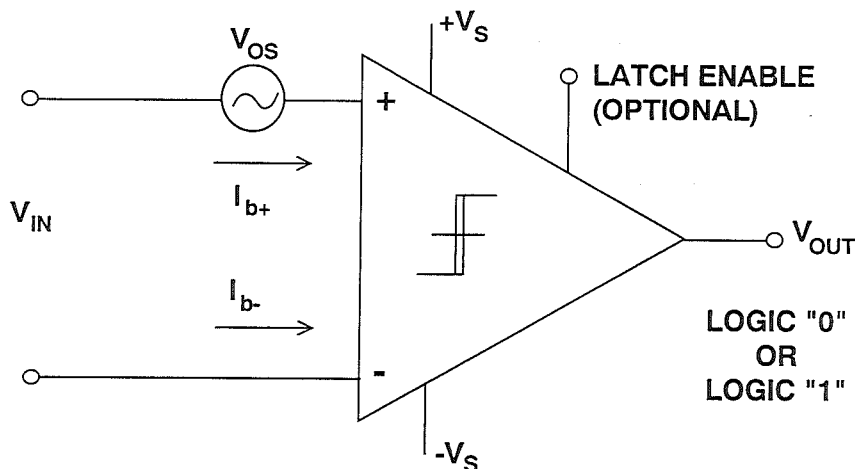


Figure 2.46

Most comparators have an internal latch. The latch-enable signal has two states: *compare* (track) and *latch* (hold). When the latch-enable signal is in the compare state, the comparator output continuously responds to the sign of the net differential input signal. When the latch-enable signal transitions to the latch state, the comparator output goes to either a logic "1" or a logic "0", depending on the sign of the differential input signal at the instant of the transition (at this point, we are neglecting the setup and hold-time, as well as the

output propagation delay associated with the latch-enable function). Even though many comparators have a latch-enable function, they are often operated only in the compare mode.

Comparator DC specifications are similar to those of op amps: input offset voltage, input bias current, offset and drift, common-mode input range, gain, CMR, and PSR. Standard logic-related DC, timing and interface specs are associated with the comparator outputs.

## KEY COMPARATOR SPECIFICATIONS

- DC:
  - ◆ Input Offset Voltage, Input Bias Current
  - ◆ Gain (Open-Loop)
  - ◆ Common-Mode Input Range
  - ◆ Common Mode Rejection (CMR)
  - ◆ Power Supply Rejection (PSR)
  - ◆ Hysteresis
  - ◆ Output Logic Levels
  - ◆ Maximum Differential and Common-Mode Inputs
- AC:
  - ◆ Propagation Delay
  - ◆ Propagation Delay Dispersion
  - ◆ Output Logic Rise and Fall Time
  - ◆ Latch-Enable Delay to Output High and Low
  - ◆ Minimum Latch-Enable Pulse Width
  - ◆ Latch-Enable Input Setup and Hold Time

Figure 2.47

The addition of hysteresis to a comparator's transfer function is often useful in a noisy environment, or where it is undesirable for the comparator to toggle continuously between states

when the input signal is at or near the switching threshold. The transfer function for a comparator with hysteresis is shown in Figure 2.48.

## COMPARATOR HYSTERESIS

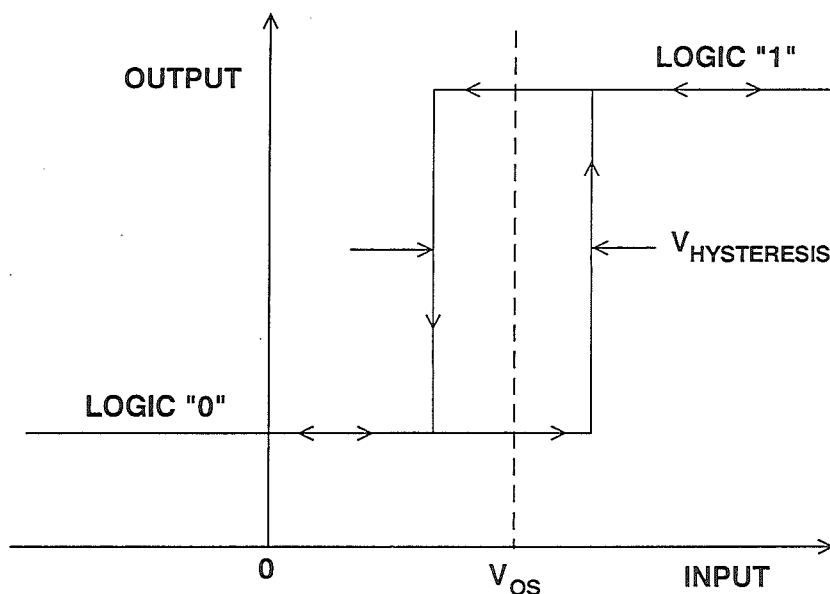


Figure 2.48

If the input voltage approaches the switching threshold ( $V_{OS}$ ) from the negative direction, the comparator will switch from a "0" to a "1" when the input crosses  $V_{OS} + V_H/2$ . The "new" switching threshold now becomes  $V_{OS} - V_H/2$ . The comparator output will remain in a "1" state until the threshold  $V_{OS} - V_H/2$  is crossed, coming from the positive direction. Input noise centered around  $V_{OS}$  will not cause the comparator to switch states unless it exceeds the region bounded by  $V_{OS} \pm V_H/2$ .

The key comparator AC specification is *propagation delay*: it is the time required for the output to reach the 50% point of a transition, after the differential input signal crosses the offset voltage - when driven by a square wave (typically 100mV in amplitude) to a prescribed value of input overdrive (usually 5mV or 10mV).

## COMPARATOR PROPAGATION DELAY

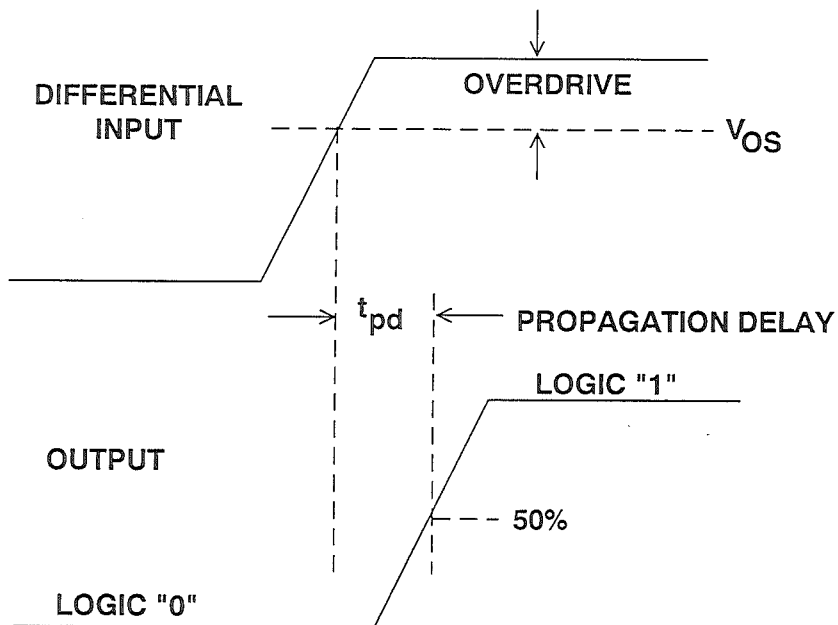


Figure 2.49

The propagation delay in practical comparators decreases somewhat as the input overdrive is increased. This variation in propagation delay as a function of overdrive is called *dispersion*. The effects of dispersion are illustrated in the ATE application shown in Figure 2.51, where the ECL gate under test (DUT) is being tested for output logic risetime. The comparator threshold is first set to  $-1.7\text{V}$  (10% point). The programmable delay,  $T_2$ , is adjusted until the output of the D flip-flop is toggling equally between the "1" and "0" output states. The comparator

threshold is then set to  $-0.9\text{V}$  (90% point), and the programmable delay is changed until the D flip-flop is again toggling equally between the "1" and "0" output states. The change in  $T_2$  between the two measurements corresponds to the DUT output logic risetime. Comparator dispersion will cause a corresponding risetime measurement error due to the two different overdrive conditions required to perform the 10% and 90% measurement. Fast comparators for ATE applications typically have dispersions less than 100ps.

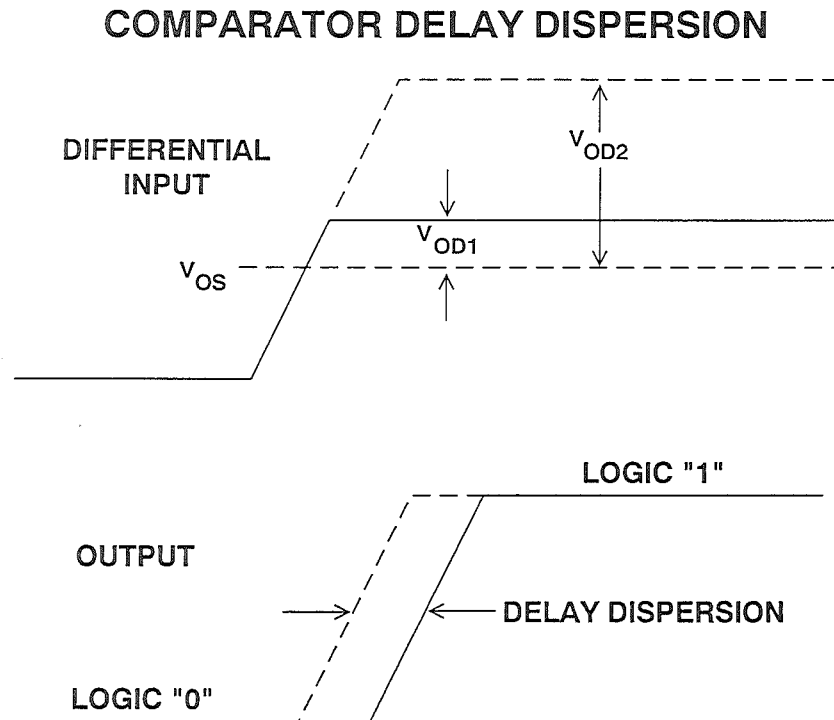


Figure 2.50



## RISETIME MEASUREMENT USING COMPARATOR IN AN ATE SYSTEM

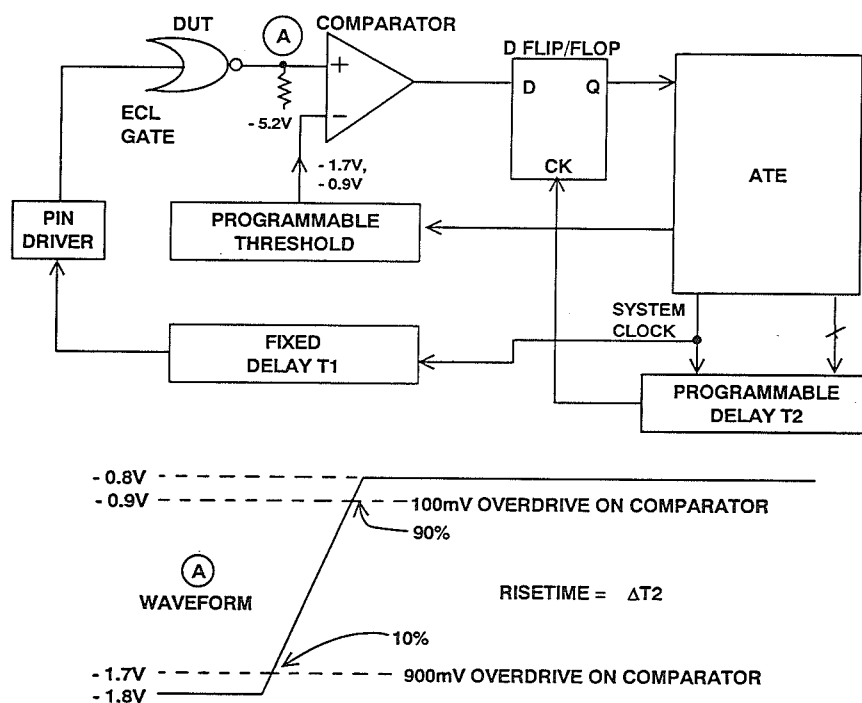


Figure 2.51

## COMPARATOR/RAMP DELAY GENERATOR

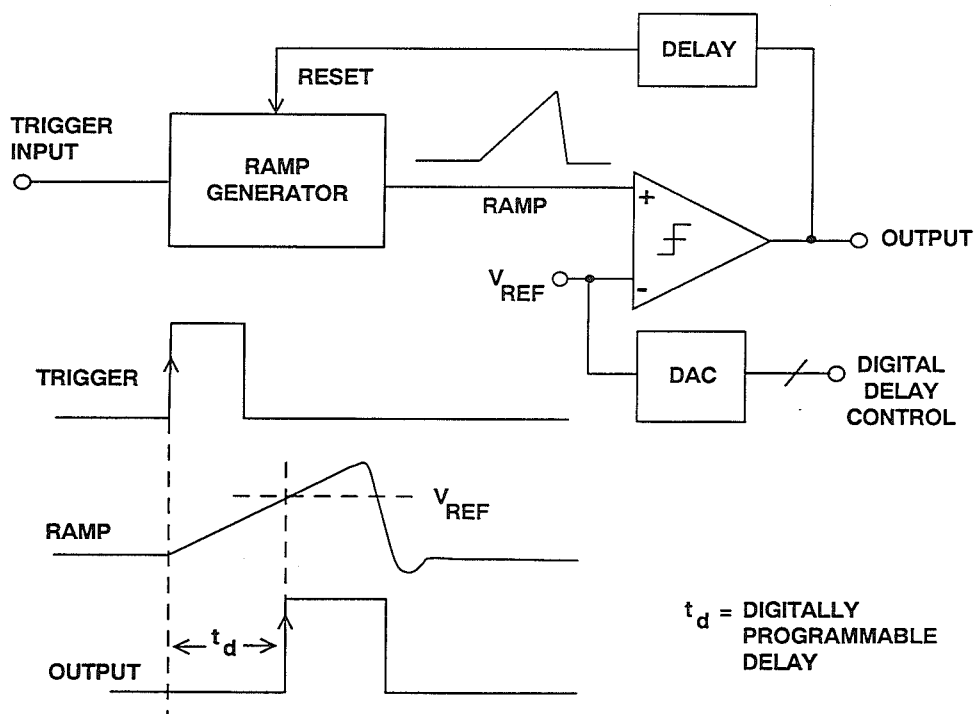


Figure 2.52

A comparator may be used for precise time delay generation if one of its inputs is driven by a ramp voltage (Figure 2.52). The steadily increasing (or decreasing) ramp is applied to the comparator, and its output will change state when its reference level is crossed. The comparator is also an important element of pulse-width modulators, peak detectors, delay generators, time-to-digital converters, and microprocessor supervisory circuits.

Window comparators make use of two comparators with different reference voltages and a common input voltage. The comparators are connected to logic in such a way that the final output logic level is asserted when the input signal falls between the two reference voltages (Figure 2.53). This circuit may be used with fast comparators to make accurate settling time measurements.

### WINDOW COMPARATOR CIRCUIT

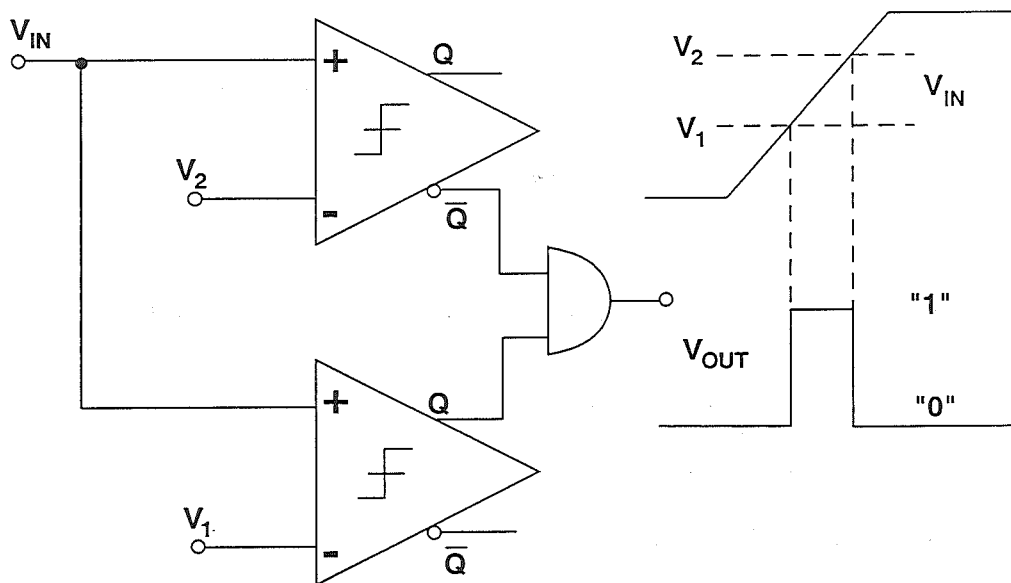


Figure 2.53

The comparator internal latch-enable function is particularly useful in ADC applications because it allows the comparator decision to be recorded *at a known instant of time*. Flash converters make use of this concept and are constructed of many parallel comparators which share a common latch-enable line. Typical timing associated with the latch-enable function is shown in Figure 2.54. The delay between the assertion of

latch-enable and the 50% point of the output logic swing is referred to as *latch-enable to output delay*. It may be different for positive and negative-going outputs. The other key specification associated with the latch-enable function is the minimum allowable latch-enable pulse width. This specification determines the maximum frequency at which the comparator can be strobed.

## LATCH-ENABLE TIMING

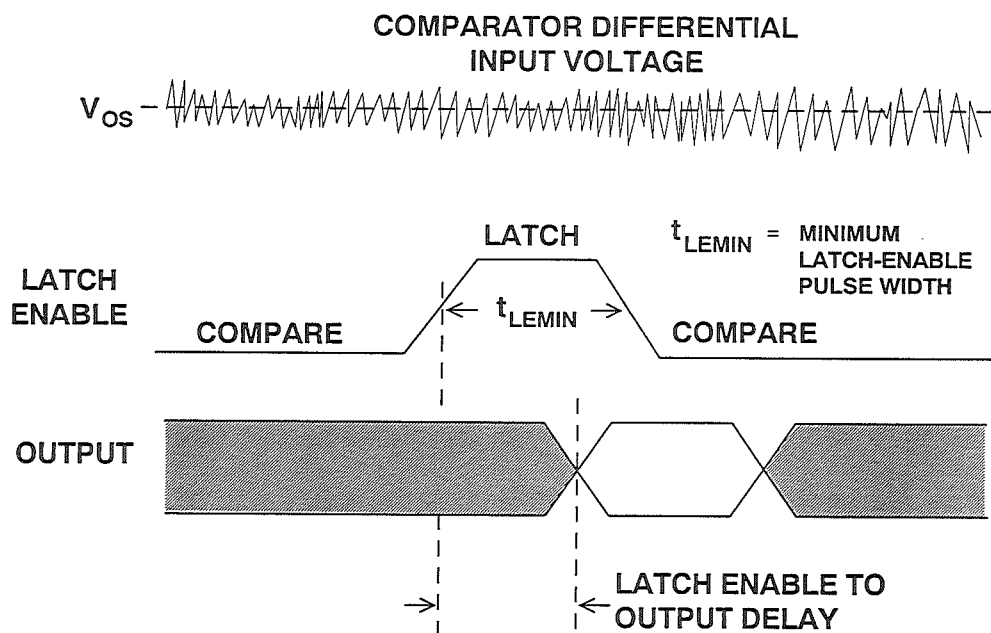


Figure 2.54

Fast comparators are somewhat difficult to apply because of their high gain and bandwidth. Proper application of high speed layout, grounding, decoupling, and signal routing is mandatory when using comparators. The biggest problem is their tendency to oscillate when the input signal is very near to or equal to the switching thresh-

old. Hysteresis and the use of a narrow latch-enable pulse will generally help this condition. TTL comparators are more likely to oscillate than ECL ones because of their large output swings and fast edges, often combined with power supply current spikes as the output changes state.

## REDUCING COMPARATOR OSCILLATION

- Use Good High Frequency Techniques:
  - ◆ Signal Routing
  - ◆ Grounding (Using Ground Plane)
  - ◆ Decoupling (HF and LF)
  - ◆ No Sockets
- Use Narrow Latch-Enable Strobe
- Hysteresis

Figure 2.55

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2. C. Kitchen and L. Counts, **Instrumentation Amplifier Applications Guide**, Analog Devices, Inc., 1991.
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4. **System Applications Guide**, Analog Devices, Inc., 1993.

## SECTION 3

### ANALOG SIGNAL PROCESSING CIRCUITS

- Dynamic Range Compression
- Logarithmic Amplifiers
- Analog Multipliers
- RMS to DC Converters
- Modulators and Mixers
- Automatic Gain Control (AGC) and Voltage-Controlled Amplifiers (VCAs)



## SECTION 3

## ANALOG SIGNAL PROCESSING CIRCUITS

*James Bryant, Walt Kester*

## DYNAMIC RANGE COMPRESSION

In some cases, a wide dynamic range is an essential aspect of a signal, something to be preserved at all costs. This is true, for example, in the high-quality reproduction of music. However, it is often necessary to compress the signal to a smaller range without any significant loss of information. Compression is often used in magnetic recording, where the upper end of the dynamic range is limited by tape saturation, and the lower end by the granularity of the medium. In professional noise-reduction systems, compression is “undone” by precisely-matched nonlinear expansion during reproduction. Similar techniques are often used in conveying speech over noisy channels, where the performance is more likely to be measured in terms of word-intelligibility than audio fidelity. The reciprocal processes of compressing and expanding are implemented using “compandors”, and many schemes have been devised to achieve this function.

Logarithmic amps find wide applications where signals having wide dynamic ranges (perhaps greater than 100dB) must be processed by elements, such as ADCs, which may have more limited dynamic ranges. Log amps have maximum incremental gain for small signals; the gain decreases in inverse proportion to the magnitude of the input. This permits the amplifier to accept signals with a wide input dynamic range and compress them substantially.

Log amps provide nonlinear dynamic range compression and are used in applications where low harmonic distortion is not a requirement. All types of log amps produce a low dynamic range output without the need to first acquire some measure of the signal amplitude for use in controlling gain.

There is another class of *linear* dynamic range compression systems where the gain of the amplifiers in the signal processing chain is independent of the instantaneous amplitude of the signal, but is controlled by a closed loop system in such a way as to render the output (that is the peak, or rms value) essentially constant. The harmonic distortion is relatively low. These systems use what are often called *variable-gain amplifiers*. While correct, this lacks precision, because *nonlinear* amplifiers (such as log amps) also exhibit variable gain, but in direct response to the signal magnitude. The term *voltage controlled amplifier* (VCA) is preferred in this context; it clearly describes the way in which the gain control is implemented, while allowing latitude in regard to the actual circuit means used to achieve the function. The gain may be controlled by a *current* within the circuit, but usually a voltage. Analog multipliers may be used as VCAs, but other topologies will also be discussed later in this section.

In this section, we will first examine *nonlinear* signal compression using log amps. A discussion of analog multipli-



ers follows, with emphasis on analog signal processing applications. Finally, a discussion of *linear* compression techniques using voltage-controlled

amplifiers within automatic-gain-control (AGC) loops concludes the section.

### LOGARITHMIC AMPLIFIERS

The term "Logarithmic Amplifier" (generally abbreviated to "log amp") is something of a misnomer, and "Logarithmic Converter" would be a better description. The conversion of a signal to its equivalent logarithmic value involves a nonlinear operation, the consequences of which can be confusing if not fully understood. It is important to realize that many of the familiar concepts of linear circuits are irrelevant to log amps. For example, the incremental gain of an ideal log amp approaches infinity as the input tends to zero, and a change of offset at the output of a log amp is equivalent to a change of amplitude at its input - not a change of input offset.

For the purposes of simplicity in our initial discussions, we shall assume that

both the input and the output of a log amp are voltages, although there is no particular reason why logarithmic current, transimpedance, or transconductance amplifiers should not also be designed.

If we consider the equation  $y = \log(x)$  we find that every time  $x$  is multiplied by a constant  $A$ ,  $y$  increases by another constant  $A1$ . Thus if  $\log(K) = K1$ , then  $\log(AK) = K1 + A1$ ,  $\log(A^2K) = K1 + 2A1$ , and  $\log(K/A) = K1 - A1$ . This gives a graph as shown in Figure 3.1, where  $y$  is zero when  $x$  is unity,  $y$  approaches minus infinity as  $x$  approaches zero, and which has no values for  $x$  for which  $y$  is negative.

### GRAPH OF $Y = \text{LOG}(X)$

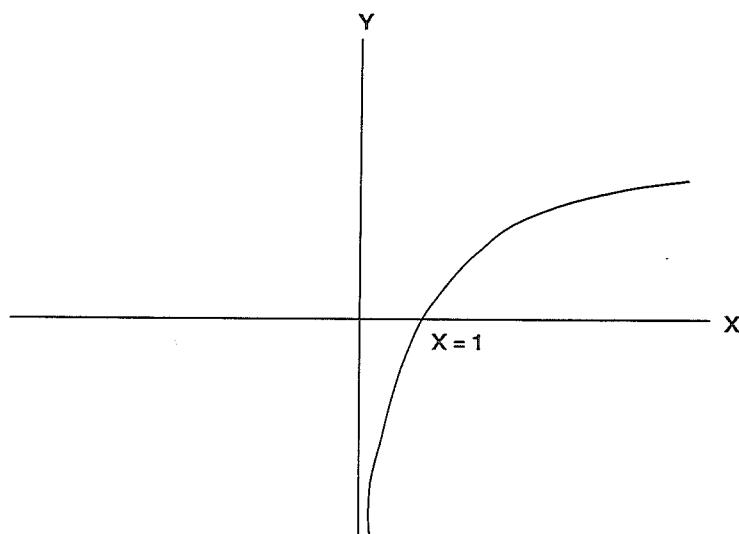


Figure 3.1

On the whole, log amps do not behave in this way. Apart from the difficulties of arranging infinite negative output voltages, such a device would not, in fact, be very useful. A log amp must satisfy a transfer function of the form

$$V_{out} = V_y \log(V_{in}/V_x)$$

over some range of input values which may vary from 100:1 (40dB) to over 1,000,000:1 (120dB).

With inputs very close to zero, log amps cease to behave logarithmically, and most then have a linear  $V_{in}/V_{out}$  law. This behavior is often lost in device noise. Noise often limits the dynamic

range of a log amp. The constant,  $V_y$ , has the dimensions of voltage, because the output is a voltage. The input,  $V_{in}$ , is divided by a voltage,  $V_x$ , because the argument of a logarithm must be a simple dimensionless ratio.

A graph of the transfer characteristic of a log amp is shown in Figure 3.2. The scale of the horizontal axis (the input) is logarithmic, and the ideal transfer characteristic is a straight line. When  $V_{in} = V_x$ , the logarithm is zero ( $\log 1 = 0$ ).  $V_x$  is therefore known as the *intercept voltage* of the log amp because the graph crosses the horizontal axis at this value of  $V_{in}$ .

## LOG AMP TRANSFER FUNCTION

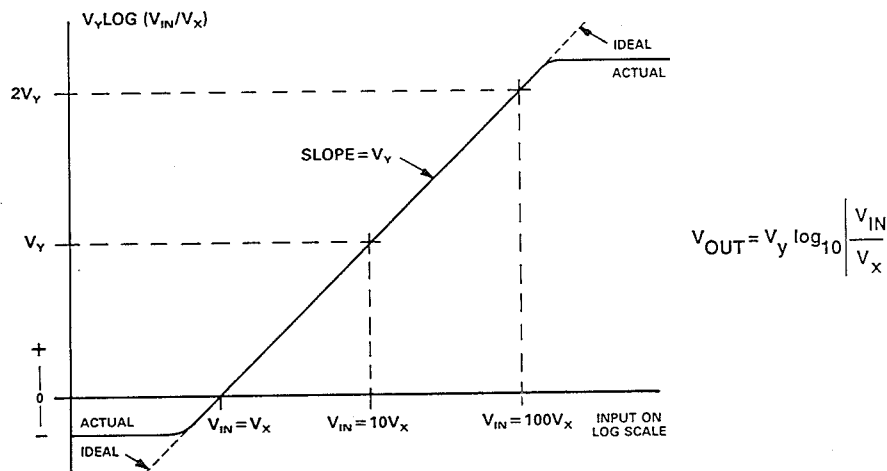


Figure 3.2

The slope of the line is proportional to  $V_y$ . When setting scales, logarithms to the base 10 are most often used because this simplifies the relationship to decibel values: when  $V_{in} = 10V_x$ , the logarithm has the value of 1, so the output voltage is  $V_y$ . When  $V_{in} = 100V_x$ , the output is  $2V_y$ , and so forth.  $V_y$  can therefore be viewed either as the "slope voltage" or as the "volts per decade factor."

The logarithm function is indeterminate for negative values of  $x$ . Log amps can respond to negative inputs in three different ways: (1) They can give a fullscale negative output as shown in

Figure 3.3. (2) They can give an output which is proportional to the log of the absolute value of the input and disregards its sign as shown in Figure 3.4. This type of log amp can be considered to be a full-wave detector with a logarithmic characteristic, and is often referred to as a *detecting* log amp. (3) They can give an output which is proportional to the log of the absolute value of the input and has the same sign as the input as shown in Figure 3.5. This type of log amp can be considered to be a video amp with a logarithmic characteristic, and may be known as a *logarithmic video* (*log video*) amplifier or, sometimes, a *true log amp*.

### BASIC LOG AMP (SATURATES WITH NEGATIVE INPUT)

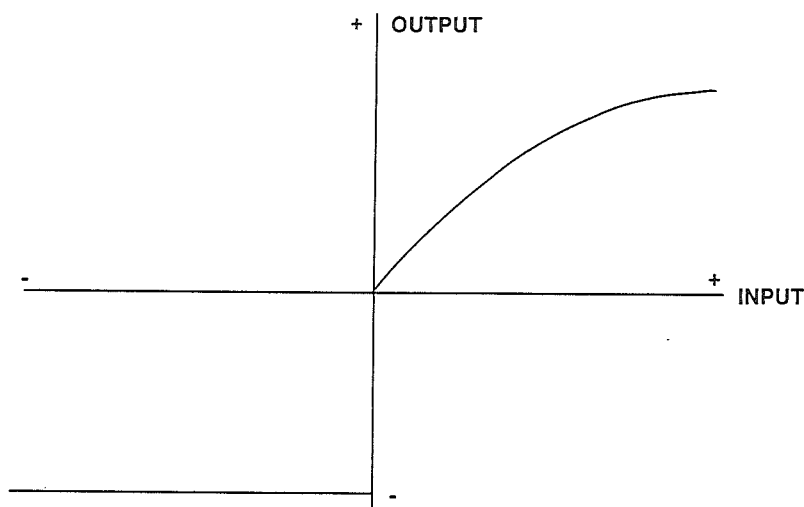


Figure 3.3

**DETECTING LOG AMP  
(OUTPUT POLARITY INDEPENDENT  
OF INPUT POLARITY)**

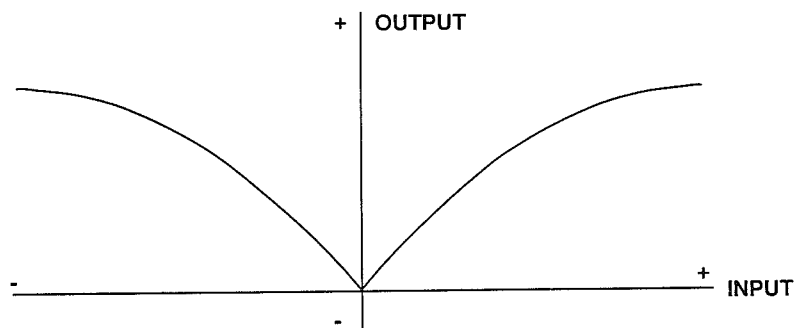


Figure 3.4

**LOG VIDEO OR "TRUE LOG AMP"  
(SYMMETRICAL RESPONSE  
TO POSITIVE OR NEGATIVE SIGNALS)**

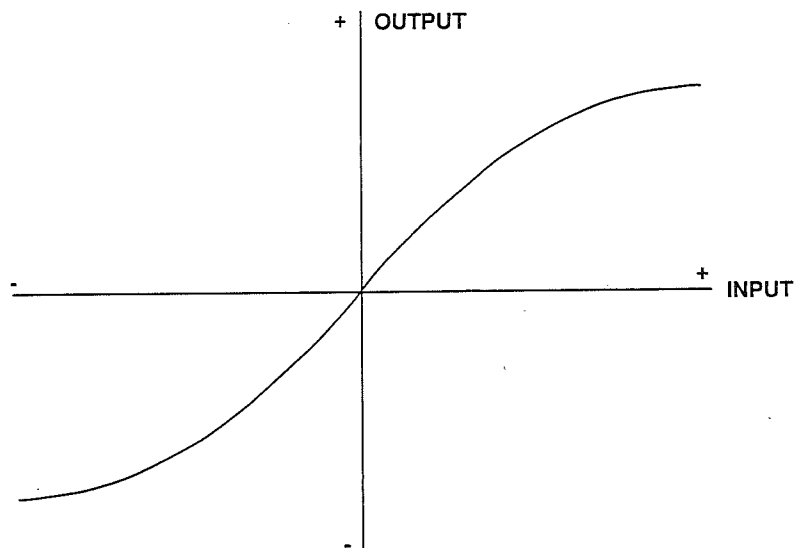


Figure 3.5

There are three basic architectures which may be used to produce log amps: the *basic diode log amp*, the *successive detection log amp*, and the “*true log amp*” which is based on cascaded semi-limiting amplifiers.

The voltage across a silicon diode is proportional to the logarithm of the current through it. If a diode is placed in the feedback path of an inverting op-amp, the output voltage will be proportional to the log of the input current as shown in Figure 3.6. In practice, the dynamic range of this configuration is limited to 40-60dB because of non-ideal diode characteristic, but if the diode is replaced with a diode-connected transistor as shown in Figure 3.7, the dynamic range can be extended to 120dB or more. This type of log amp has three disadvantages: (1) both the slope and intercept are temperature dependent; (2) it will only handle unipolar signals; and (3) its bandwidth is both limited

and dependent on signal amplitude. Where several such log amps are used on a single chip to produce an analog computer which performs both log and antilog operations, the temperature variation in the log operations is unimportant, since it is compensated by a similar variation in the antilogging. This makes possible the AD538, a monolithic analog computer which can multiply, divide, and raise to powers (see Figure 3.8). Where actual logging is required, however, the AD538 and similar circuits require temperature compensation (Reference 7). The major disadvantage of this type of log amp for high frequency applications, though, is its limited frequency response - which cannot be overcome. However carefully the amplifier is designed, there will always be a residual feedback capacitance  $C_c$  (often known as Miller capacitance), from output to input which limits the high frequency response (See Figure 3.7).

## THE DIODE / OP-AMP LOG AMP

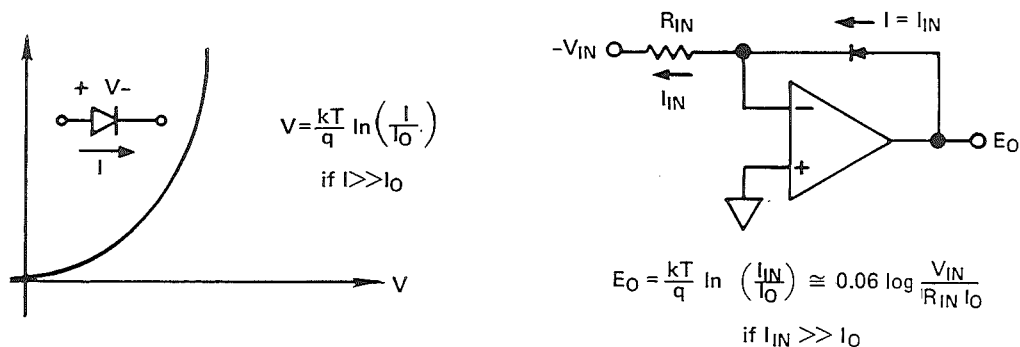


Figure 3.6

### TRANSISTOR / OP-AMP LOG AMP

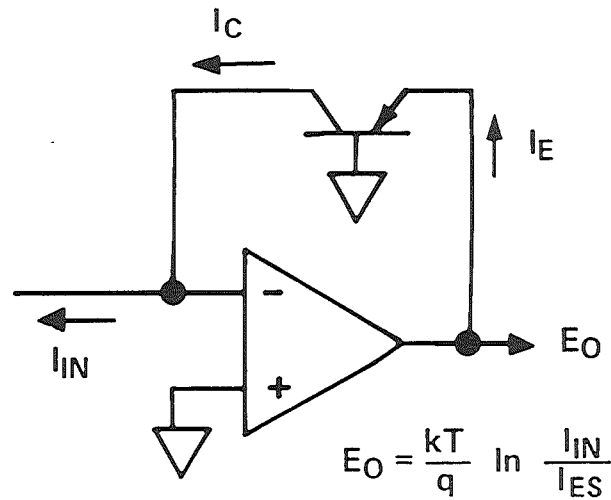


Figure 3.7

### AD538 LOG AMP SIMPLIFIED DIAGRAM

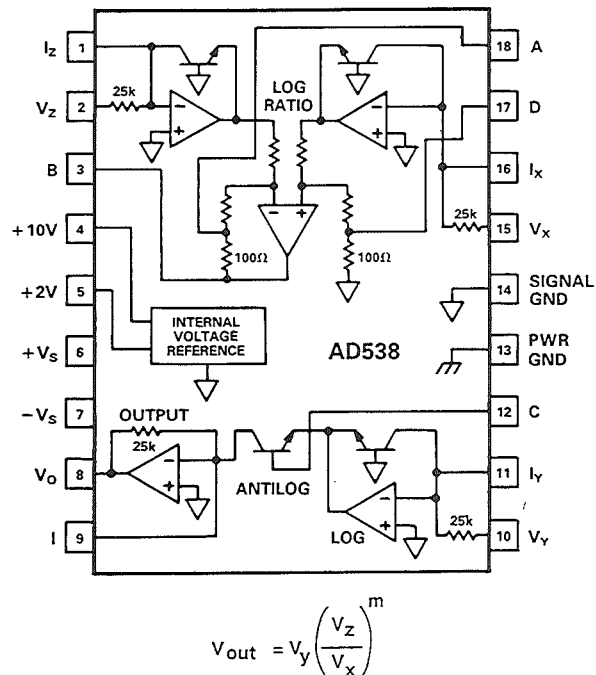


Figure 3.8

What makes this Miller capacitance particularly troublesome is that the impedance of the emitter-base junction is inversely proportional to the current flowing in it - so that if the log amp has a dynamic range of 1,000,000:1, then its bandwidth will also vary by 1,000,000:1. In practice, the variation is less because other considerations limit the large signal bandwidth, but it is very difficult to make a log amp of this type with a small-signal bandwidth greater than a few hundred kHz.

For high frequency applications, therefore, detecting and "true log" architectures are used. Although these differ in detail, the general principle behind

their design is common to both: instead of one amplifier having a logarithmic characteristic, these designs use a number of similar cascaded linear stages having well-defined large signal behavior.

Consider N cascaded limiting amplifiers, the output of each driving a summing circuit as well as the next stage (Figure 3.9). If each amplifier has a gain of A dB, the small signal gain of the strip is NA dB. If the input signal is small enough for the last stage not to limit, the output of the summing amplifier will be dominated by the output of the last stage.

## BASIC MULTI-STAGE LOG AMP ARCHITECTURE

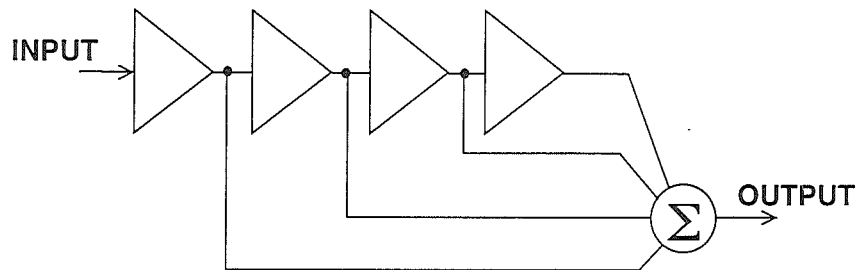


Figure 3.9

As the input signal increases, the last stage will limit. It will now make a fixed contribution to the output of the summing amplifier, but the incremental gain to the summing amplifier will drop to  $(N-1)A$  dB. As the input continues to increase, this stage in turn will limit and make a fixed contribution to the output, and the incremental gain will drop to  $(N-2)A$  dB, and so forth - until the first stage limits, and the output ceases to change with increasing signal input.

The response curve is thus a set of straight lines as shown in Figure 3.10. The total of these lines, though, is a very good approximation to a logarithmic curve, and in practical cases, is an even better one, because few limiting amplifiers, especially high frequency ones, limit quite as abruptly as this model assumes.

### BASIC MULTI-STAGE LOG AMP RESPONSE (UNIPOLAR CASE)

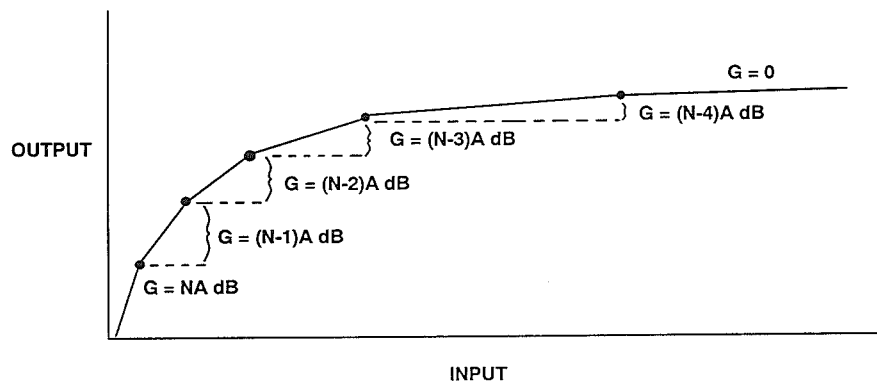


Figure 3.10

The choice of gain,  $A$ , will also affect the log linearity. If the gain is too high, the log approximation will be poor. If it is too low, too many stages will be required to achieve the desired dynamic range. Generally, gains of 10 to 12dB ( $3x$  to  $4x$ ) are chosen.

This is, of course, an ideal and very general model - it demonstrates the

principle, but its practical implementation at very high frequencies is difficult. Assume that there is a delay in each limiting amplifier of  $t$  nanoseconds (this delay may also change when the amplifier limits but let's consider first order effects!). The signal which passes through all  $N$  stages will undergo delay of  $Nt$  nanoseconds, while the signal which only passes one stage will be



delayed only  $t$  nanoseconds. This means that a small signal is delayed by  $Nt$  nanoseconds, while a large one is "smeared", and arrives spread over  $Nt$  nanoseconds. A nanosecond equals a foot at the speed of light, so such an effect represents a spread in position of  $Nt$  feet in the resolution of a radar system-which may be unacceptable in some systems (for most log amp applications this is not a problem).

A solution is to insert delays in the signal paths to the summing amplifier, but this can become complex. Another solution is to alter the architecture slightly so that instead of limiting gain stages, we have stages with small

signal gain of  $A$  and large signal (incremental) gain of unity (0dB). We can model such stages as two parallel amplifiers, a limiting one with gain, and a unity gain buffer, which together feed a summing amplifier as shown in Figure 3.11.

Figure 3.11 shows that such stages, cascaded, form a log amp without the necessity of summing from individual stages. Both the multi-stage architectures described above are *video* log amplifiers, or *true log* amplifiers, but the most common type of high frequency log amplifier is the *successive detection* log amp architecture shown in Figure 3.12.

## STRUCTURE AND PERFORMANCE OF "TRUE" LOG AMP ELEMENT AND OF A LOG AMP FORMED BY SEVERAL SUCH ELEMENTS

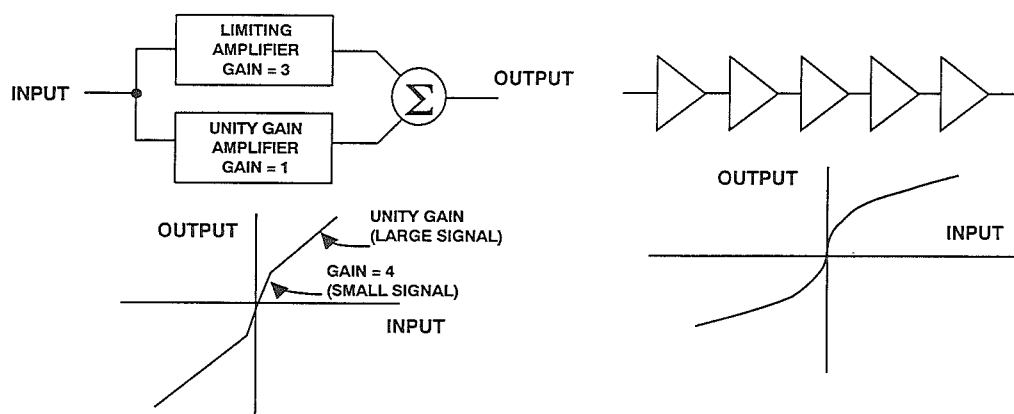
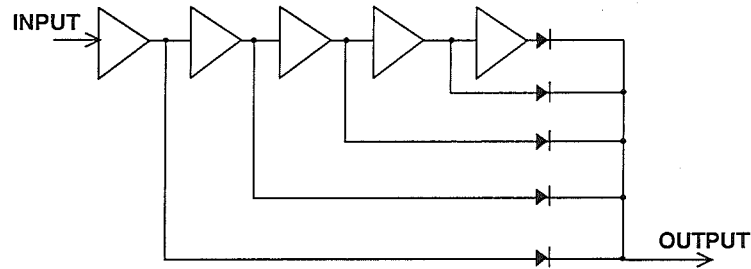


Figure 3.11

## SUCCESSIVE DETECTION LOGARITHMIC AMPLIFIER



Detectors may be full- or half-wave but should be current output devices (not simple diodes) so that the detector outputs may be summed without additional summing components being necessary.

Figure 3.12

The *successive detection* log amp consists of cascaded limiting stages as described above, but instead of summing their outputs directly, these outputs are applied to detectors, and the detector outputs are summed as shown in Figure 3.12. If the detectors have current outputs, the summing process may involve no more than connecting all the detector outputs together.

Log amps using this architecture have two outputs: the log output and a limiting output. In many applications, the limiting output is not used, but in some (FM receivers with “S”-meters, for example), both are necessary.

The log output of a successive detection log amplifier generally contains ampli-

tude information, and the phase and frequency information is lost. This is not necessarily the case, however, if a half-wave detector is used, and attention is paid to equalizing the delays from the successive detectors - but the design of such log amps is demanding.

The specifications of log amps will include *noise*, *dynamic range*, *frequency response* (some of the amplifiers used as successive detection log amp stages have low frequency as well as high frequency cutoff), the *slope of the transfer characteristic* (which is expressed as V/dB or mA/dB depending on whether we are considering a voltage- or current-output device), the *intercept point* (the input level at which the output voltage or current is zero), and the *log linearity*. (See Figures 3.13 and 3.14)

## KEY PARAMETERS OF LOG AMPS

- **NOISE:** The Noise Referred to the Input (RTI) of the Log Amp. It May Be Expressed as a Noise Figure or as a Noise Spectral Density (Voltage, Current, or Both) or as a Noise Voltage, a Noise Current, or Both
- **DYNAMIC RANGE:** Range of Signal Over Which the Amplifier Behaves in a Logarithmic Manner (Expressed in dB)
- **FREQUENCY RESPONSE:** Range of Frequencies Over Which the Log Amp Functions Correctly
- **SLOPE:** Gradient of Transfer Characteristic in V/dB or mA/dB
- **INTERCEPT POINT:** Value of Input Signal at Which Output is Zero
- **LOG LINEARITY:** Deviation of Transfer Characteristic (Plotted on log/lin Axes) from a Straight Line (Expressed in dB)

Figure 3.13

## LOG LINEARITY

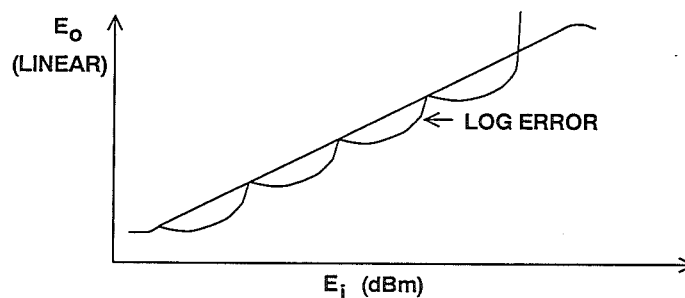


Figure 3.14

In the past, it has been necessary to construct high performance, high frequency successive detection log amps (called log strips) using a number of individual monolithic limiting amplifiers such as the one shown in Figure

3.15). Notice that such components are not, themselves, log amps but are components from which log amps may be made. The circuit contains a limiting amplifier which drives both the output and an internal half-wave rectifier.

### SIMPLIFIED SCHEMATIC OF MONOLITHIC LIMITING AMPLIFIER WITH HALF-WAVE DETECTOR (SL-1521)

3

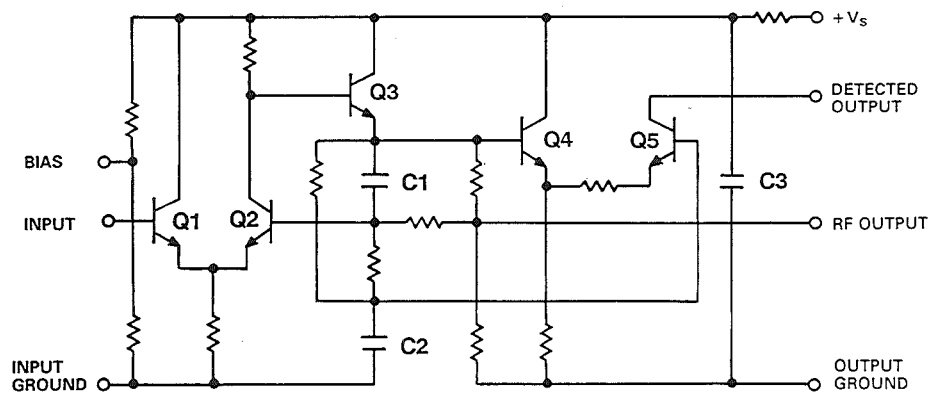


Figure 3.15

### PERFORMANCE OF LIMITING / DETECTING AMPLIFIER (SL-1521)

- Bandwidth: 7MHz to 245MHz
- Voltage Gain: 12dB
- Maximum Detected Output Current: 1mA at 60MHz, RF Input = 0.5V rms
- Maximum RF Output Voltage: 1.6V peak-to-peak
- Maximum Input Before Overload: 1.9V rms
- Power Dissipation: 84mW

Figure 3.16

Figure 3.17 shows the overall transfer function of a log amp made with four such stages. The detected current output of each stage is plotted against input, as is the sum of all the outputs.

It is clear that the sum of these currents approximates a straight line for inputs between  $300\mu\text{V}$  and  $100\text{mV}$  - about 48dB.

### 4-STAGE SUCCESSIVE DETECTION LOG STRIP CONSTRUCTED FROM LIMITING / DETECTING AMPLIFIERS (SL-1521s)

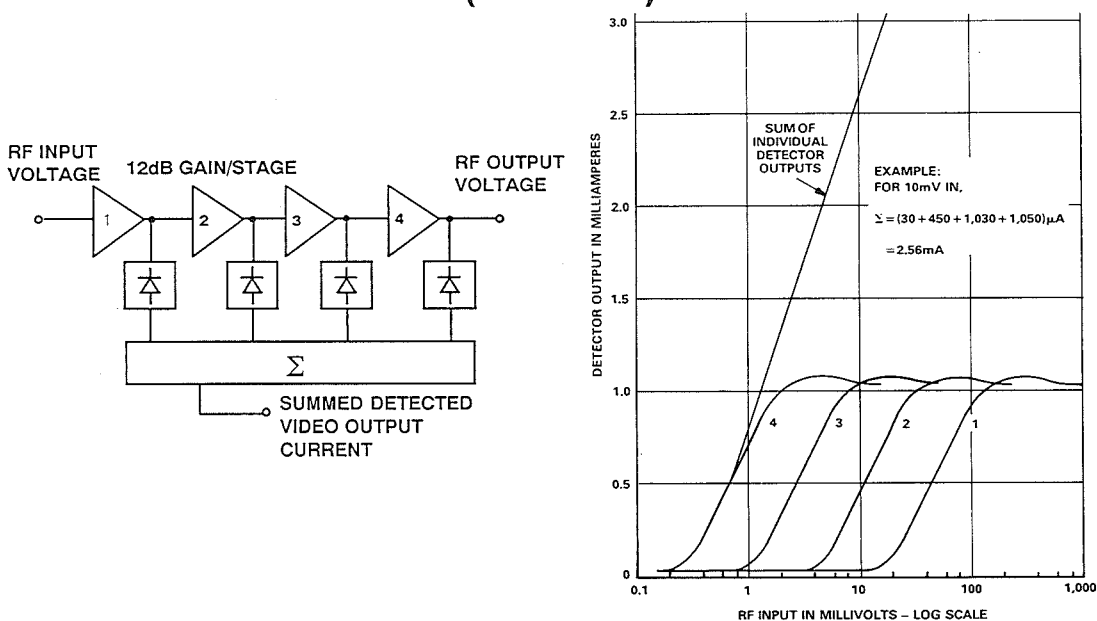
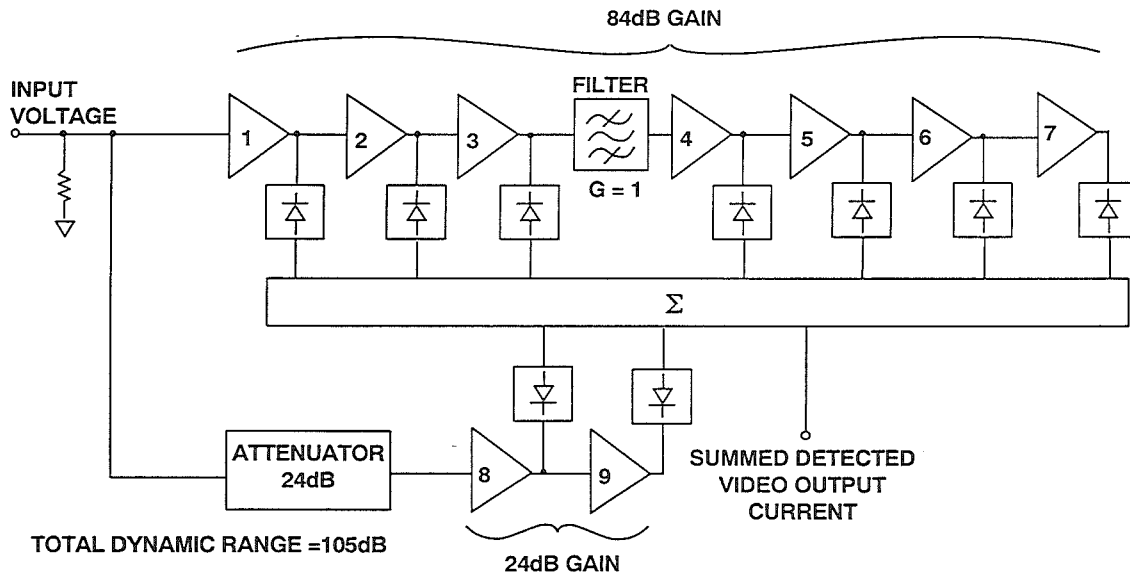


Figure 3.17

If we add stages, the dynamic range increases by 12 dB with each stage until the strip limits on the noise of its own input stage. This occurs with six stages if they are simply connected together broadband. If the noise figure is 5dB at  $450\Omega$ , this gives about  $70\mu\text{V}$  broadband noise (assuming 220MHz bandwidth). The limiting amplifier limits with 100mV drive, so there must be a gain of less than 1428 (63dB) to the input of the last stage. At 12dB/stage, this requires five stages so, with the output stage, we cannot have more than six stages without limiting on noise. This gives a dynamic range of less than 70dB.

We can increase the dynamic range by placing an interstage filter between the third and fourth stages of the strip to limit the bandwidth as shown in Figure 3.18. If we reduce the bandwidth to 10MHz, the noise is reduced by the square root of 22 (13.5dB), so we are still limited to seven stages. The interstage filter used does not affect the accuracy of the log response, PROVIDED that it has a voltage gain which is precisely unity throughout the pass-band.

## 105 dB LOG AMP USING AN AUXILIARY STRIP (SL-1521s)



3

Figure 3.18

If we allow for the effects of noise, seven stages will only give some 80dB dynamic range. If further dynamic range is required, we must use an auxiliary strip. This makes use of the fact that although the output of the limiting amplifier saturates with 100mV input, the device operates without problems with inputs up to 1.9V.

If, therefore, we add another two stage strip of limiting amplifiers, with a 24dB attenuator at its input, in parallel with the existing strip, and summing its outputs to those of the existing strip, we can add another 24dB of detector range before the input to the main seven-stage strip is overloaded. This gives us nine stages, for a theoretical dynamic range of 108dB - in practice, it is possible to achieve about 103-105dB.

When constructing a log strip such as the one described above, there are

various considerations of coupling, decoupling, filter design, and feedback via the detector pins which must be addressed in any successful design. The single stage limiting amplifier building block has a low frequency cutoff of about 10MHz which makes it impossible to use in many lower frequency applications.

Recent advances in IC processes have allowed the complete log strip function to be integrated into a single chip, thereby eliminating the need for costly hybrid log strips.

The AD640 log amp contains five limiting stages (10dB per stage) and five full-wave detectors in a single IC package, and its logarithmic performance extends from dc to 145MHz. Furthermore, its amplifier and full-wave detector stages are balanced so that, with reasonably well-considered layout,

instability from feedback via supply rails is unlikely. A block diagram of the AD640 is shown in Figure 3.19. Unlike all previous integrated circuit log amps, the AD640 is laser trimmed to high absolute accuracy of both slope and

intercept, and is fully temperature compensated. Key features of the AD640 are summarized in Figure 3.20. The transfer function for the AD640 as well as the log linearity is shown in Figure 3.21.

## BLOCK DIAGRAM OF THE AD640 MONOLITHIC LOG AMP

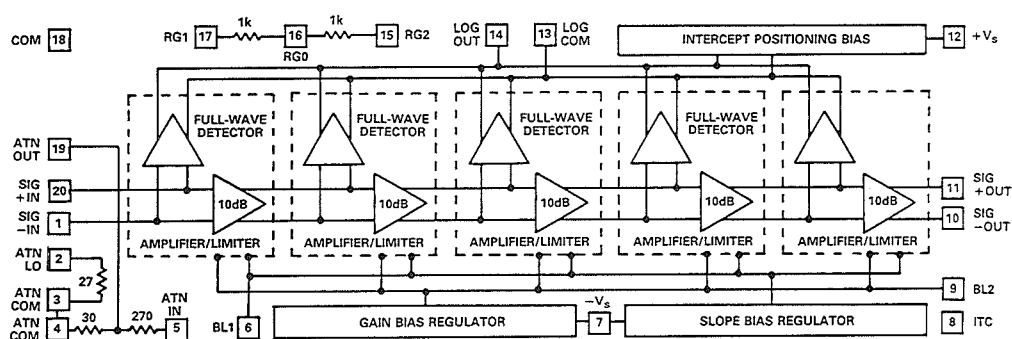


Figure 3.19

## AD640 KEY FEATURES

- 45dB Dynamic Range - Two AD640s Cascadable to 95dB
- Bandwidth dc to 145MHz - 120MHz when Cascaded
- Laser-Trimmed Slope of 1mA/decade - Temperature Stable
- Laser-Trimmed Intercept of 1mV - Temperature Stable
- Less than 1dB Log Non-Linearity
- Balanced Circuitry for Stability
- Minimal External Component Requirement

Figure 3.20

## DC LOGARITHMIC TRANSFER FUNCTION AND ERROR CURVE FOR SINGLE AD640

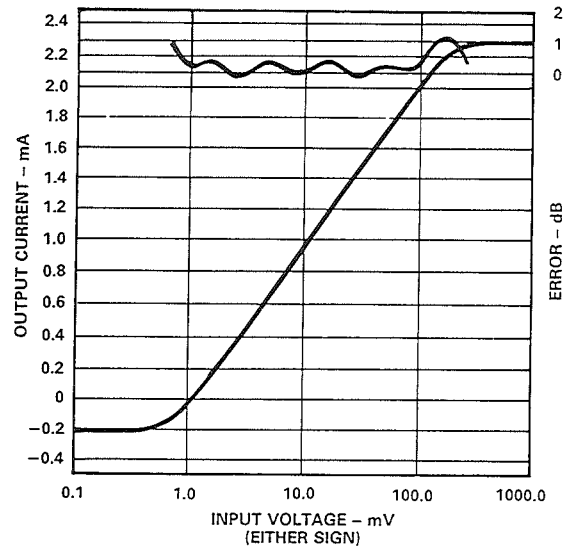


Figure 3.21

Because of its high accuracy, the actual waveform driving the AD640 must be considered when calculating responses. When a waveform passes through a log function generator, the mean value of

the resultant waveform changes. This does not affect the slope of the response, but the apparent intercept is modified according to Figure 3.22.

## THE EFFECT OF WAVEFORM ON INTERCEPT POINT

INPUT WAVEFORM	PEAK OR RMS	INTERCEPT FACTOR	ERROR (RELATIVE TO A DC INPUT)
Square Wave	Either	1	0.00dB
Sine Wave	Peak	2	-6.02dB
Sine Wave	RMS	$1.414 (\sqrt{2})$	-3.01dB
Triwave	Peak	$2.718 (e)$	-8.68dB
Triwave	RMS	$1.569 (e/\sqrt{3})$	-3.91dB
Gaussian Noise	RMS	1.887	-5.52dB

Figure 3.22



The AD640 is calibrated and laser trimmed to give its defined response to a DC level or a symmetrical 2kHz square wave. It is also specified to have an intercept of 2mV for a sinewave input (that is to say a 2kHz sinewave of amplitude 2mV peak [not peak-to-peak] gives the same mean output signal as a DC or square wave signal of 1mV).

The waveform also affects the ripple or nonlinearity of the log response. This ripple is greatest for DC or square wave inputs because every value of the input

voltage maps to a single location on the transfer function, and thus traces out the full nonlinearities of the log response. By contrast, a general time-varying signal has a continuum of values within each cycle of its waveform. The averaged output is thereby "smoothed" because the periodic deviations away from the ideal response, as the waveform "sweeps over" the transfer function, tend to cancel. As is clear in Figure 3.23, this smoothing effect is greatest for a triwave.

## THE EFFECT OF WAVEFORM ON AD640 LOG LINEARITY AND INTERCEPT POINT

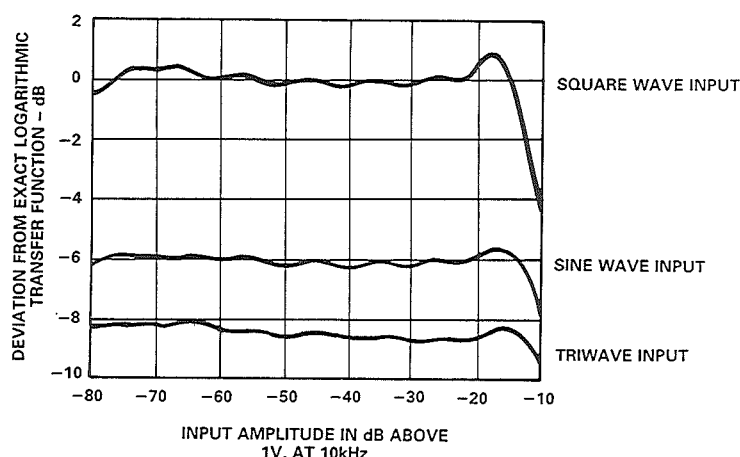


Figure 3.23

Each of the five stages in the AD640 has a gain of 10dB and a full-wave detected output. The transfer function for the device was shown in Figure 3.21 along with the error curve. Note the excellent log linearity over an input range of 1 to 100mV (40dB). Although well suited to RF applications, the AD640 is dc-coupled throughout. This allows it to be used in LF and VLF

systems, including audio measurements, sonar, and other instrumentation applications requiring operation to low frequencies or even dc.

When two AD640s are cascaded, the second will be delivering an output from the noise of the first. If the full potential dynamic range is to be realized, the bandwidth must be limited. This may

be done with high-pass, low-pass, or band-pass filters, depending on the required response, but the voltage gain of these filters in their passband must be unity, or there will be a kink in the log response. Figure 3.24 shows a 70dB log amp for broadband operation from

### 70dB LOG AMP FOR 50-150MHz USING TWO AD640s

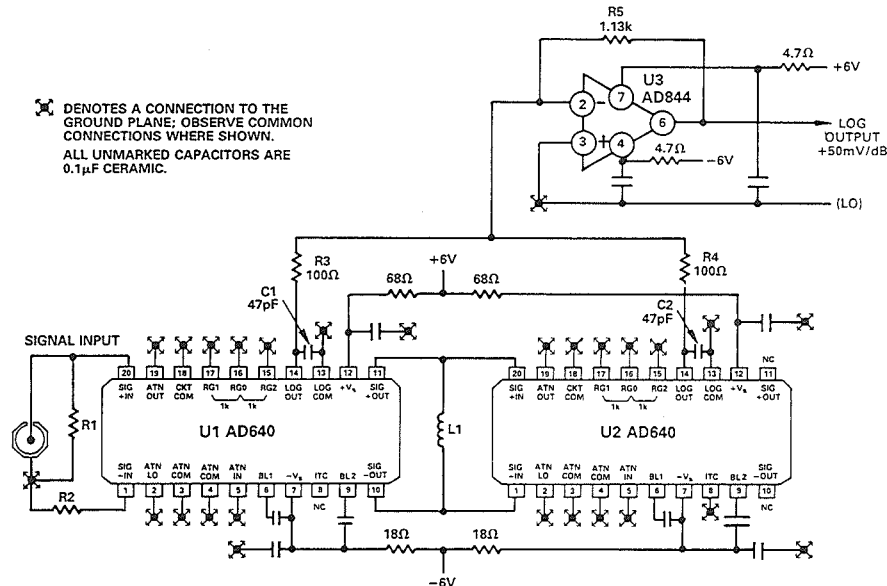


Figure 3.24

### 95dB LOW FREQUENCY LOG AMP (10Hz - 100kHz) USING TWO AD640s

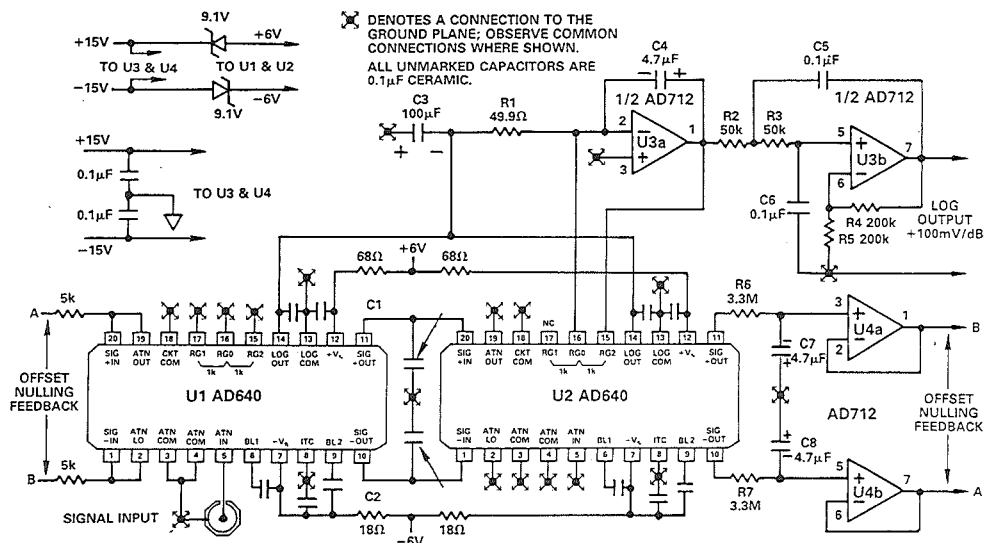


Figure 3.25

An external op amp can be used to convert the AD640 output current to a buffered output voltage as shown in Figure 3.26. The input to the AD640 (1mV to 100mV, or 40dB) results in an op amp output of 0 to 2V. If this output is applied to an 8 bit flash ADC having a corresponding input range, the weight of the ADC least significant bit (LSB) is 0.157dB reflected to the input of the AD640. For input signals near zero, the

LSB value (reflected to the AD640 input) is approximately 0.02mV, while for signals approaching 100mV, the LSB value is approximately 2mV. This corresponds to an effective dynamic range of  $20\log_{10}(100\text{mV}/0.02\text{mV})$ , or 74dB. The 50dB dynamic range of the 8 bit flash converter has therefore been increased to 74dB (equivalent to a 12 bit ADC) through the use of the 40dB AD640 and the op amp.

### OP-AMP CONVERTS CURRENT OUTPUT OF AD640 TO A VOLTAGE FOR DRIVING A FLASH CONVERTER

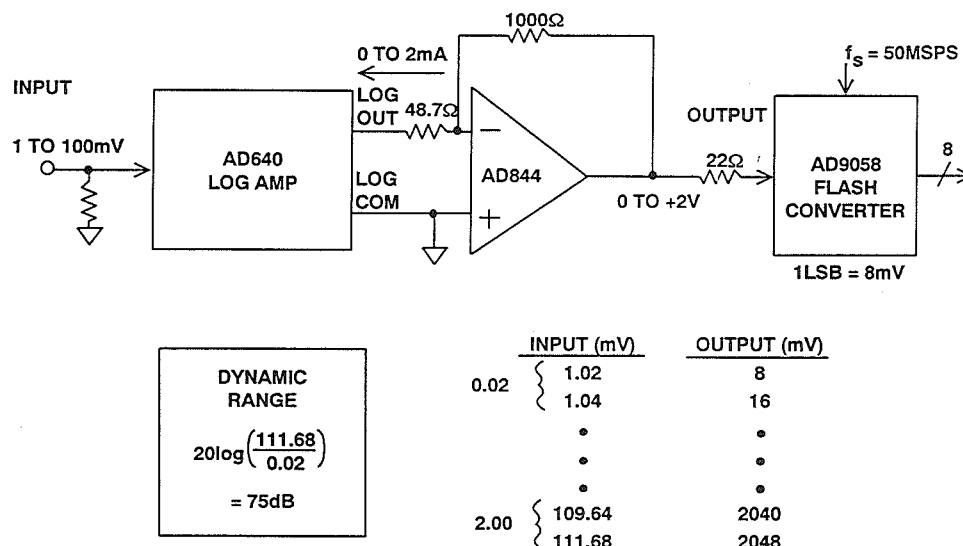


Figure 3.26

The AD606 is a complete monolithic 70MHz bandwidth log amp using 9 stages of successive detection, and is shown in Figure 3.27. Key specifications are summarized in Figure 3.28. Seven of the amplifier/detector stages handle inputs from -80dBm (32μV rms) up to about -14dBm (45mV rms). The noise floor is about -83dBm (18μV rms). Another two parallel stages receive the input attenuated by 22.3dB, and respond to inputs up to +10dBm (707mV rms). The gain of each stage is 11.15dB

and is accurately stabilized over temperature by a precise biasing system.

The AD606 provides both logarithmic and limited outputs. The logarithmic output is from a three-pole post-demodulation lowpass filter and provides an output voltage of +0.1V DC to +4V DC. The logarithmic scaling is such that the output is +0.5V for a sinusoidal input of -75dBm, and +3.5V at an input of +5dBm. Over this range, the log linearity is typically within ±0.4dB.

## AD606 50MHz, 80dB LOG AMP BLOCK DIAGRAM

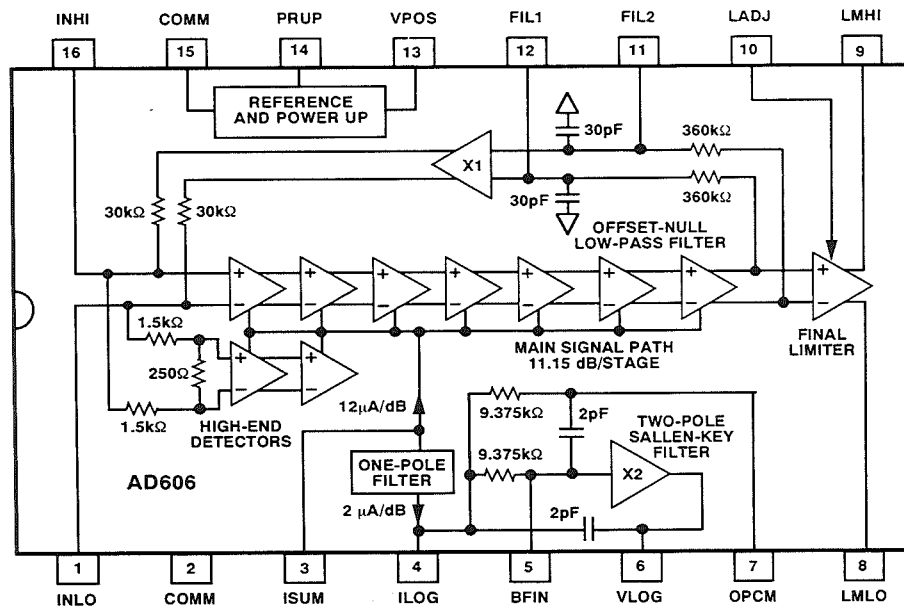


Figure 3.27

## AD606 LOG AMP KEY FEATURES

- Dynamic Range:  $-75\text{dBm}$  to  $+5\text{dBm}$  (80dB)
- Input Noise:  $< 1.5\text{nV}/\sqrt{\text{Hz}}$
- Usable from 200Hz to Greater than 50MHz
- Slope:  $37.5\text{mV/dB}$  Voltage Output
- On-Chip Lowpass Output Filter
- +5V Single-Supply, 65mW Power Consumption

Figure 3.28

The AD606 can operate above and below these limits, with reduced linearity, to provide as much as 90dB of conversion range. A second lowpass filter automatically nulls the input offset of the first stage down to the submicrovolt level.

The AD606's limiter output provides a hard-limited signal output as a differen-

tial current of  $\pm 1.2\text{mA}$  from open-collector outputs. In a typical application, both of these outputs are loaded by  $200\Omega$  resistors to provide a voltage gain of more than 90dB from the input. This limiting amplifier has exceptionally low amplitude-to-phase conversion.

## **ANALOG MULTIPLIERS**

A multiplier is a device having two input ports and an output port. The signal at the output is the product of the two input signals. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor,  $K$ , which has the dimension of voltage (see Figure 3.29). From a mathematical point of view, multiplication is a "four quadrant" operation - that is to say that both inputs may be either positive or negative, as may be the output. Some of the circuits used to produce electronic multipliers, however, are limited to signals of one polarity. If both signals must be unipolar, we have a "single quadrant" multiplier, and the output will also be unipolar. If one of the signals is unipolar, but the other may

have either polarity, the multiplier is a "two quadrant" multiplier, and the output may have either polarity (and is "bipolar"). The circuitry used to produce one- and two-quadrant multipliers may be simpler than that required for four quadrant multipliers, and since there are many applications where full four quadrant multiplication is not required, it is common to find accurate devices which work only in one or two quadrants. An example is the AD539, a wideband dual two-quadrant multiplier which has a single unipolar  $V_y$  input with a relatively limited bandwidth of 5MHz, and two bipolar  $V_x$  inputs, one per multiplier, with bandwidths of 60MHz. A block diagram of the AD539 is shown in Figure 3.31.

## BASIC ANALOG MULTIPLIER

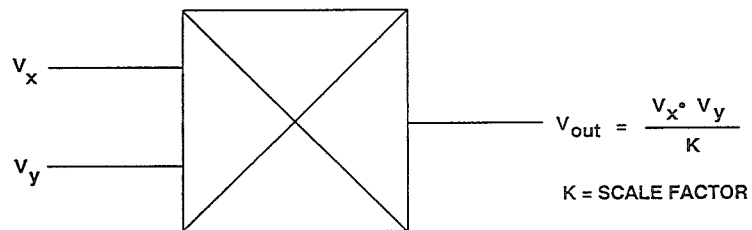


Figure 3.29

## TYPES OF MULTIPLIERS

Type	$V_x$	$V_y$	$V_{out}$
Single Quadrant	Unipolar	Unipolar	Unipolar
Two Quadrant	Bipolar	Unipolar	Bipolar
Four Quadrant	Bipolar	Bipolar	Bipolar

Figure 3.30

## AD539 FUNCTIONAL BLOCK DIAGRAM

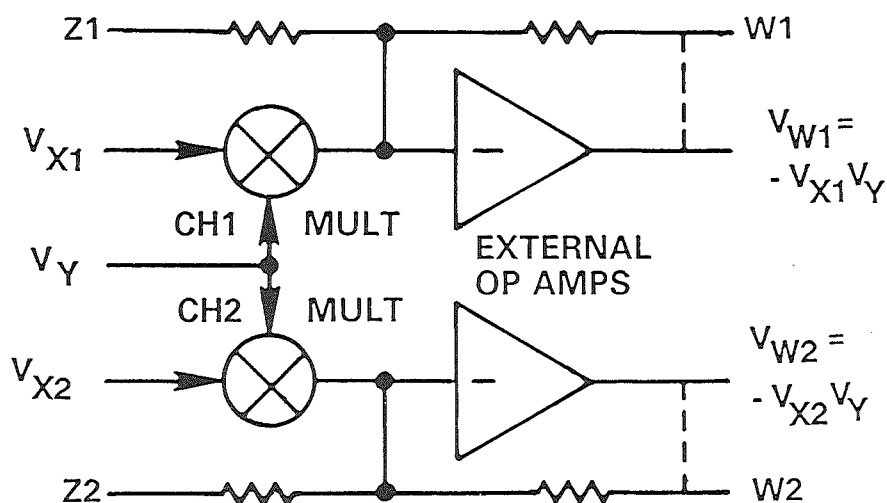


Figure 3.31

The simplest electronic multipliers use logarithmic amplifiers. The computation relies on the fact that the antilog of the

sum of the logs of two numbers is the product of those numbers (see Figure 3.32).

## COMPUTATION WITH LOG AND ANTILOG CIRCUITS

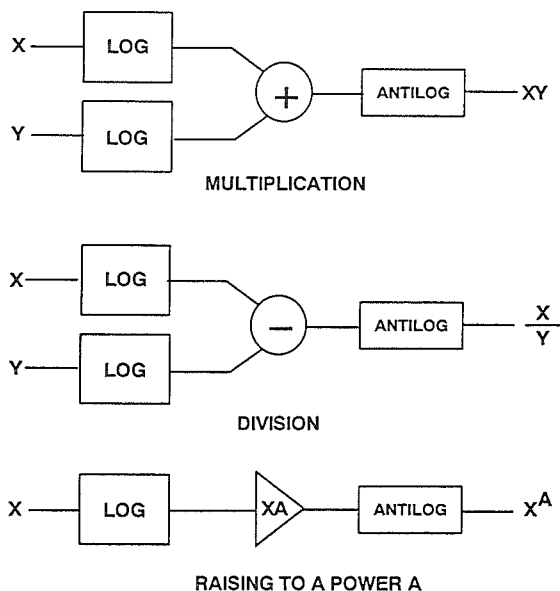


Figure 3.32

The disadvantages of this type of multiplication are the very limited bandwidth and single quadrant operation. A far better type of multiplier uses the "Gilbert Cell". This structure was invented by Barrie Gilbert in the late 1960s. (See References 1 and 2).

There is a linear relationship between the collector current of a silicon junction transistor and its transconductance (gain) which is given by

$$dI_C / dV_{be} = qI_C / kT,$$

where

$I_C$  = the collector current  
 $V_{be}$  = the base-emitter voltage  
 $q$  = the electron charge (1.60219E-19)  
 $k$  = Boltzmann's constant (1.38062E-23)  
 $T$  = the absolute temperature.

This relationship may be exploited to construct a multiplier with a long-tailed pair of silicon transistors, as shown in Figure 3.33.

This is a rather poor multiplier because (1) the Y input is offset by the  $V_{be}$  - which changes non-linearly with  $V_Y$ ; (2) the X input is non-linear as a result of the exponential relationship between  $I_C$  and  $V_{be}$ ; and (3) the scale factor varies with temperature.

Gilbert realized that this circuit could be linearized and made temperature stable by working with currents, rather than voltages, and by exploiting the logarithmic  $I_C/V_{be}$  properties of transistors (See Figure 3.34.) The X input to the Gilbert Cell takes the form of a differential current, and the Y input is a unipolar current. The differential X currents flow in two diode-connected transistors, and the logarithmic voltages compensate for the exponential  $V_{be}/I_C$  relationship. Furthermore, the  $q/kT$  scale factors cancel. This gives the Gilbert Cell the linear transfer function

$$\Delta I_C = \frac{\Delta I_X I_Y}{I_X}$$

## BASIC TRANSCONDUCTANCE MULTIPLIER CIRCUIT

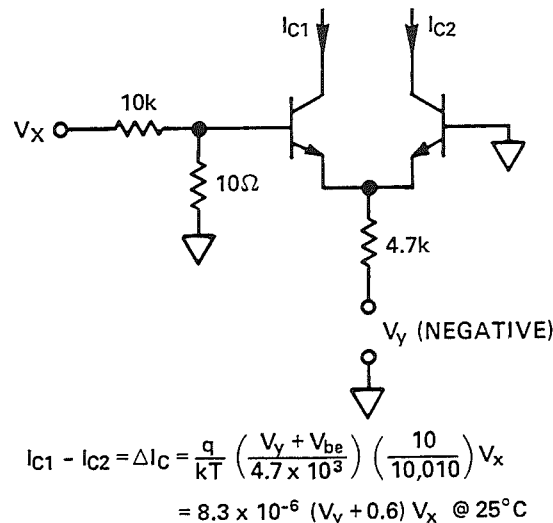
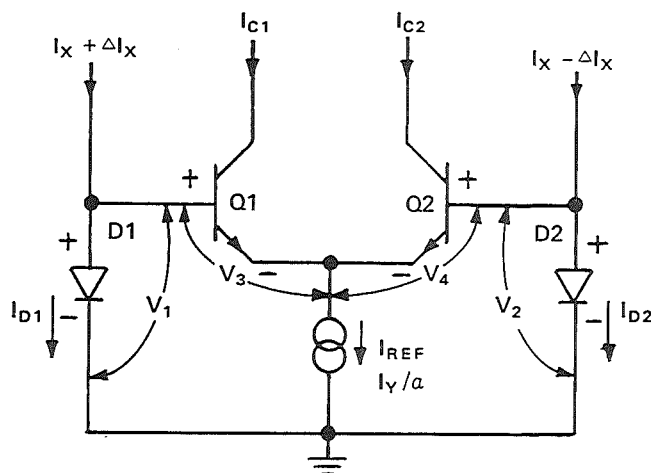


Figure 3.33



## THE GILBERT CELL: A LINEAR TWO-QUADRANT MULTIPLIER

$$\Delta I_C = I_{C1} - I_{C2}$$



$$\Delta I_C = \frac{\Delta I_X I_Y}{I_X}$$

Figure 3.34

As it stands, the Gilbert Cell has three inconvenient features: (1) its X input is a differential current; (2) its output is a differential current; and (3) its Y input is a unipolar current - so the cell is only a two quadrant multiplier.

By cross-coupling two such cells and using two voltage-to-current converters (as shown in Figure 3.35), we can convert the basic architecture to a four

quadrant device with voltage inputs, such as the AD534. At low and medium frequencies, a subtractor amplifier may be used to convert the differential current at the output to a voltage. Because of its voltage output architecture, the bandwidth of the AD534 is only about 1MHz, although the AD734, a later version, has a bandwidth of 10MHz.

## 4-QUADRANT TRANSLINEAR MULTIPLIER: THE AD534

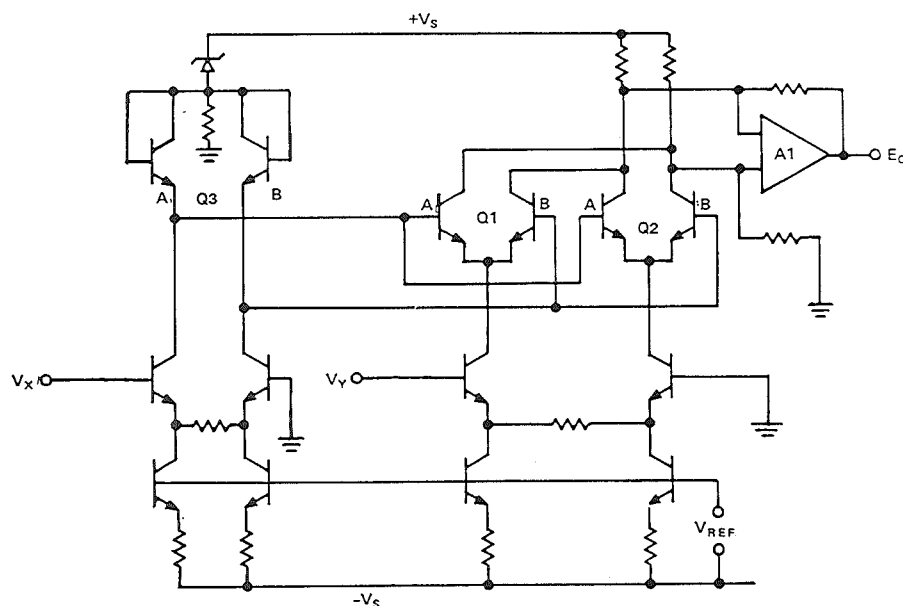


Figure 3.35

In Figure 3.35, Q1A & Q1B, and Q2A & Q2B form the two core long-tailed pairs of the two Gilbert Cells, while Q3A and Q3B are the linearizing transistors for both cells. In Figure 3.35 there is an operational amplifier acting as a differential current to single-ended voltage converter, but for higher speed applications, the cross-coupled collectors of Q1 and Q2 form a differential open collector current output (as in the AD834 500MHz multiplier).

The translinear multiplier relies on the matching of a number of transistors and currents. This is easily accomplished on a monolithic chip. Even the best IC processes have some residual errors,

however, and these show up as four dc error terms in such multipliers (see Figure 3.36). In early Gilbert Cell multipliers, these errors had to be trimmed by means of resistors and potentiometers external to the chip, which was somewhat inconvenient. With modern analog processes, which permit the laser trimming of SiCr thin film resistors on the chip itself, it is possible to trim these errors during manufacture so that the final device has very high accuracy. Internal trimming has the additional advantage that it does not reduce the high frequency performance, as may be the case with external trimpots.

### TRIMMABLE ERRORS IN MULTIPLIERS

- X-Input Offset Voltage:      Y Feedthrough
- Y-Input Offset Voltage:      X Feedthrough
- Z-Input (Output Amplifier)  
    Voltage Offset:              dc Output Offset Voltage
- Resistor Mismatch:          Gain Error

Figure 3.36

### KEY FEATURES OF THE TRANSLINEAR MULTIPLIER

- High Accuracy: Better than 0.1% Possible
- Wide Bandwidth (Over 60MHz Voltage Output, Over 500MHz Current Output)
- Simplicity, Low Cost, and Ease of Use

Figure 3.37

Because the internal structure of the translinear multiplier is necessarily differential, the inputs are usually differential as well (after all, if a single-ended input is required it is not hard to ground one of the inputs). This is not only convenient in allowing common-mode signals to be rejected, it also permits more complex computations to be performed. The AD534 (shown previously in Figure 3.35) is the classic example of a four-quadrant multiplier based on the Gilbert Cell. It has an accuracy of 0.1% in the multiplier mode,

fully differential inputs, and a voltage output. However, as a result of its voltage output architecture, its bandwidth is only about 1MHz.

For wideband applications, the basic multiplier with open collector current outputs is used. The AD834 is an 8-pin device with differential X inputs, differential Y inputs, differential open collector current outputs, and a bandwidth of over 500MHz. A block diagram is shown in Figure 3.38.

### THE AD834 FOUR-QUADRANT 500MHz MULTIPLIER

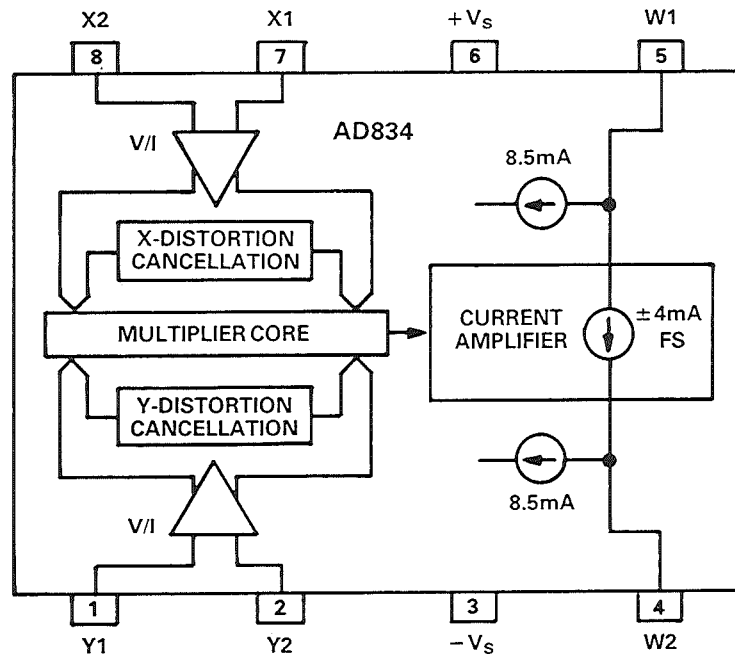


Figure 3.38

The AD834 is a true linear multiplier with a transfer function of

$$I_{out} = \frac{V_x \cdot V_y}{1V \cdot 250\Omega}$$

Its X and Y offsets are trimmed to  $500\mu V$  (3mV max), and it may be used

in a wide variety of applications including multipliers (broadband and narrowband), squarers, frequency doublers, and high frequency power measurement circuits. A consideration when using the AD834 is that, because of its very wide bandwidth, its input bias currents, approximately  $50\mu A$  per input, must be considered in the design

of input circuitry lest, flowing in source resistances, they give rise to unplanned offset voltages.

A basic wideband multiplier using the AD834 is shown in Figure 3.39. The differential output current flows in equal load resistors, R1 and R2, to give a differential voltage output. This is the simplest application circuit for the device. Where only the high frequency outputs are required, transformer coupling may be used, with either

simple transformers, or for better wideband performance, transmission line or "Ruthroff" transformers (See Reference 3).

The AD734 is a 10MHz four-quadrant multiplier with an external input to dynamically change the scale factor, thereby accomplishing a direct-divide function. A functional block diagram of the device is shown in Figure 3.41.

## BASIC CONNECTIONS FOR WIDEBAND AD834 OPERATION

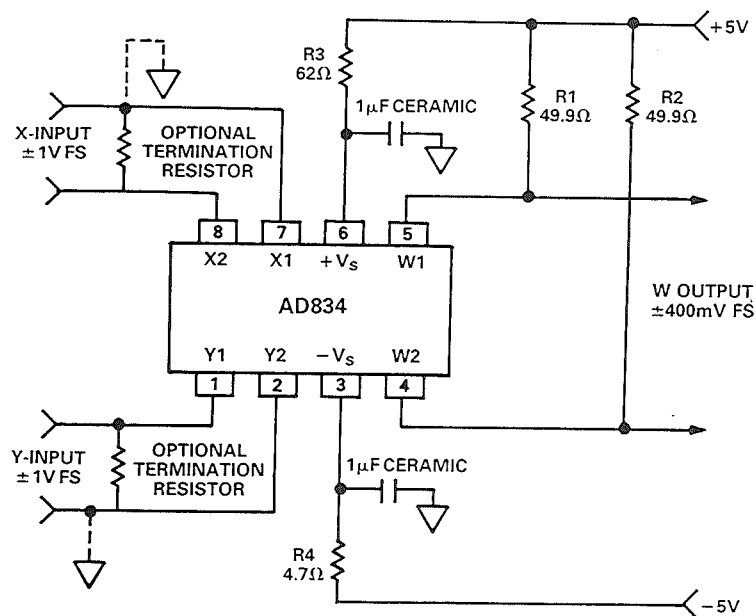


Figure 3.39

### AD834 OPERATION WITH WIDEBAND TRANSFORMER COUPLED OUTPUT

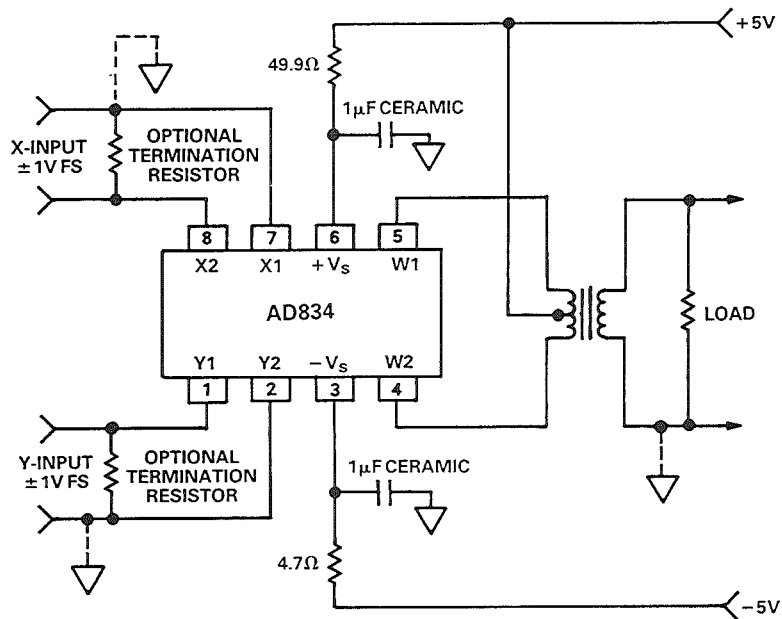
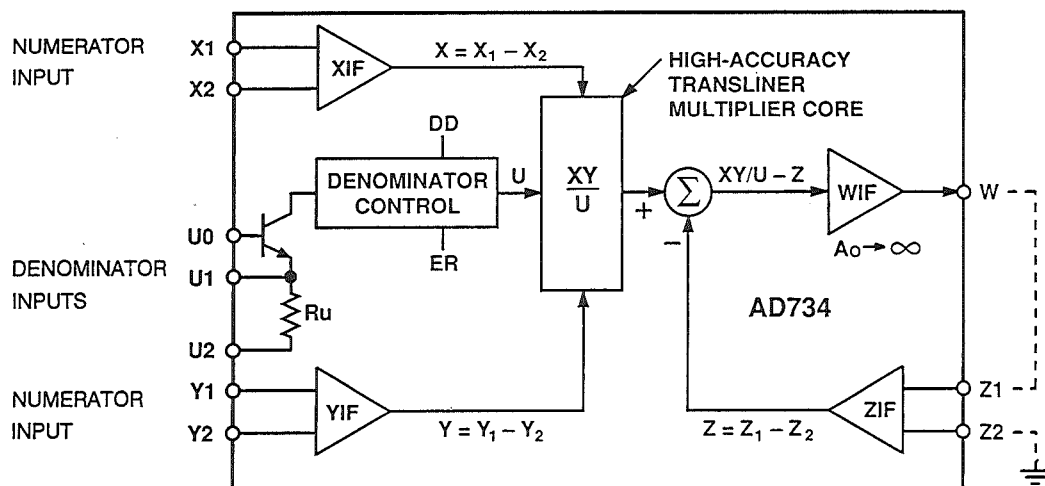


Figure 3.40

### A 10MHz MULTIPLIER WITH DIRECT-DIVIDE CAPABILITY: THE AD734



$$W = \left[ \frac{(X_1 - X_2)(Y_1 - Y_2)}{U_1 - U_2} - (Z_1 - Z_2) \right] A_0$$

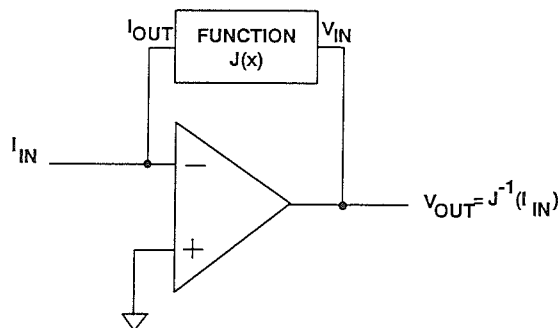
Figure 3.41

Multipliers can be placed in the feedback loop of op amps to form several useful functions. Figure 3.42 illustrates the basic principle of analog computation that a function generator in a negative feedback loop computes the

inverse function (provided, of course, that the function is monotonic over the range of operations).

Figure 3.43 shows a multiplier and an op amp configured as a divider in both inverting and non-inverting mode.

### A FUNCTION GENERATOR IN A NEGATIVE-FEEDBACK LOOP GENERATES THE INVERSE FUNCTION



NOTE: FUNCTION MUST BE MONOTONIC OVER THE RELEVANT RANGE

Figure 3.42

### MULTIPLIERS USED WITH OP-AMPS TO PERFORM DIVISION

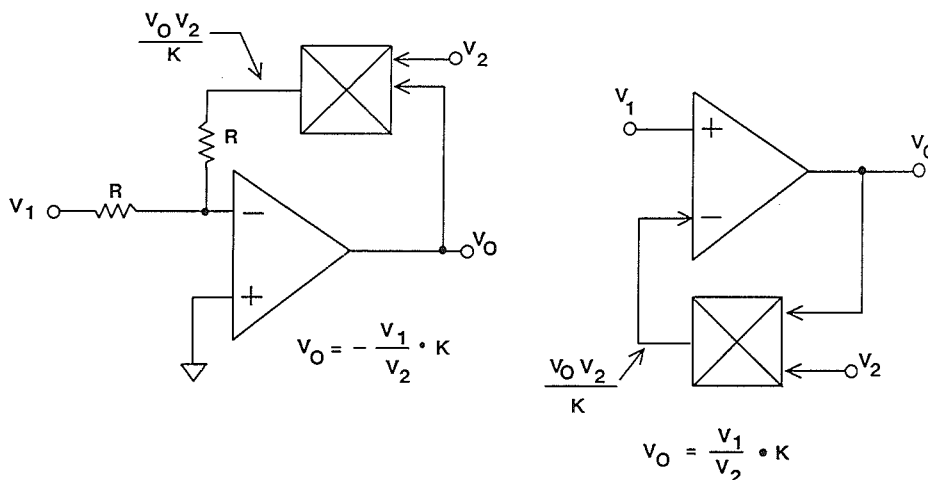


Figure 3.43

## RMS TO DC CONVERTERS

The root mean square (rms) is a fundamental measurement of the magnitude of an ac signal. Defined practically, the rms value assigned to the ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Defined mathematically, the rms value of a voltage is defined as the value obtained by squaring the signal, taking the average, and then taking the square root. The averaging time must be sufficiently long to allow filtering at the lowest frequencies of operation desired. A complete discussion of rms to dc converters can be found in Reference 13, but we will show a few examples of how efficiently analog circuits can perform this function.

The first method, called the *explicit* method, is shown in Figure 3.44. The

input signal is first squared by a multiplier. The average value is then taken by using an appropriate filter, and the square root is taken using an op amp with a second squarer in the feedback loop. This circuit has limited dynamic range because the stages following the squarer must try to deal with a signal that varies enormously in amplitude. This restricts this method to inputs which have a maximum dynamic range of approximately 10:1 (20dB). However, excellent bandwidth (greater than 100MHz) can be achieved with high accuracy if a multiplier such as the AD834 is used as a building block (see Figure 3.45).

3

### EXPLICIT RMS COMPUTATION

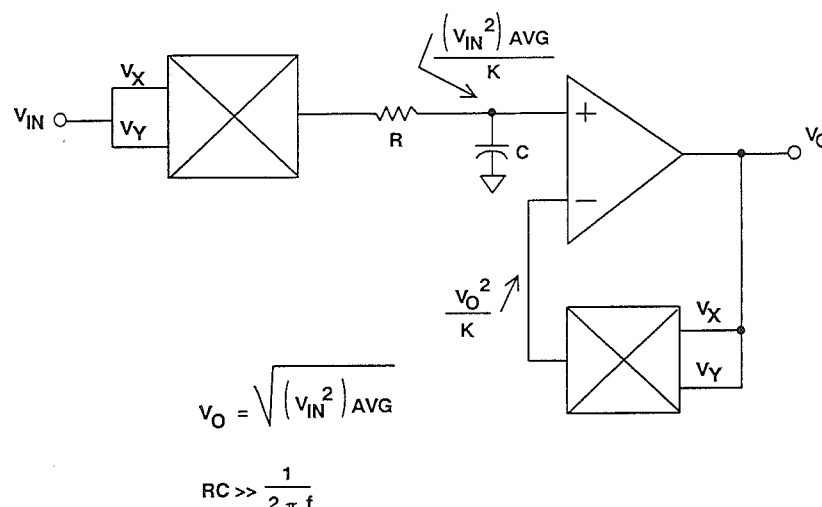


Figure 3.44



# WIDEBAND RMS MEASUREMENT WITH THE AD834

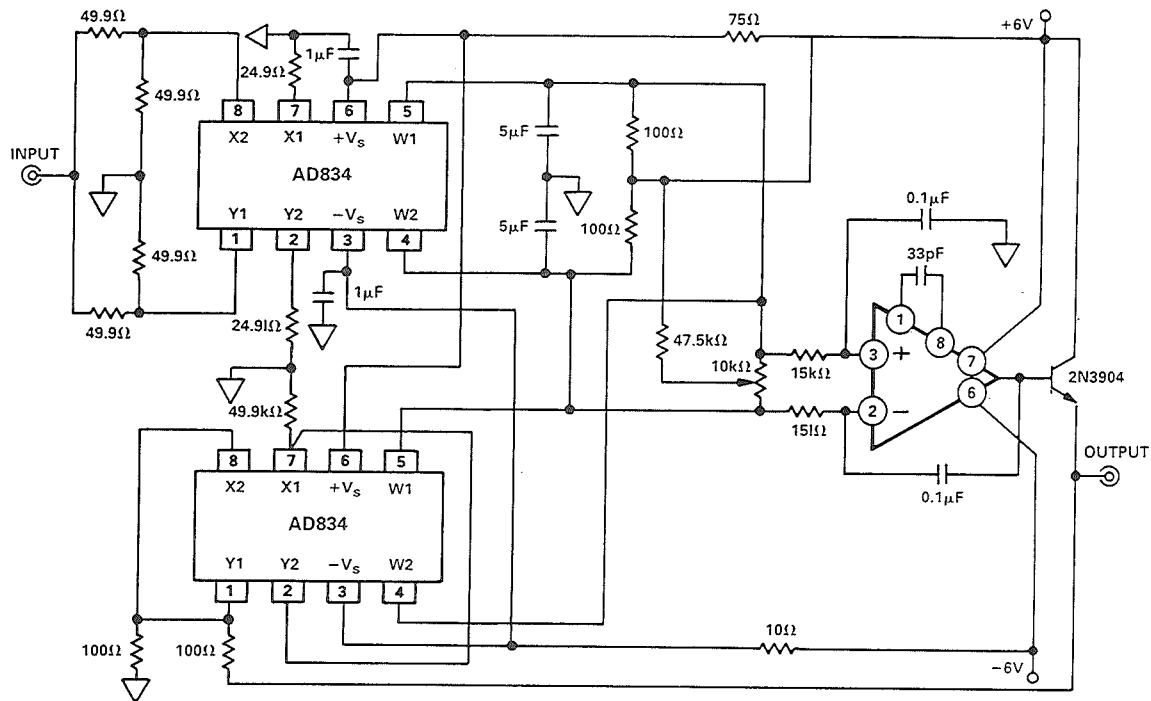


Figure 3.45

Figure 3.46 shows the circuit for computing the rms value of a signal using the *implicit* method. Here, the output is fed back to the direct-divide input of a multiplier such as the AD734. In this circuit, the output of the multiplier varies linearly (instead of as the square)

with the rms value of the input. This considerably increases the dynamic range of the implicit circuit as compared to the explicit circuit. The disadvantage of this approach is that it generally has less bandwidth than the explicit computation.

## IMPLICIT RMS COMPUTATION

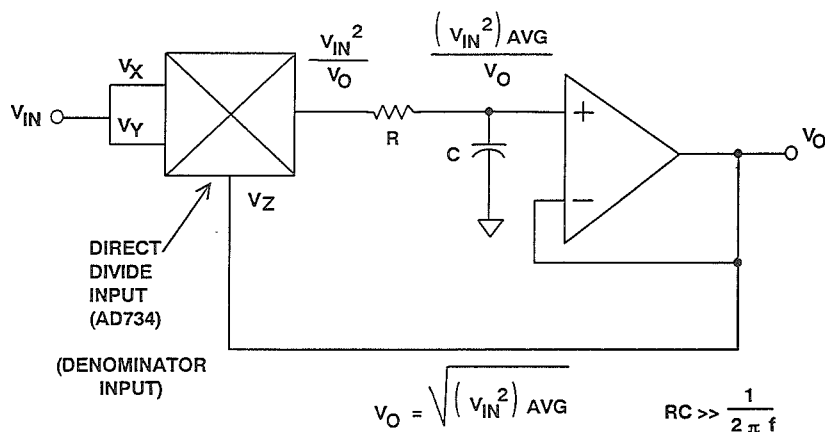


Figure 3.46

While it is possible to construct such an rms circuit from an AD734, it is far simpler to design a dedicated rms circuit. The  $V_{IN}^2/V_Z$  circuit may be current driven and need only be one quadrant if the input first passes through an absolute value circuit.

Figure 3.47 shows a simplified diagram of a typical monolithic RMS/DC converter, the AD536A. It is subdivided into four major sections: absolute value circuit (active rectifier), squarer/divider, current mirror, and buffer amplifier. The input voltage  $V_{IN}$ , which can be AC or DC, is converted to a unipolar current,  $I_1$ , by the absolute value circuit A1, A2.  $I_1$  drives one input of the one-quadrant squarer/divider which has the transfer function:  $I_4 = I_1^2/I_3$ . The output current,  $I_4$ , of the squarer/divider drives the current mirror through a lowpass filter formed by R1 and externally connected capacitor,  $C_{AV}$ . If the  $R1C_{AV}$  time constant is much greater than the longest period of the input signal, then  $I_4$  is effectively

averaged. The current mirror returns a current,  $I_3$ , which equals  $AVG[I_4]$ , back to the squarer/divider to complete the implicit rms computation. Thus:

$$I_4 = AVG [I_1^2/I_4] = I_1 \text{ rms}$$

The current mirror also produces the output current,  $I_{out}$ , which equals  $2I_4$ .  $I_{out}$  can be used directly or converted to a voltage with R2 and buffered by A4 to provide a low impedance voltage output. The transfer function becomes:

$$V_{out} = 2R2 \cdot I_{rms} = V_{IN} \text{ rms}$$

The dB output is derived from the emitter of Q3, since the voltage at this point is proportional to  $-\log V_{IN}$ . Emitter follower, Q5, buffers and level shifts this voltage, so that the dB output voltage is zero when the externally supplied emitter current ( $I_{REF}$ ) to Q5 approximates  $I_3$ . However, the gain of the dB circuit has a TC of approximately 3300ppm/°C and must be temperature compensated.

## THE AD536A MONOLITHIC RMS-TO-DC CONVERTER

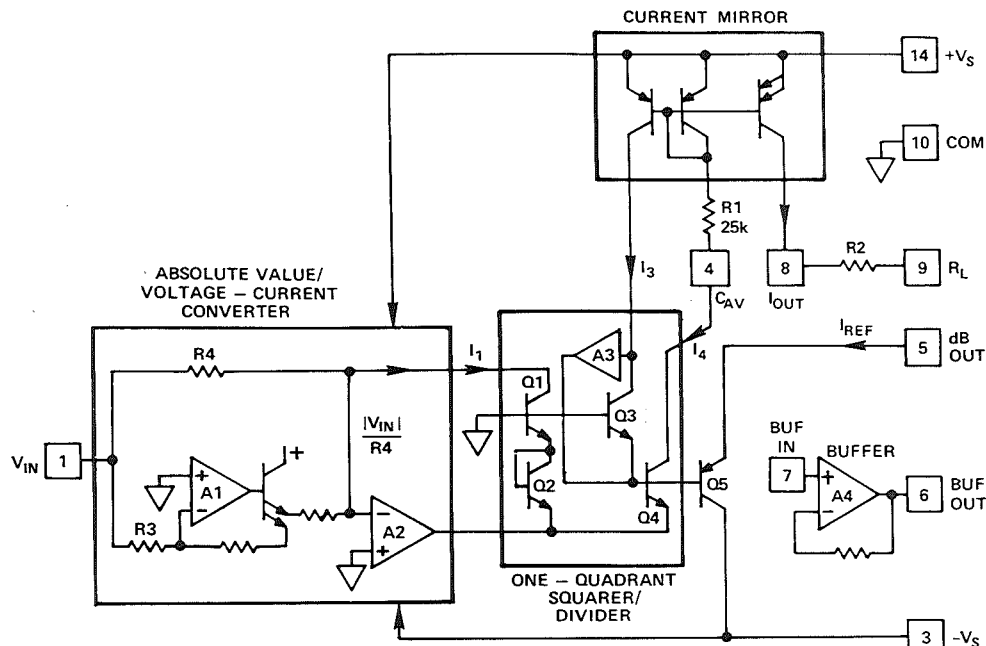


Figure 3.47

There are a number of commercially available RMS/DC converters in monolithic form which make use of these principles. The AD536A is a true RMS/DC converter with a bandwidth of approximately 450kHz for  $V_{\text{rms}} > 100\text{mV rms}$ , and 2MHz bandwidth for  $V_{\text{rms}} > 1\text{V rms}$ . The AD636 is

designed to provide 1MHz bandwidth for low-level signals up to 200mV rms. The AD637 has a 600kHz bandwidth for 100mV rms signals, and an 800MHz bandwidth for 1V rms signals. Low cost, general purpose RMS/DC converters such as the AD736 and AD737 (power-down option) are also available.

## MODULATORS AND MIXERS

A *modulator* (also called a *mixer* when it is used as a frequency changer) is closely related to a multiplier. The output of a multiplier is the instantaneous product of its inputs. The output of a modulator is the instantaneous product of a *signal* on one of its inputs (known as the *signal* input) and the *sign of the signal* on the other input (known as the *carrier* input). A modulator may be modeled as an amplifier whose gain is switched positive and negative by the output of a comparator on its carrier input (as in the case of

the AD630 balanced modulator) - or as a multiplier with a high-gain limiting amplifier between the carrier output and one of its ports (see Figure 3.48). Both architectures have been used to produce modulators, but the switched amplifier version, although potentially very accurate, tends to be rather slow. Most high speed integrated circuit modulators consist of the translinear multiplier (based on the Gilbert Cell) with a limiting amplifier in the carrier path.

### TWO MODULATOR MODELS

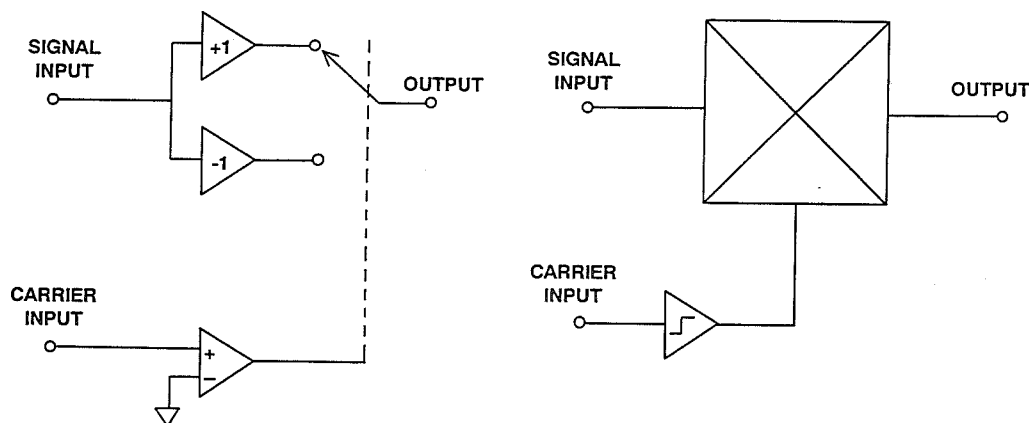


Figure 3.48

If two periodic waveforms,  $A_m \cos(\omega_m t)$  and  $A_c \cos(\omega_c t)$ , are applied to the inputs of a multiplier (with a scale factor of 1V for simplicity of analysis), then the output will be given by:

$$V_o(t) = 1/2 A_m A_c [\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t]$$

This signal contains signals at the sum and difference frequencies, but not at the original frequencies. Some RF engineers also call these the upper and lower *sidebands*. There is a 6dB loss in an ideal modulator. Note that using the cosine formulae rather than sine formulae makes the equations easier to manipulate because  $\cos(a) = \cos(-a)$  (which makes sign unimportant during

simplification), and because  $\cos(0)=1$ , so that for DC signals (when  $\omega_m t=0$ ),  $\cos(\omega_m t)$  is equal to unity.

When we say that the original frequencies are not present in the output of a modulator, we make the assumption that the modulator is perfectly balanced - i.e. neither its signal port nor its carrier port has any offset. In practice, both ports will have some offset, and so there will be some signal and carrier leakage. Trimming offset on the inputs of a modulator will reduce the leakages, but there will always be untrimmable residual leakages which are due to coupling by stray capacitance, and to nonlinearities in the core, rather than to offsets.

## CAUSES OF SIGNAL AND CARRIER LEAKAGE IN MODULATORS

- Offset on the Signal Port Causes Carrier Leakage
- Offset on the Carrier Port Causes Signal Leakage
- Even when all offsets have been trimmed out there is residual signal and carrier leakage caused by stray capacitance and core nonlinearities.

Figure 3.49

This "sum and difference mixer" is the function which we expect of modulators. However, if we use a linear multiplier as a modulator, we find that any noise or modulation on the carrier input appears in the output signal. If we replace the simple multiplier with a modulator, any amplitude variation on the carrier input disappears.

Like an analog multiplier, a modulator multiplies two signals. But unlike analog multipliers, the multiplication is not linear. Instead, the signal input is "chopped" by the local oscillator carrier signal that alternates between +1 and -1 in sign (i.e., a squarewave). This is equivalent to passing the carrier signal  $A_c \cos(\omega_c t)$  through a comparator, or limiting amplifier. The square wave with a frequency of  $\omega_c t$  has the form represented by the Fourier series of odd harmonics:

$$K[\cos(\omega_c t) - 1/3 \cos(3\omega_c t) + 1/5 \cos(5\omega_c t) - 1/7 \cos(7\omega_c t) + \dots]$$

The sum of the series:  $[1, -1/3, +1/5, -1/7 + \dots]$  is  $\pi/4$ . Therefore, the value of  $K$  is  $4/\pi$ , such that a balanced modulator acts as a unity gain amplifier when a positive DC signal is applied to its carrier input.

Therefore, if a modulator is driven by a signal  $A_m \cos(\omega_m t)$  and a carrier  $\cos(\omega_c t)$  (the carrier amplitude is unimportant provided it is great enough to drive the limiting amplifier), then the output will be the product of the signal and the squared carrier above.

The final output is given by:

$$2A_m/\pi[\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t - 1/3\{\cos(\omega_m + 3\omega_c)t + \cos(\omega_m - 3\omega_c)t\} + 1/5\{\cos(\omega_m + 5\omega_c)t + \cos(\omega_m - 5\omega_c)t\} - 1/7\{\cos(\omega_m + 7\omega_c)t + \cos(\omega_m - 7\omega_c)t\} + \dots]$$

This output contains sum and difference frequencies of the signal and carrier, and of the signal and each of the odd harmonics of the carrier (in the ideal, perfectly balanced modulator, products of even harmonics are not present - in real modulators, which have residual offsets on their carrier ports, low-level even harmonic products are also present, just how low their level depends on the size of the offset). In most applications, a filter is used to remove the products of the higher harmonics so that, effectively, the modulator does behave like a multiplier. (In analyzing the above expressions, we must remember that  $\cos(A) = \cos(-A)$ , so that  $\cos(\omega_m - N\omega_c)t = \cos(N\omega_c - \omega_m)t$ , so we do not have to worry about "negative frequencies".) After filtering, the modulator output is given by:

$$2A_m/\pi[\cos(\omega_m + \omega_c)t + \cos(\omega_m - \omega_c)t]$$

Because of the  $2/\pi$  term, a modulator has a minimum 3.92dB insertion loss, in the absence of any gain. (The AD831 has a gain of 3.92dB to provide unity gain from RF to IF).

The most obvious application of a modulator is a *mixer* or *frequency changer*. If we apply an input signal at  $F_1$  and a carrier at  $F_2$  to a modulator, we find that the output contains signals at the sum and difference frequencies as shown in Figure 3.50. This applies even if the signal is a modulated signal containing a number of frequency components.

## THE MODULATOR AS A MIXER (FREQUENCY CHANGER)

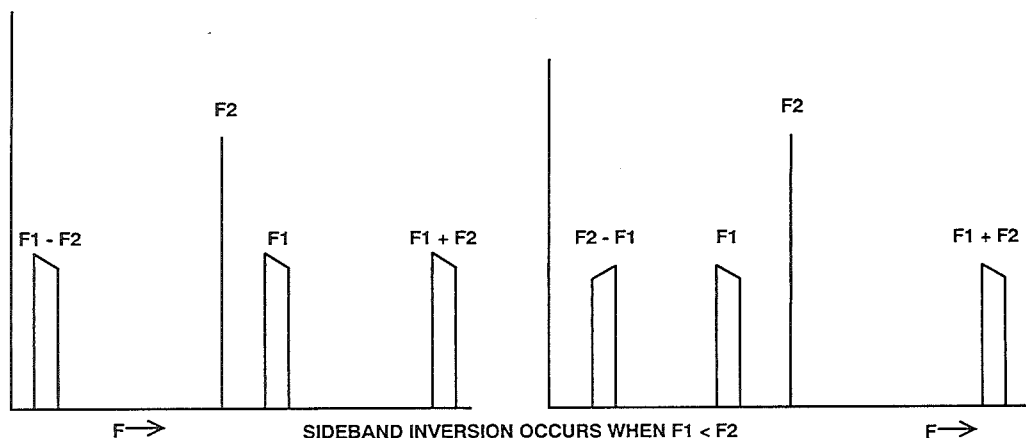


Figure 3.50

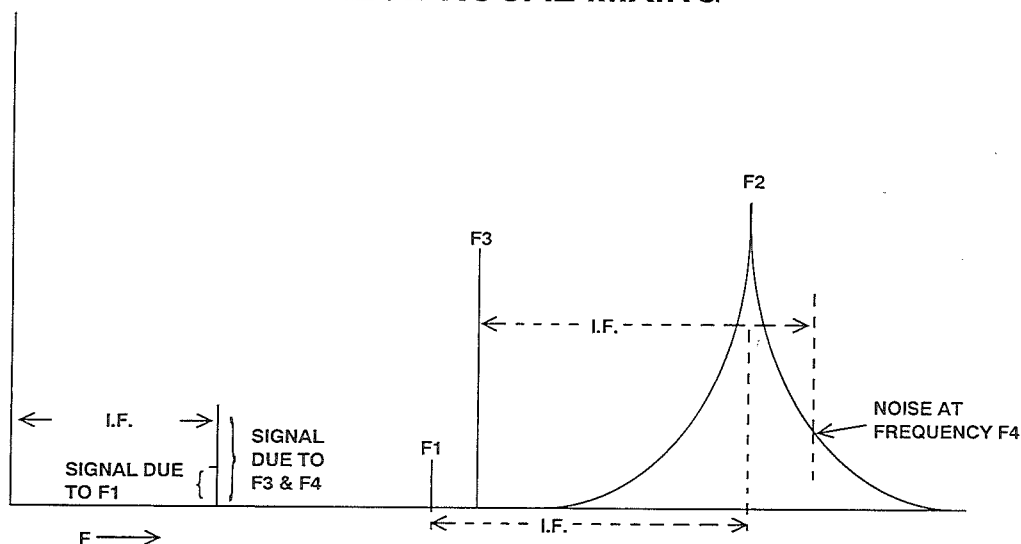
As we have mentioned above, we cannot have “negative frequencies”, and so if  $F_1 - F_2$  is negative, what we actually see is a frequency of  $F_2 - F_1$ . If  $F_1$  is a complex signal containing a number of components, however, we find that if the carrier frequency,  $F_2$ , is less than  $F_1$ , then the sidebands are inverted in both the sum and difference products, but if  $F_2$  is greater than  $F_1$ , then in the difference product, the sidebands are inverted, as shown in the diagram.

The *mixer*, or frequency changer, is a key component in most radio receivers. While it is inappropriate to go into a detailed discussion of receiver design in this section, it is perhaps useful to point out two important features of modulators for use in receivers. These are *noise* and *strong signal performance* (see References 4 and 5).

Suppose that we have a mixer with a noisy carrier channel which causes the

carrier frequency,  $F_2$ , to spread out on either side of its center as shown in Figure 3.51. If we are receiving a small wanted signal,  $F_1$ , then we shall see a small IF output from the mixer at  $F_2 - F_1$ . If, however, there is a strong unwanted signal at  $F_3$ , then the product,  $F_4 - F_3$ , of  $F_3$  and that part of the broadband carrier noise indicated by  $F_4$  on the diagram, will also fall at the IF and, being larger than the wanted IF component, will swamp it. This phenomenon is known as *reciprocal mixing*, and can cause severe limitation on the dynamic range of a receiver. While it is probably more commonly caused by noise or spurious synthesizer sidebands in the oscillator driving the modulator carrier port, it is common for it to be caused by noise in the modulator itself, and it should certainly be considered when choosing a mixer for radio receiver (see Reference 6).

## RECIPROCAL MIXING



NOTE: NOISE ON THE CARRIER PORT CAUSES UNWANTED RESPONSES

Figure 3.51

In the past, the sensitivity of a radio receiver has been one of its most important features. Today, while sensitivity is still important, the behavior of the receiver in the presence of strong signals is equally important. The characteristic chosen as a measure of a mixer's performance in this respect is its *third order intermodulation* performance. The key specification is the *third order intercept point*.

Consider a nonlinear amplifier with two large input signals, at  $F1$  and  $F2$  as

shown in Figure 3.52. The nonlinearity gives rise to additional output components at  $F1+F2$  and  $F1-F2$ : these are known as *second order intermodulation products*. These second order products mix with the original signals and produce *third order intermodulation products* at frequencies  $2F1-F2$  and  $2F2-F1$ .

## SECOND AND THIRD-ORDER INTERMODULATION PRODUCTS FOR $f_1 = 5\text{MHz}$ , $f_2 = 6\text{MHz}$

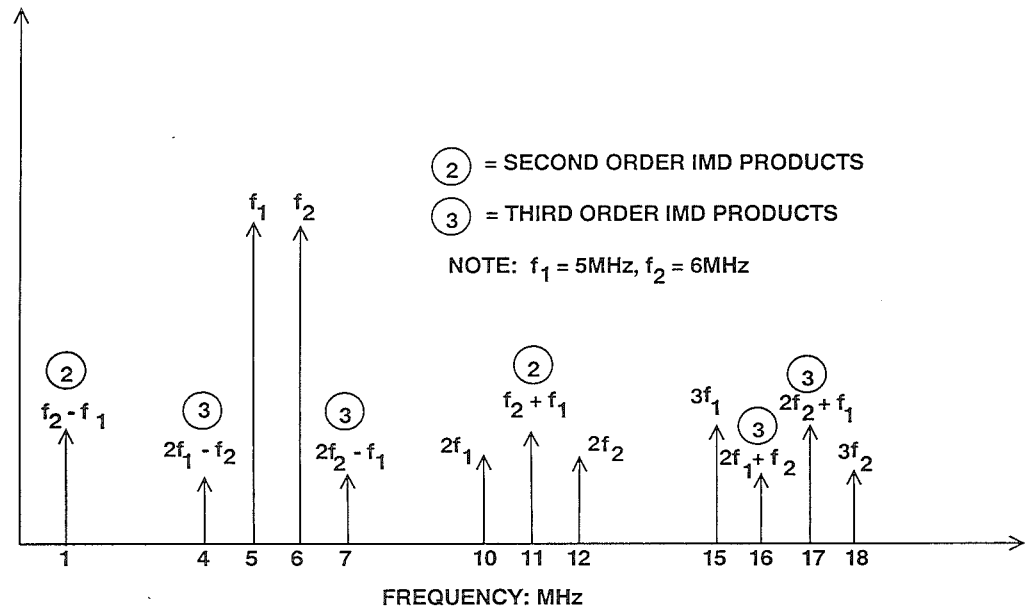


Figure 3.52

The third order intermodulation products are a major nuisance in radio reception, especially in channelized systems, because they fall close to the signals causing them. As an example, consider a receiver monitoring a frequency of 145.5000MHz. In Europe, this frequency is the calling frequency of the 2 meter Amateur Band. Working channels in this band are separated by 25kHz. Suppose that there are two transmitters working at 145.400 and 145.450 MHz respectively. The third order IMD products of these two frequencies fall at 145.350 and 145.500MHz. If the receiver is liable to third order IMD, it will respond to the third order products - which it itself produces - and appear to be receiving a signal at 145.500MHz.

It is impossible to design an amplifier or mixer which is unaffected by third order intermodulation. All that can be done is

to minimize the problem. The third order intercept point mentioned above is the parameter which measures how susceptible a device is to third order IMD.

If we plot the input versus the output amplitudes of an amplifier on a log/log (dB/dB) scale as shown in Figure 3.53, we obtain a straight line slope of unity. At a certain input level, the device saturates, and the output ceases to rise. A measure of this saturation point is known as the *1dB compression point*. If we plot the level of the second order IMD products in the output against the level of a two-tone input on the same axes, we obtain a straight line with a slope of 2. This line also ceases to rise when it reaches some limit. If, however, we extend the two straight lines past their limiting values, they will eventually cross. The value of the power in one of the two-tone inputs at this "inter-



cept point" is the *second order intercept point* of the device or system being measured. The level of the third order IMD products can also be plotted as a function of input, and the slope of the

straight line is 3. The intersection of this line with the extension of the unity-slope line is known as the *third order intercept point*.

## INTERCEPT POINTS, GAIN COMPRESSION, AND IMD

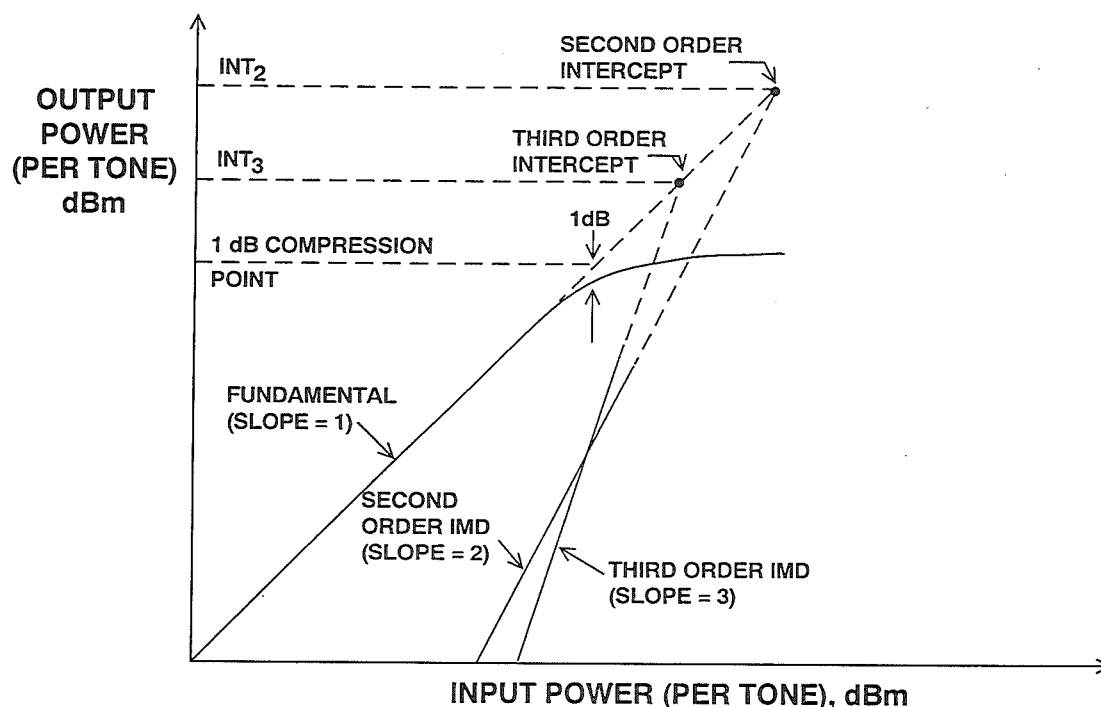


Figure 3.53

In mixers for receivers, values of third order intercept point can vary from  $-15\text{dBm}$  to over  $+45\text{dBm}$ . Any value below  $0\text{dBm}$  is generally considered poor, and good performance requires values of at least  $+15\text{dBm}$  and, preferably, more. The second-order intercept point may also be specified, but it is generally of less concern.

The AD831 is a low distortion, wide dynamic range, monolithic mixer for use in such applications as RF to IF down conversion in HF and VHF receivers, the second mixer in digital mobile radio base stations, direct-to-baseband conversion, quadrature modulation and

demodulation, and doppler-frequency shift detection in ultrasound imaging applications. The mixer includes a local oscillator driver and a low-noise output amplifier. The AD831 provides a  $+24\text{dBm}$  third-order intercept point for  $-10\text{dBm}$  local oscillator power, thus improving system performance and reducing system cost, compared to passive mixers, by eliminating the need for a high power local oscillator driver and its associated shielding and isolation problems. A simplified block diagram of the AD831 is shown in Figure 3.54, and key specifications in Figure 3.55.

## THE AD831 LOW DISTORTION MIXER

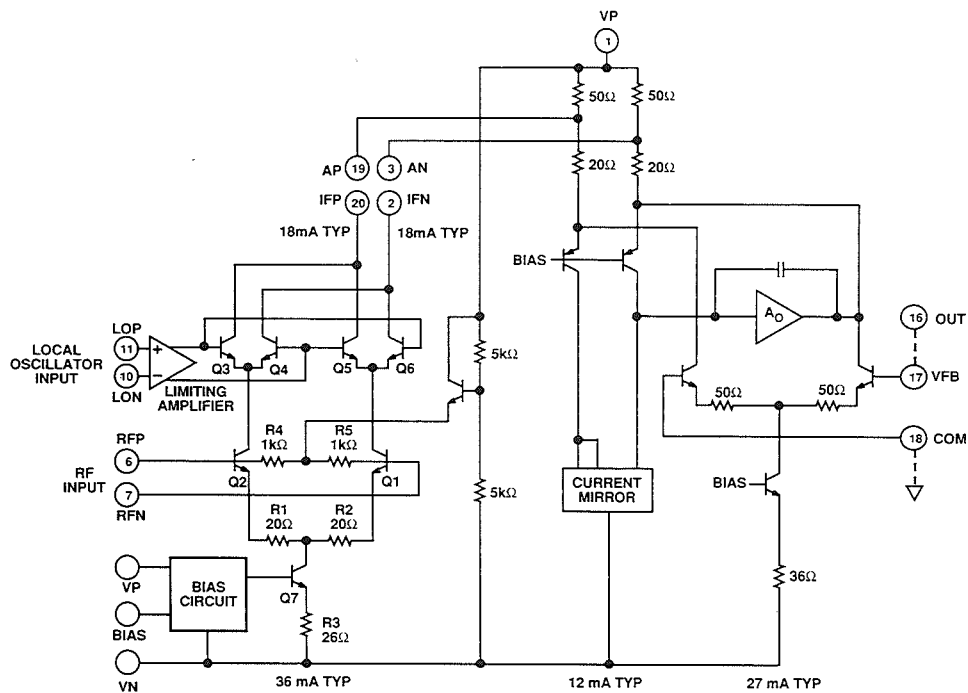


Figure 3.54

## AD831 MIXER KEY FEATURES

- **Doubly-Balanced Mixer**
- **Low Distortion:**
  - ◆ +24dBm Third Order Intercept
  - ◆ +10dBm 1dB Compression Point
- **Low LO Drive Required: -10dBm**
- **Bandwidth:**
  - ◆ 500MHz RF and LO Input Bandwidths
  - ◆ 250MHz Differential Current IF Output
  - ◆ DC to > 200MHz Single-Ended Voltage IF Output

Figure 3.55

The basic mixing property of modulators is also used for many operations where dynamic range is far less important. These include frequency synthesis by mixing, frequency changing with fixed level signals, and sideband generation.

One application worth considering is using a modulator as a precision rectifier.

If an AC signal is applied to both inputs of a modulator as shown in Figure 3.56, the instantaneous output will be equal to the input, if the input is positive, and to the inverse of the input (and therefore still positive), if the input is negative. This arrangement, therefore, behaves as a precision rectifier.

## A MODULATOR USED AS A PRECISION RECTIFIER

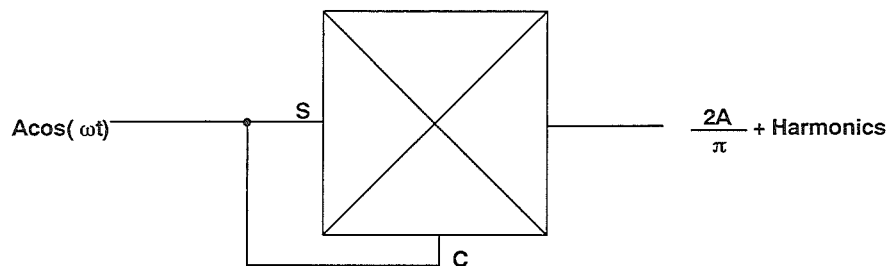


Figure 3.56

If, instead of applying a signal to both ports of a modulator, a signal is applied to the signal port and a reference signal at the same frequency (but not necessarily the same phase) to the carrier port, then the output will be propor-

tional both to the amplitude of the signal input and the cosine of their phase difference. In this mode a modulator acts as a phase-sensitive rectifier (see Figure 3.57).

## A MODULATOR USED AS A PHASE-SENSITIVE RECTIFIER

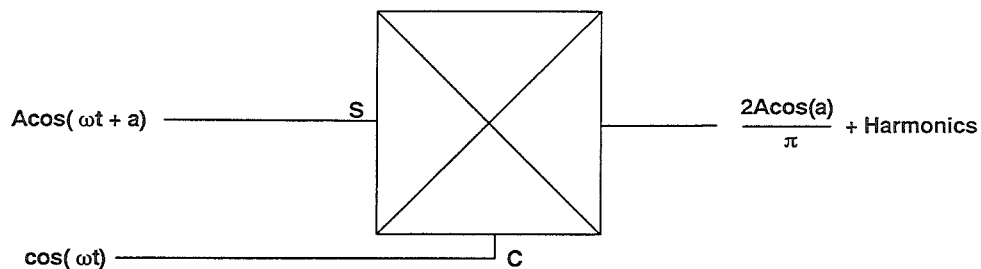


Figure 3.57

## AUTOMATIC GAIN CONTROL (AGC) AND VOLTAGE-CONTROLLED AMPLIFIERS (VCAs)

In radio systems, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic-range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1MHz carrier modulated at 1kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0dBm or -120dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations.

AGC circuits are dynamic-range compressors which respond to some metric of the signal – often its mean amplitude – acquired over an interval corresponding to many periods of the carrier. Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since impulsive noise can now activate the AGC detection circuits. Nonlinear filtering and the concept of “delayed AGC” can be useful in optimizing an AGC system. Many tradeoffs are found in practice; Figure 3.58 shows a basic system.

## A TYPICAL AUTOMATIC GAIN CONTROL (AGC) SYSTEM)

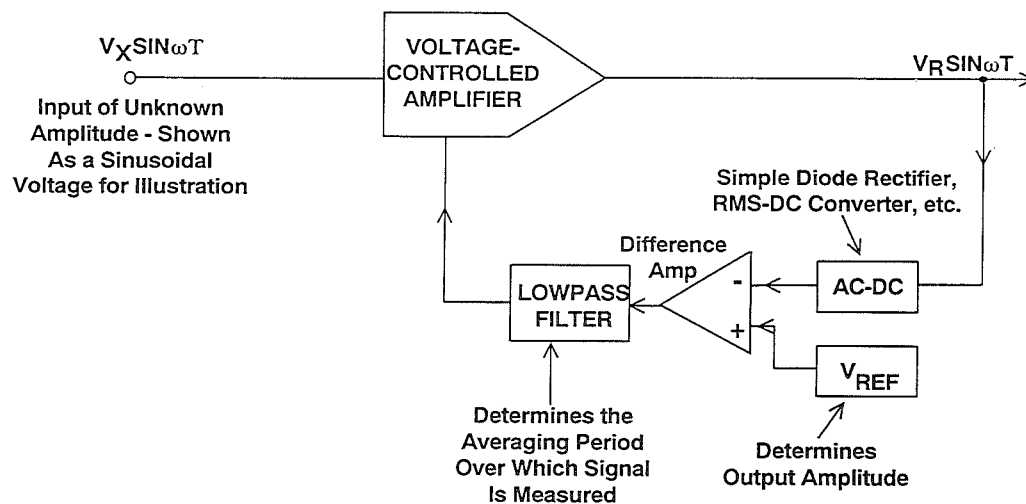


Figure 3.58

It is interesting to note that an AGC loop actually has two outputs. The obvious output is the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA, which is

in reality, a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal.

## VOLTAGE CONTROLLED AMPLIFIERS (VCAs)

A multiplier can be used as a variable-gain amplifier as shown in Figure 3.59. The control voltage is applied to one input, and the signal to the other. The AD539 two-quadrant multiplier (60MHz bandwidth) and the AD844 current feedback amplifier can be used in a 20MHz variable gain amplifier configuration (Figure 3.60). The frequency response of the variable gain amplifier for gains of +4 to -46dB, as

well as the transient response, is shown in Figure 3.61. A current feedback (or transimpedance) amplifier is ideally suited for this application, since its bandwidth remains relatively constant over a wide range of closed-loop gains. In this configuration, the gain is directly proportional to the control voltage. The transfer function of the circuit is

$$V_w = -\frac{V_x V_y}{2V}$$

3

### USING A MULTIPLIER AS A VOLTAGE-CONTROLLED-AMPLIFIER (VCA)

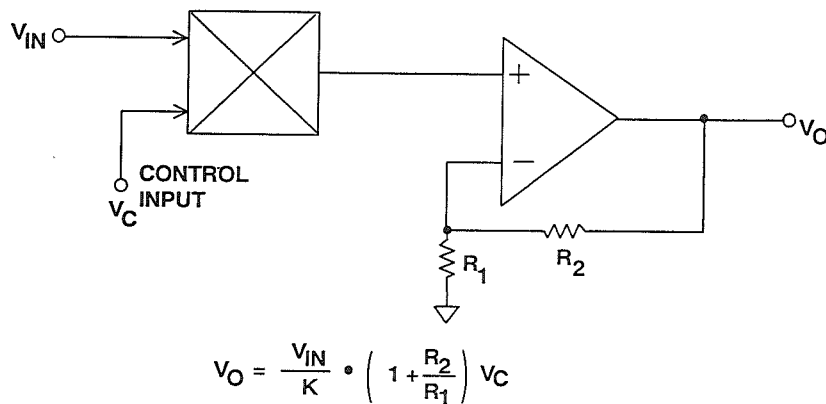


Figure 3.59

# A 20MHz VCA USING THE AD539 MULTIPLIER AND THE AD844 CURRENT FEEDBACK OP AMP

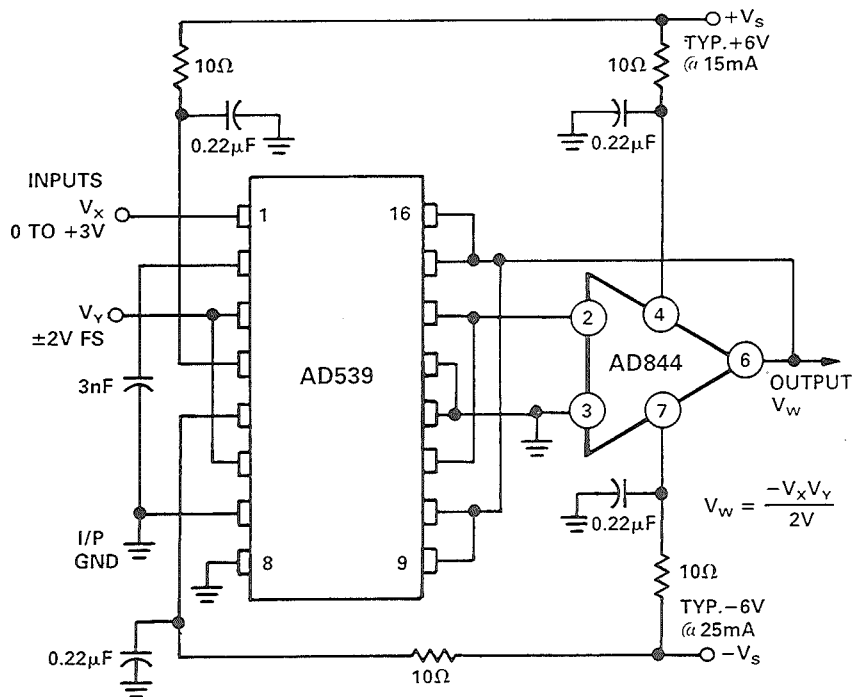
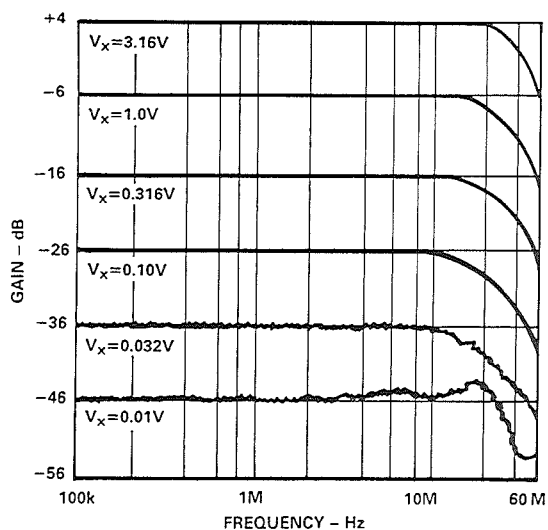
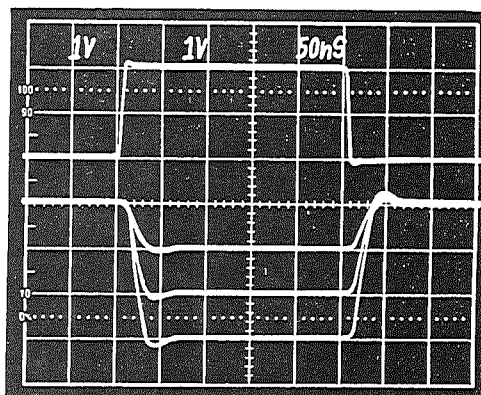


Figure 3.60

## FREQUENCY AND TRANSIENT RESPONSE OF THE 20MHz VCA



VGA ac Response



VGA Transient Response with  $V_x = 1V, 2V, \text{ and } 3V$

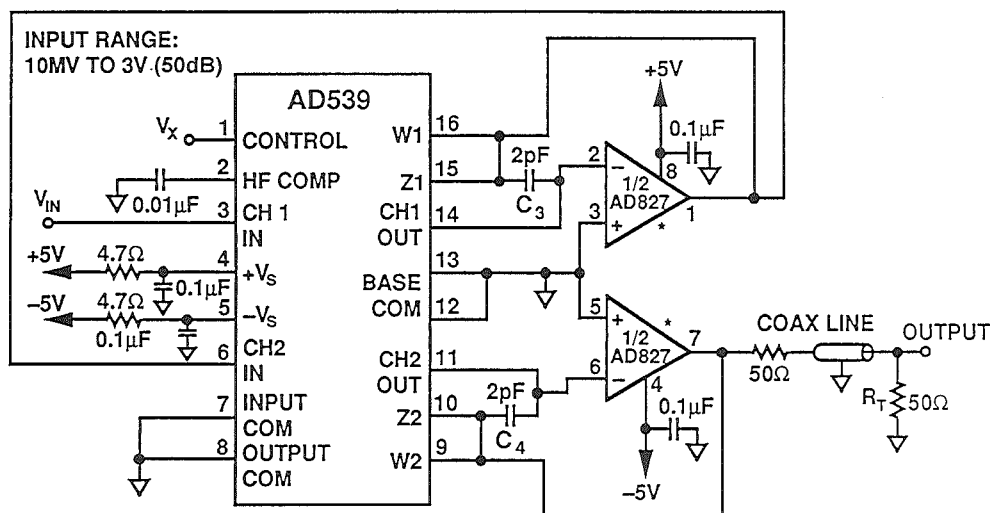
Figure 3.61

In Figure 3.62, the AD827 dual high-speed op-amp is used to provide output current-to-voltage conversion, and the two sections of the AD539 multiplier are connected in series to provide a VCA with a square-law response. The trans-

fer function of this circuit (measured at the reverse-terminated load) is

$$\frac{V_{out}}{V_{in}} = \frac{V_x^2}{8V^2}$$

### AN 8MHz VCA WITH SQUARE-LAW GAIN CONTROL USING THE AD539 MULTIPLIER



\*PINOUT SHOWN IS FOR MINI-DIP PACKAGE

$$V_{out} \text{ AT TERMINATION RESISTOR, } R_T = V_x^2 V_{in} / 8V^2$$

$$V_{out} \text{ AT PIN 7 OF AD827} = V_x^2 V_{in} / 4V^2$$

Figure 3.62

Alternately, the two sections of the AD539 may be operated in parallel with linear gain control. The frequency response of this circuit is about 8MHz using the AD827 op amp. The AD811 high-speed op amp may be substituted in these circuits for increased performance.

Faster op-amps and faster multipliers may be used to achieve higher bandwidth VCAs. A 90MHz VCA is shown in Figure 3.63. The AD834's outputs are in the form of differential currents from a

pair of open collectors, ensuring that the full bandwidth of the multiplier (which exceeds 500MHz) is available. In this case, more moderate bandwidth is obtained using current-to-voltage conversion provided by the AD811 op amp, to realize a practical amplifier with a single-ended, ground-referenced output. Using feedback resistors R8 and R9 of 511Ω, the overall gain ranges from -70dB for  $V_G \sim 0$  to +12dB (a numerical gain of four) when  $V_G = +1V$ . The frequency response for the VCA is shown in Figure 3.64.



## A 90MHz VCA USING THE 500MHz AD834 MULTIPLIER AND THE AD811 OP AMP PROVIDES 80dB DYNAMIC RANGE

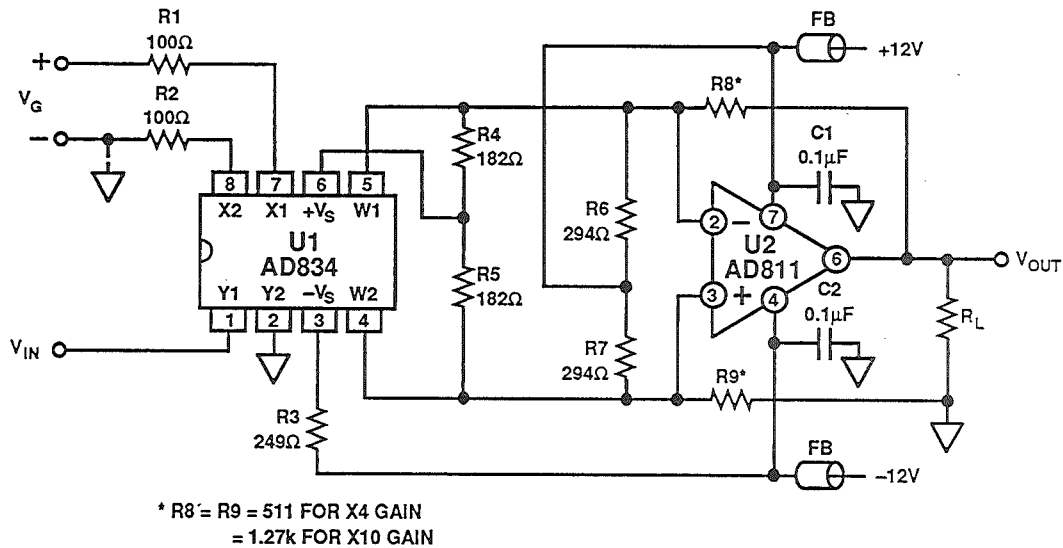


Figure 3.63

## FREQUENCY RESPONSE OF THE 90MHz VCA FOR MAXIMUM GAINS OF +12dB AND +20dB

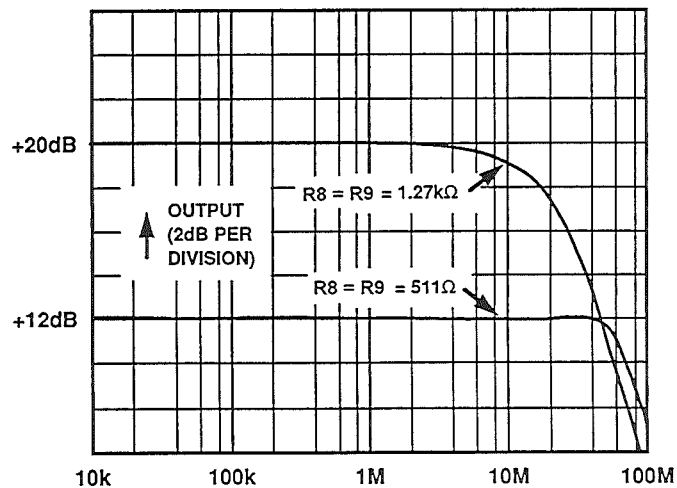


Figure 3.64

Most VCAs made with analog multipliers have gain which is *linear in volts* with respect to the control voltage, moreover they tend to be noisy. There is a demand, however, for a VCA which combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, and AD603 achieve these demanding and conflicting objectives with a unique and elegant solution - the X-AMP™ (for *exponential amplifier*). The concept is simple: a fixed-gain

amplifier follows a passive, broadband attenuator equipped with special means to alter its attenuation under the control of a voltage (see Figure 3.65). The amplifier is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (about 30 to 40dB) and minimize distortion. Since this amplifier's gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay; since its gain is high, its input is never driven beyond a few millivolts. Therefore, it is always operating within its small signal response range.

### SINGLE CHANNEL OF THE DUAL 30MHz AD600/AD602 X-AMP

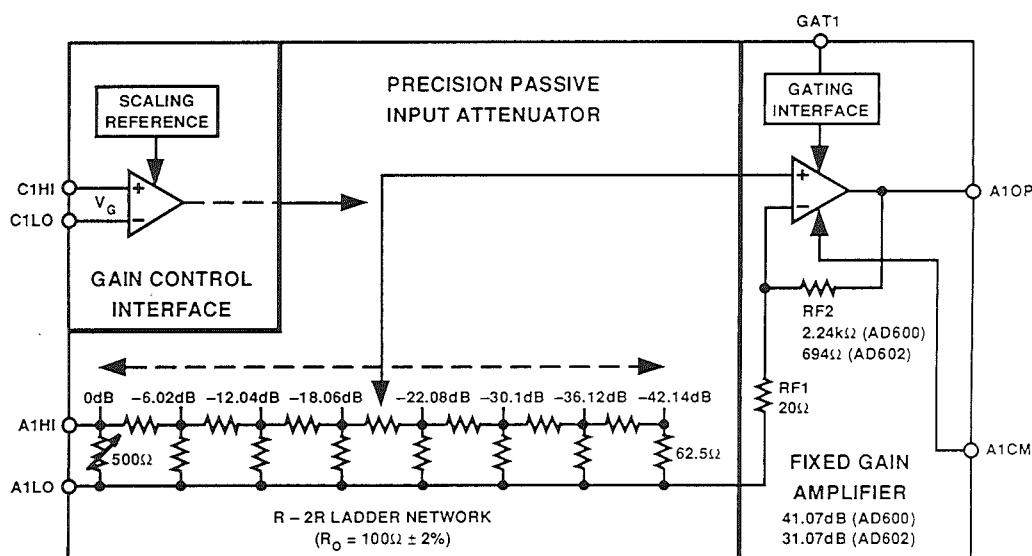


Figure 3.65

The attenuator is a 7-section (8-tap) R-2R ladder network. The voltage ratio between all adjacent taps is exactly 2, or 6.02dB. This provides the basis for the precise linear-in-dB behavior. The overall attenuation is 42.14dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about  $\pm 0.2\text{dB}$ . The overall gain can be varied all the way from the fixed (maximum) gain to a value 42.14dB less. For example, in the AD600, the fixed gain is 41.07dB (a voltage gain of 113); using this choice, the full gain range is  $-1.07\text{dB}$  to  $+41.07\text{dB}$ . The gain is

related to the control voltage by the relationship  $G_{\text{dB}} = 32V_G + 20$  where  $V_G$  is in volts. For the AD602, the fixed gain is 31.07dB (a voltage gain of 35.8), and the gain is given by  $G_{\text{dB}} = 32V_G + 10$ .

The gain at  $V_G = 0$  is laser trimmed to an absolute accuracy of  $\pm 0.2\text{dB}$ . The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 3.66 shows the gain versus the differential control voltage for both the AD600 and the AD602.

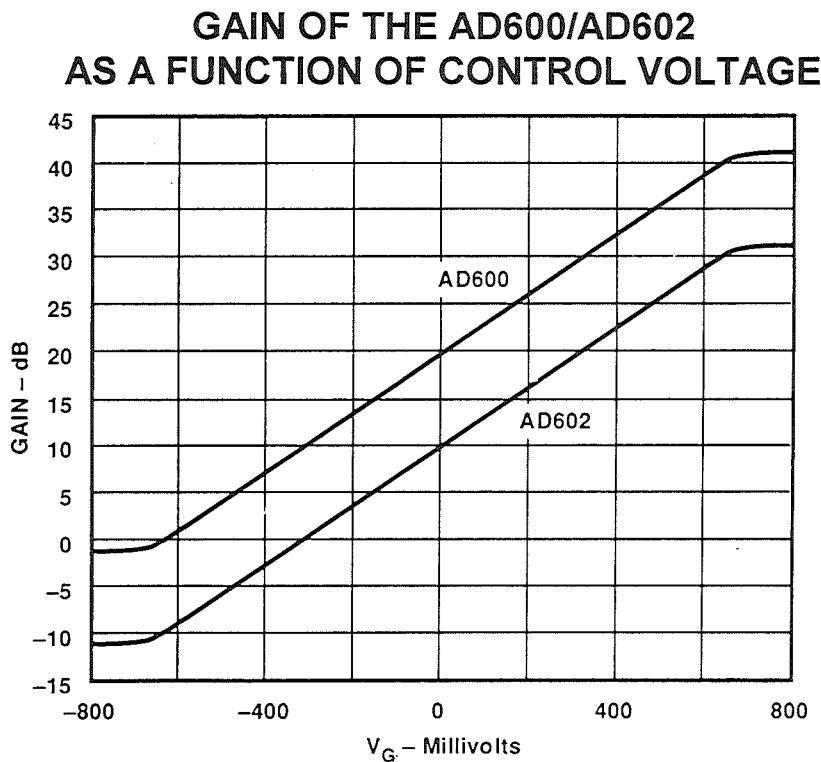


Figure 3.66

In order to understand the operation of the AD600/AD602, consider the simplified diagram shown in Figure 3.67. Notice that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance ( $g_m$ ) stages; the other input of all these  $g_m$

stages is connected to the amplifier's gain-determining feedback network,  $R_{F1}/R_{F2}$ . When the emitter bias current,  $I_E$ , is directed to one of the 8 transistor pairs (by means not shown here), it becomes the input stage for the complete amplifier.

### CONTINUOUS INTERPOLATION BETWEEN TAPS IN THE X-AMP IS PERFORMED WITH CURRENT-CONTROLLED $g_m$ STAGES

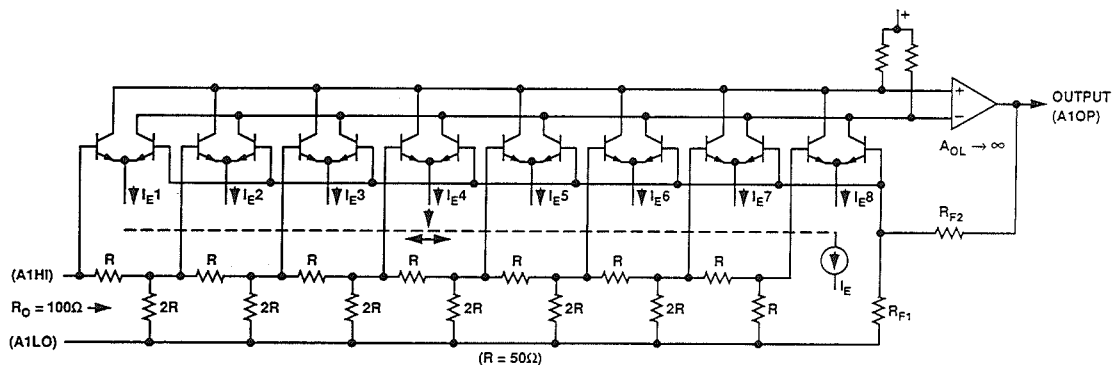


Figure 3.67

When  $I_E$  is connected to the pair on the left-hand side, the signal input is connected directly to the amplifier, giving the maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If  $I_E$  were now to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02dB, and the distortion would remain low, because only one  $g_m$  stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When  $I_E$  is equally divided between two  $g_m$  stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3dB, as one might first

expect, but rather by  $20\log 1.5$ , or 3.52dB. This error, when divided equally over the whole range, would amount to a gain ripple of  $\pm 0.25\text{dB}$ ; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of  $I_E$  always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple (see Reference 12). As  $I_E$  moves further to the right, the overall gain progressively drops.

The total input-referred noise of the X-AMP™ is  $1.4\text{nV}/\sqrt{\text{Hz}}$ ; only slightly more

than the thermal noise of a  $100\Omega$  resistor which is  $1.29\text{nV}/\sqrt{\text{Hz}}$  at  $25^\circ\text{C}$ . The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain. For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore  $1.4\text{nV}/\sqrt{\text{Hz}} \times 113$ , or  $158\text{nV}/\sqrt{\text{Hz}}$ . Referred to its maximum output of 2V rms, the signal-to-noise ratio would be 82dB in a 1MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10dB greater, or 92dB. Key features of the AD600/AD602 are summarized in Figure 3.68.

## KEY FEATURES OF THE AD600/AD602 X-AMPS

- Precise Decibel-Scaled Gain Control
- Accurate Absolute Gain Calibration
- Low Input-Referred Noise ( $1.4\text{nV}/\sqrt{\text{Hz}}$ )
- Constant Bandwidth (dc to 35MHz)
- Low Distortion:  $-60\text{dBc}$  THD at  $\pm 1\text{V}$  Output
- Stable Group Delay ( $\pm 2\text{ns}$  Over Gain Range)
- Response Time: Less than  $1\mu\text{s}$  for 40dB Gain Change
- Low Power (125mW per channel maximum)
- Differential Control Inputs

Figure 3.68

The AD603 X-AMP is a single version of the AD600/AD602 which provides 90MHz bandwidth. There are two pin-programmable gain ranges:  $-11\text{dB}$  to

$+31\text{dB}$  with 90MHz bandwidth, and  $+9\text{dB}$  to  $+51\text{dB}$  with 9MHz bandwidth. Key specifications for the AD603 are summarized in Figure 3.69.

## KEY FEATURES OF THE AD603 X-AMP

- Precise "Linear in dB" Gain Control
- Pin Programmable Gain Ranges:
  - 11dB to +31dB with 90MHz Bandwidth
  - +9dB to + 51dB with 9MHz Bandwidth
- Bandwidth Independent of Variable Gain
- Low Input-Referred Noise (1.3nV/√Hz)
- ±0.5dB Typical Gain Accuracy
- Low Distortion: –60dBc, 1V rms Output @ 10MHz
- Low Power (125mW)
- 8-pin Plastic SOIC or Ceramic DIP

3

Figure 3.69

## AN 80 dB RMS-LINEAR-dB MEASUREMENT SYSTEM

Monolithic RMS/DC converters provide an inexpensive means to measure the rms value of a signal of arbitrary waveform. They also may provide a low-accuracy logarithmic ("decibel-scaled") output. However, they have a fairly small dynamic range – typically only 50dB. More troublesome is that the bandwidth is roughly proportional to the signal level; for example, the AD636 provides a 3dB bandwidth of 900kHz for an input of 100mV rms, but only a 100kHz bandwidth for an input of 10mV rms. Its "raw" logarithmic output is unbuffered, uncalibrated, and not stable over temperature, requiring considerable support circuitry, including at least two adjustments and a special high-TC resistor.

All of these problems can be eliminated using an AD636 merely as *the detector element* in an AGC loop, in which the difference between the rms output of the amplifier and a fixed DC reference is nulled in a loop integrator. The dynamic range and the accuracy with which the signal can be determined are now entirely dependent on the amplifier used in the AGC system. Since the input to the RMS/DC converter is forced to a constant amplitude, close to its maximum input capability, the bandwidth is no longer signal-dependent. If the amplifier has a precise exponential ("linear-dB") gain-control law, its control voltage is forced by the AGC loop to have the general form

$$V_{\text{LOG}} = V_S \log_{10} \frac{V_{\text{IN(RMS)}}}{V_Z}$$

where  $V_S$  is the logarithmic slope and  $V_Z$  is the logarithmic intercept, that is, the value of  $V_{\text{IN}}$  for which  $V_{\text{LOG}}$  is zero.

Figure 3.70 shows a practical wide-dynamic-range rms measurement system using the AD600. It can handle inputs of from 100 $\mu$ V to 1V rms (4 decades) with a constant measurement

bandwidth of 20Hz to 2MHz, limited primarily by the AD636 RMS/DC converter. Its logarithmic output is a buffered voltage, accurately-calibrated to 100mV/dB, or 2V per decade, which simplifies the interpretation of the reading when using a DVM, and is arranged to be -4V for an input of 100 $\mu$ V rms input, zero for 10mV, and +4V for a 1V rms input. In terms of the above equation,  $V_S$  is 2V and  $V_Z$  is 10mV.

## A COMPLETE 80dB RMS-LINEAR-dB MEASUREMENT SYSTEM

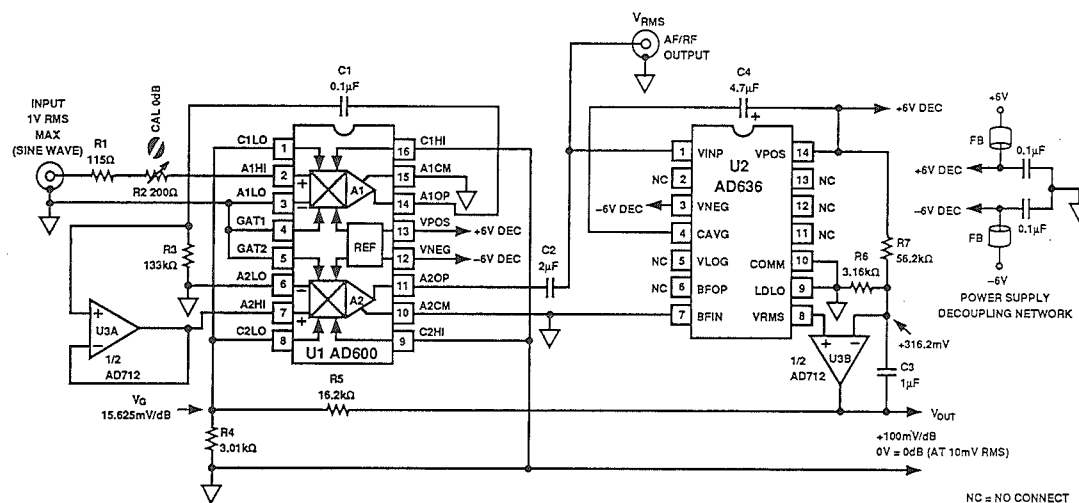


Figure 3.70

Note that the peak "log-output" of  $\pm 4$ V requires the use of  $\pm 6$ V supplies for the dual op-amp U3 (AD712), although lower supplies would suffice for the AD600 and AD636. If only  $\pm 5$ V supplies are available, it will either be necessary to use a reduced value for  $V_S$  (say, 1V,

in which case the peak output would be only  $\pm 2$ V), or to restrict the dynamic range of the signal to about 60dB.

The two amplifiers of the AD600 are used in cascade. The modest bandwidth of the unity-gain buffer U3A eliminates

the risk of instability at the highest gains. The buffer also allows the use of a high-impedance coupling network (C1/R3) which introduces a high-pass corner at about 12Hz. An input attenuator of 10dB ( $\times 0.316$ ) is now provided by R1 + R2 operating in conjunction with the AD600's input resistance of 100 $\Omega$ . The adjustment provides exact calibration of  $V_Z$  in critical applications, but R1 and R2 may be replaced by a fixed resistor of 215 $\Omega$  if very close calibration is not needed, since the input resistance of the AD600 (and all the other key parameters of it and the AD636) are already laser-trimmed for accurate operation. This attenuator allows inputs as large as  $\pm 4V$  to be accepted, that is, signals with an rms value of 1V combined with a crest-factor of up to 4.

The output of A2 is AC-coupled via another 12Hz high-pass filter formed by C2 and the 6.7k $\Omega$  input resistance of the AD636. The averaging time-constant for the RMS/DC converter is determined by C4. The unbuffered output of the AD636 (at pin 8) is compared with a fixed voltage of +316mV set by the positive supply voltage of +6V and resistors R6 and R7. ( $V_Z$  is proportional to this voltage, and systems requiring greater calibration accuracy should replace the supply-dependent reference with a more stable source. However,  $V_S$  is independent of the supply voltages, being determined by the band-gap reference in the X-AMP.) Any difference in these voltages is integrated by the op-amp U3B, with a time-constant of 3ms formed by the parallel sum of R6/R7 and C3.

If the gain of the AD600 is too high,  $V_{OUT}$  will be greater than the "set-point" of 316mV, causing the output of

U3B – that is,  $V_{LOG}$  – to ramp up (note that the integrator is non-inverting). A fraction of  $V_{LOG}$  is connected to the *inverting* gain-control inputs of the AD600, causing the gain to be reduced, as required, until  $V_{OUT}$  is equal to 316mV (DC), at which time the AC voltage at the output of A2 is forced to exactly 316mV (rms). This fraction is set by R4 and R5 such that a 15.625mV change in the control voltages of A1 and A2 – which would change the gain of the two cascaded amplifiers by 1 dB – requires a change of 100mV at  $V_{LOG}$ . Since A2 is forced to operate well below its limiting level, waveforms of high crest-factor can be tolerated throughout the amplifier.

To verify the operation, assume an input of 10mV rms is applied to the input, resulting in a voltage of 3.16mV rms at the input to A1 (due to the 10dB attenuator). If the system performs as claimed,  $V_{LOG}$  (and hence  $V_G$ ) should be zero. This being the case, the gain of both A1 and A2 will be 20dB and the output of the AD600 will be 100 times (40dB) greater than its input, 316mV rms. This is the input required at the AD636 to balance the loop, confirming the basic operation. Note that unlike most AGC circuits, (which often have a high gain/temperature coefficient due to the internal "kT/q" scaling), the voltages and thus the output of this measurement system are very stable over temperature. This behavior arises directly from the exact exponential calibration of the ladder attenuator.

Typical results are shown for a sinewave input at 100kHz. Figure 3.71 shows that the output is held very close to the set-point of 316mV rms over an input range in excess of 80dB.



## SIGNAL OUTPUT $V_{out}$ VERSUS INPUT LEVEL

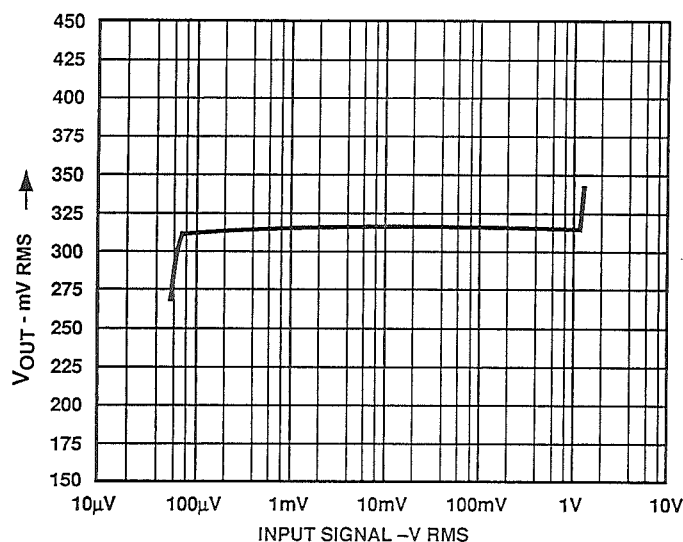


Figure 3.71

Figure 3.72 shows the “decibel” output voltage,  $V_{LOG}$ , and Figure 3.73 shows that the *deviation* from the ideal output

logarithmic output is within  $\pm 1$  dB for the 80dB range from 80 μV to 800mV.

## THE LOGARITHMIC OUTPUT $V_{LOG}$ VERSUS INPUT SIGNAL LEVEL

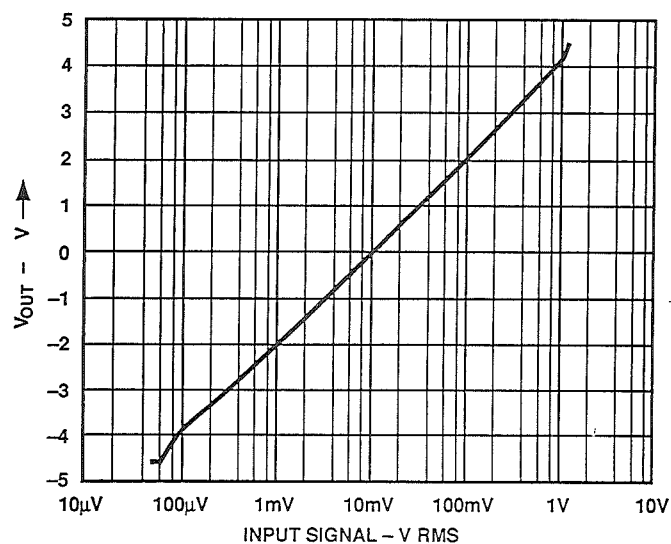


Figure 3.72

### DEVIATION FROM THE IDEAL LOGARITHMIC OUTPUT

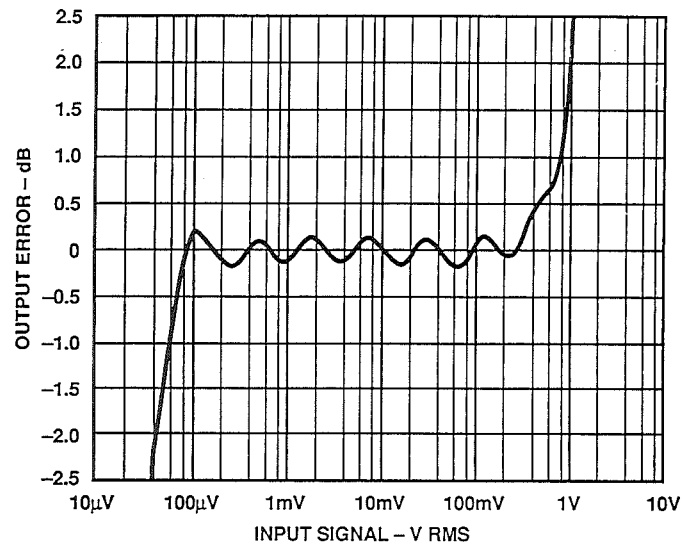


Figure 3.73

By suitable choice of the input attenuator,  $R1+R2$ , this could be centered to cover any range from  $25\mu\text{V}$  to  $250\text{mV}$  to, say,  $1\text{mV}$  to  $10\text{V}$ , with appropriate correction to the value of  $V_Z$ . (Note that  $V_Z$  is not affected by the changes in the range). The gain ripple of  $\pm 0.2\text{dB}$  seen in this curve is the result of the finite interpolation error of the X-AMP. It occurs with a periodicity of  $12\text{dB}$  – twice the separation between the tap points in each amplifier section.

This ripple can be canceled whenever the X-AMP stages are cascaded by introducing a  $3\text{dB}$  offset between the

two pairs of control voltages. A simple means to achieve this is shown in Figure 3.74: the voltages at  $C1\text{HI}$  and  $C2\text{HI}$  are “split” by  $\pm 46.875\text{mV}$ , or  $\pm 1.5\text{dB}$ . Alternatively, either one of these pins can be individually offset by  $3\text{dB}$ , and a  $1.5\text{dB}$  gain adjustment made at the input attenuator ( $R1+R2$ ). The error curve shown in Figure 3.75 demonstrates that over the central portion of the range, the output voltage can be maintained very close to the ideal value. The penalty for this modification is higher errors at both ends of the range.

## METHOD FOR CANCELING THE GAIN-CONTROL RIPPLE

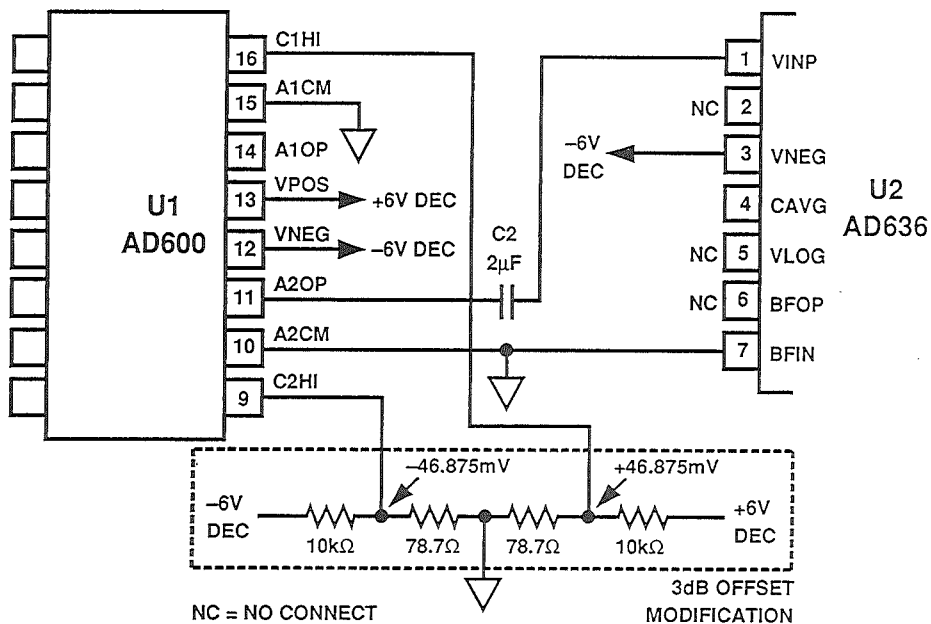


Figure 3.74

## LOGARITHMIC ERROR USING THE PREVIOUS CIRCUIT MODIFICATION

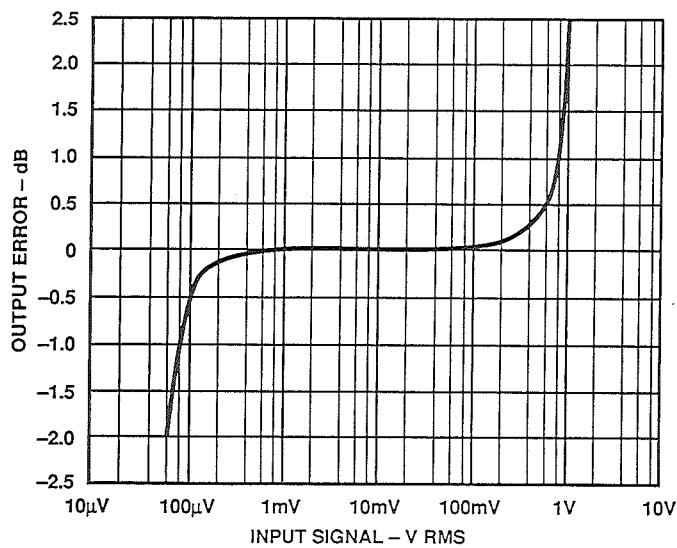


Figure 3.75

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## SECTION 4

### SAMPLED DATA SYSTEMS

- Discrete Time Sampling of Analog Signals
- Specifying the ADC Sampling Rate and the Antialiasing Filter
- ADC Resolution and Dynamic Range Requirements
- Undersampling (Super-Nyquist)



## SECTION 4

# SAMPLED DATA SYSTEMS

*Walt Kester*

Designing a signal processing system is a challenge which involves many tradeoffs. We have discussed signal amplification in detail and explored many of the various options available. When selecting the ADC, you must continue to keep the goal of preserving signal fidelity and dynamic range in mind, while resisting the temptation to overspecify. Overspecifying the ADC, its antialiasing filter, and other peripheral circuitry is especially dangerous, because it may result in high cost and even unrealizable component requirements. In order to specify intelligently the ADC portion of the system, one

must first understand the fundamental concepts of sampling and quantization and their effects on the signal.

We will first consider the traditional problem of sampling and quantizing a *baseband* signal whose bandwidth lies between dc and an upper frequency of interest,  $f_s$ . This is often referred to as *Nyquist*, or *Sub-Nyquist Sampling*. The topic of *Super-Nyquist* sampling (sometimes called *undersampling*) where the signal of interest falls outside of the Nyquist bandwidth (dc to  $f_s/2$ ) is treated later in this section.

4

## KEY ELEMENTS OF A BASEBAND SAMPLED DATA SYSTEM

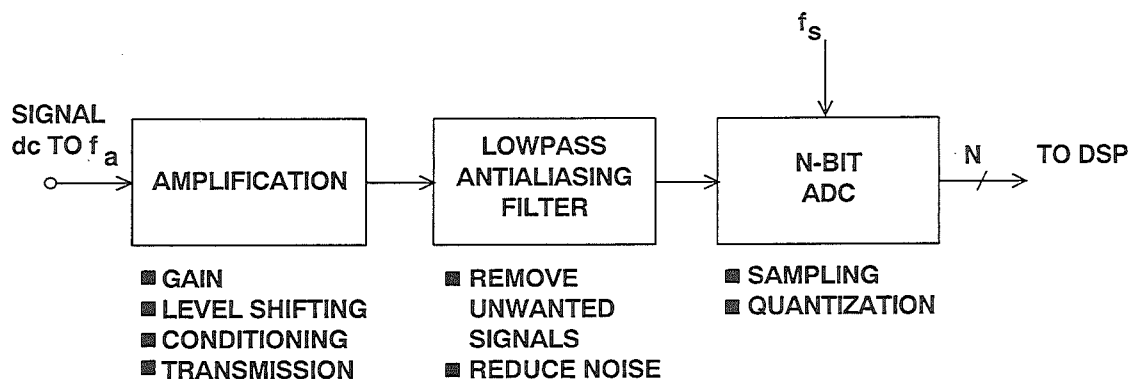


Figure 4.1



# DISCRETE TIME SAMPLING OF ANALOG SIGNALS

The concept of discrete time and amplitude sampling of an analog signal is shown in Figure 4.2. The continuous analog data must be sampled at discrete intervals,  $t_s$ , which must be carefully chosen to insure an accurate representation of the original analog signal. It is clear that the more samples taken (faster sampling rates),

the more accurate the digital representation, but if fewer samples are taken (lower sampling rates), a point is reached where critical information about the signal is actually lost. This leads us to the statement of Shannon's Information Theorem and Nyquist's Criteria given in Figure 4.3.

## SAMPLING AND QUANTIZING AN ANALOG SIGNAL

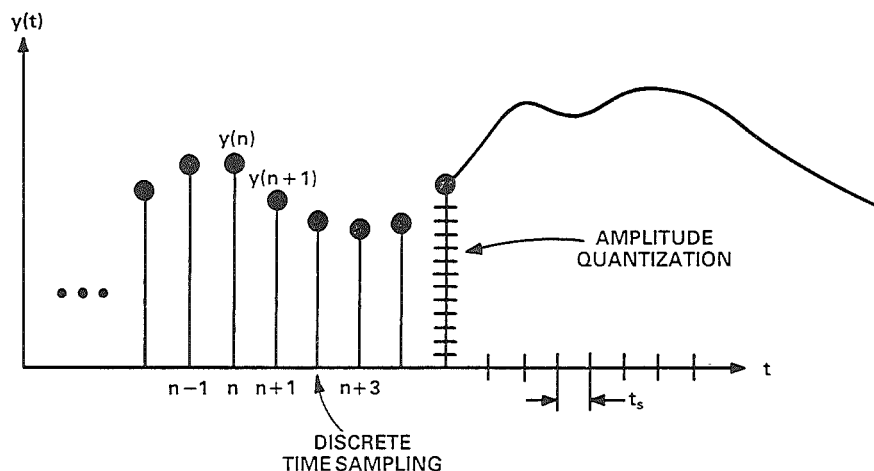


Figure 4.2

## SHANNON'S INFORMATION THEOREM AND NYQUIST'S CRITERIA

### ■ Shannon:

- ◆ An Analog Signal with a *Bandwidth* of  $f_a$  Must be Sampled at a Rate  $f_s > 2f_a$  in Order to Avoid the Loss of Information.
- ◆ The signal bandwidth may extend from DC to  $f_a$  (*Baseband Sampling*) or from  $f_1$  to  $f_2$ , where  $f_a = f_2 - f_1$  (*Undersampling, or Super-Nyquist*)

### ■ Nyquist:

- ◆ If  $f_s < 2f_a$ , then a Phenomena Called *Aliasing* Will Occur.
- ◆ *Aliasing* is used to advantage in undersampling applications.

Figure 4.3

In order to understand the implications of *aliasing* in both the time and frequency domain, first consider the four cases of a time domain representation of a sampled sinewave signal shown in Figure 4.4. In the Case 1, it is clear that an adequate number of samples have been taken to preserve the information about the sinewave. In Case 2 of the figure, only four samples per cycle are taken; still an adequate number to preserve the information. Case 3 represents the ambiguous limiting condition where  $f_s = 2f_a$ . If the relationship between the sampling points and the sinewave were such that the sinewave

was being sampled at precisely the zero crossings (rather than at the peaks, as shown in the illustration), then all information regarding the sinewave would be lost. Case 4 of Figure 4.4 represents the situation where  $f_s < 2f_a$ , and the information obtained from the samples indicates a sinewave having a frequency which is lower than  $f_s/2$ , i.e. the out-of-band signal is *aliased* into the Nyquist bandwidth between dc and  $f_s/2$ . As the sampling rate is further decreased, and the analog input frequency  $f_a$  approaches the sampling frequency  $f_s$ , the aliased signal approaches dc in the frequency spectrum.

## TIME DOMAIN EFFECTS OF ALIASING

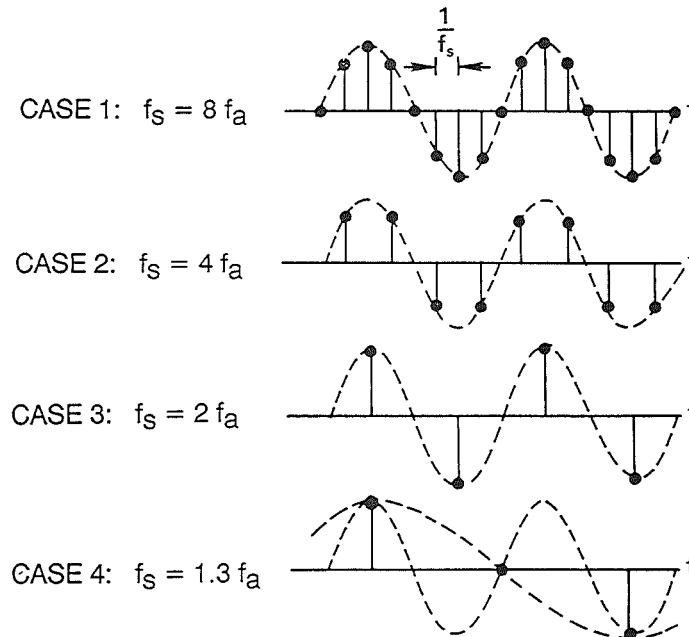


Figure 4.4

The corresponding frequency domain representation of the above scenario is shown in Figure 4.5. Note that sampling the analog signal  $f_a$  at a sampling rate  $f_s$  actually produces two alias frequency components, one at  $f_s + f_a$ , and the other at  $f_s - f_a$ . The upper alias,  $f_s + f_a$ , seldom presents a problem, since it lies outside the Nyquist bandwidth. It is the lower alias component,  $f_s - f_a$ , which causes problems when the input signal exceeds the Nyquist bandwidth,  $f_s/2$ .

From Figure 4.5, we make the important observation that *regardless of*

where the analog signal being sampled happens to lie in the frequency spectrum, the effects of sampling will cause either the actual signal or an aliased component to fall within the Nyquist bandwidth between dc and  $f_s/2$ . Therefore, any signals which fall outside the bandwidth of interest, whether they be spurious tones or random noise, must be adequately filtered *before* sampling. If unfiltered, the sampling process will alias them back within the Nyquist bandwidth where they will corrupt the wanted signals.

## FREQUENCY DOMAIN EFFECTS OF ALIASING

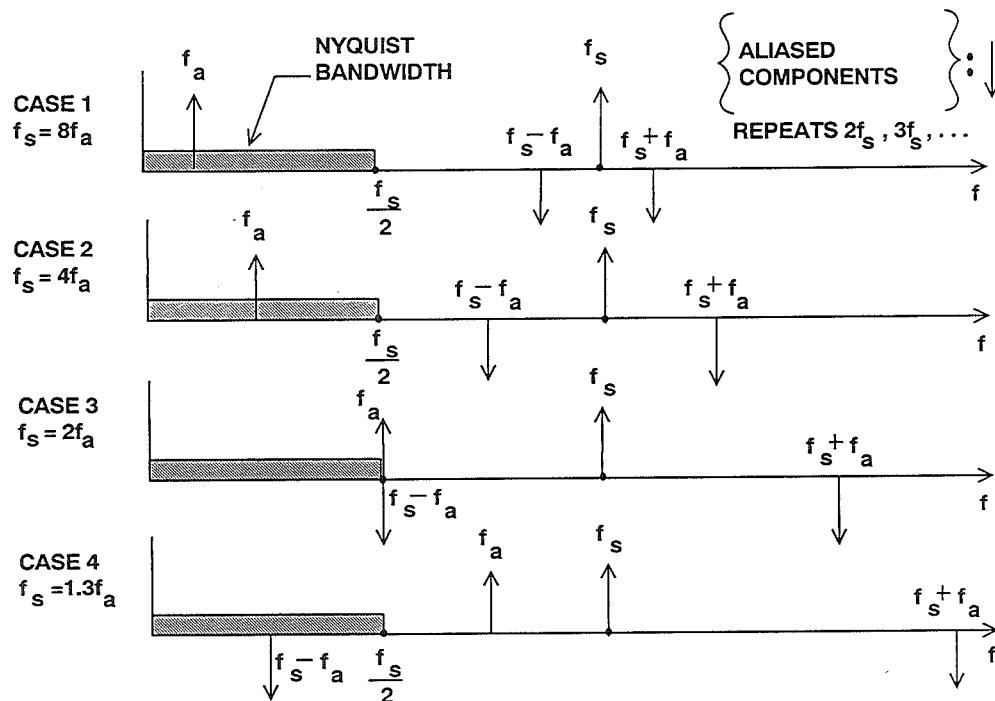


Figure 4.5

SPECIFYING THE ADC SAMPLING RATE  
AND THE ANTIALIASING FILTER

Properly specifying the ADC sampling rate basically involves trading off higher ADC sampling rates against increased antialiasing filter complexity. The first step is to know the characteristics of the signal being processed. Assume that the highest frequency of interest is  $f_a$ . The antialiasing filter passes signals from dc to  $f_a$  while attenuating signals above  $f_a$ . We have

now reached the first decision point, since there is no such thing as a perfect analog lowpass filter.

Assume that the corner frequency of the filter is chosen to be equal to  $f_a$ . The effect of the finite transition from minimum to maximum attenuation on system dynamic range is illustrated in Figure 4.6.

# EFFECTS OF ANTIALIASING FILTER ON SYSTEM DYNAMIC RANGE

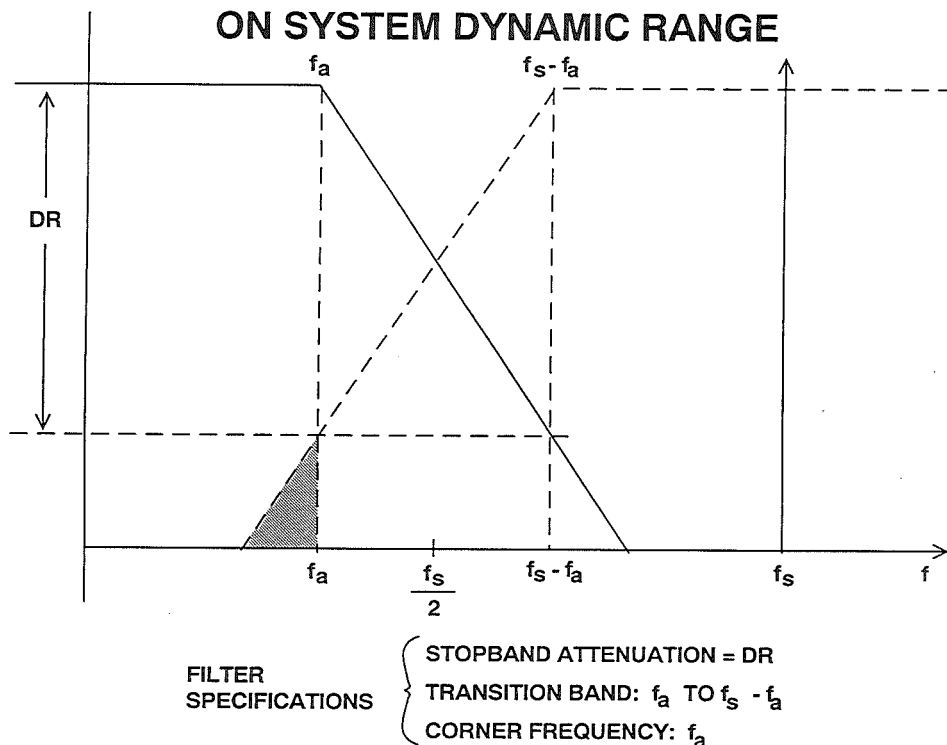


Figure 4.6

Assume that the input signal has fullscale components well above the maximum frequency of interest,  $f_a$ . The diagram shows how fullscale frequency components above  $f_s - f_a$  are aliased back into the bandwidth dc to  $f_a$ . These aliased components are indistinguishable from actual signals and therefore limit the dynamic range to the value on the diagram which is shown as  $DR$ .

Some texts recommend specifying the antialiasing filter with respect to the Nyquist frequency,  $f_s/2$ , but this assumes that the signal bandwidth of interest extends from dc to  $f_s/2$  which is rarely the case. In the example shown in Figure 4.6, the aliased components between  $f_a$  and  $f_s/2$  are not of interest and do not limit the dynamic range.

The antialiasing filter transition band is therefore determined by the corner frequency  $f_a$ , the stopband frequency

$f_s - f_a$ , and the stopband attenuation,  $DR$ . We choose the required system dynamic range based on our requirement for signal fidelity.

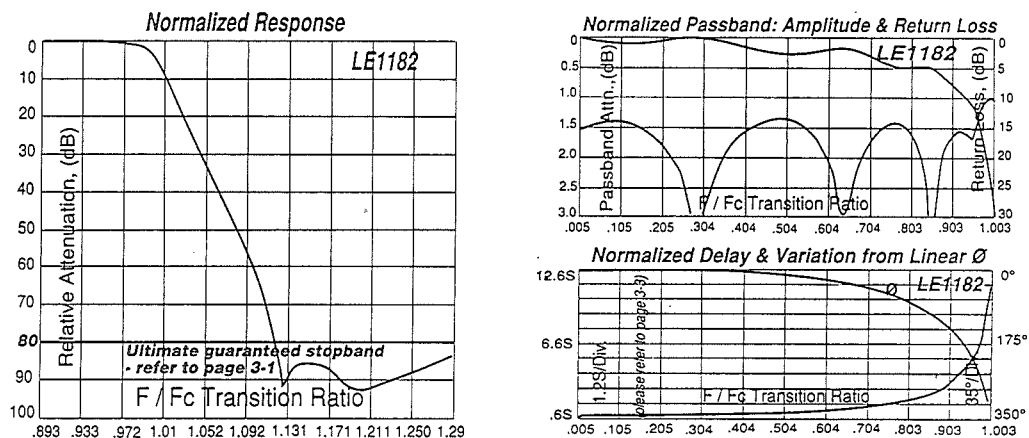
Filters become more complex as the transition band becomes sharper, all other things being equal. For instance, a Butterworth filter design gives 6dB attenuation per octave for each filter pole. Achieving 60dB attenuation in a transition region between 1MHz and 2MHz (1 octave) requires a minimum of 10 poles.

Other filter designs are generally more suited to high speed applications where the requirement for a sharp transition band is combined with requirements on in-band flatness and linear phase response. Elliptic filters are popular choices for high speed antialiasing filters.

There are a number of companies which specialize in designing custom analog filters. As an example, the normalized response of the TTE, Inc., LE1182 11-pole elliptical antialiasing filter is shown in Figure 4.7. Notice that this filter is specified to achieve at least 80dB attenuation between  $f_c$  and  $1.2f_c$  (Refer-

ence 1). The corresponding passband ripple, return loss, delay, and phase response are also shown in Figure 4.7. This custom filter is available in corner frequencies up to 100MHz and in a choice of PC board, BNC, or SMA compatible packages.

## CHARACTERISTICS OF TTE, INC., L31182-SERIES 11-POLE ELLIPTICAL FILTER



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TTE, Inc., 2251 Barry Ave., Los Angeles, CA 90064

Figure 4.7

From this discussion, we can see how the sharpness of the antialiasing transition band can be traded off against the ADC sampling frequency. Choosing a higher sampling rate (oversampling) reduces the requirement on transition band sharpness (hence, the filter complexity) at the expense of using a faster ADC and processing data at a faster rate. Remember that high speed ADCs are not oversampling as in the case of Sigma-Delta converters.

The above design process is started by choosing an initial sampling rate of 2 to 4 times  $f_a$ . Determine the filter specifications based on the required dynamic range and see if such a filter is realizable within the constraints of the system cost and performance. If not, consider a higher sampling rate and a faster ADC.

The antialiasing filter requirements may be relaxed somewhat if it is certain

that there will never be a fullscale signal at the stopband frequency  $f_s - f_a$ . In many applications it is improbable that fullscale signals will occur at this frequency. If the maximum signal at the frequency  $f_s - f_a$  will never exceed XdB below fullscale, then the filter stopband attenuation requirement is reduced by that same amount. The new

requirement for stopband attenuation at  $f_s - f_a$  based on this knowledge of the signal is now only  $DR - XdB$ . When making this type of assumption, be careful to treat any noise signals which may occur above the maximum signal frequency  $f_a$  as unwanted signals which will also alias back into the signal bandwidth.

## ADC RESOLUTION AND DYNAMIC RANGE REQUIREMENTS

So far, we have discussed only the effects of ADC sampling and aliasing on the system dynamic range. The effects of dividing the signal amplitude into a finite number of discrete quantization levels must also be considered.

Figure 4.8 shows a table of relative bit sizes for various resolution ADCs. The

fullscale input range is chosen to be approximately 2V which is popular for higher speed ADCs. The bit size (or LSB weight,  $q$ ) is determined by dividing the fullscale range of the converter by the number of possible quantization levels. Hence, a 10bit ADC having 1024 discrete levels has an LSB weight of  $2.048V/1024$ , or 2mV.

### BIT SIZES, THEORETICAL QUANTIZATION NOISE, AND SNR FOR 2.048V FULLSCALE CONVERTERS

Resolution (N Bits)	1 LSB = $q$	% FS	ppm FS	dB FS (6N)	RMS Quantization Noise, $q/\sqrt{12}$	Theoretical Fullscale SNR (dB)
6	32mV	1.56	15625	36	9.2mV	37.9
8	8mV	0.39	3906	48	2.3mV	50.0
10	2mV	0.098	977	60	580 $\mu$ V	62.0
12	500 $\mu$ V	0.024	244	72	144 $\mu$ V	74.0
14	125 $\mu$ V	0.0061	61	84	36 $\mu$ V	86.0
16	31 $\mu$ V	0.0015	15	96	13 $\mu$ V	98.1

Figure 4.8

The selection process for determining the ADC resolution should begin by determining the ratio between the largest signal (fullscale) and the smallest signal you wish the ADC to detect. Convert this ratio to dB, and divide by 6. This is your *minimum* ADC resolution requirement for dc signals. You will actually need more resolution to account for extra signal headroom, since ADCs act as hard limiters at both ends of their range. Remember that this computation is for dc or low frequency signals and that the ADC performance will degrade as the input signal slewrate increases. What will actually occur is that the final ADC resolution will be dictated by dynamic performance at high frequencies. This may lead to the selection of an ADC which has more resolution at dc than is actually required.

Also shown in the table of Figure 4.8 is the theoretical rms quantization noise produced by a perfect N-bit ADC. In the development of classical ADC quantization noise theory, the assumption is usually made that the quantization error signal is uncorrelated with the ADC input signal. If this is true, then the quantization noise appears as random noise spread uniformly over the Nyquist bandwidth, dc to  $f_s/2$ , and it has an rms value equal to  $q/\sqrt{12}$ .

If, however, the input signal is locked to a non-prime integer sub-multiple of  $f_s$ , the quantization noise will no longer appear as uniformly distributed random noise, but instead will appear as harmonics of the fundamental input sinewave. This is especially true if the

input is an exact even submultiple of  $f_s$ . Figure 4.9 illustrates the point using FFT simulation for an ideal 12 bit ADC. The FFT record length was chosen to be 4096. The spectrum on the left shows the FFT output when the input signal is an exact even submultiple ( $1/32$ ) of the sampling frequency (the frequency was chosen so that there were exactly 128 cycles per record). The ratio of the worst harmonic to the signal (Spurious Free Dynamic Range, SFDR) is approximately 78dBc. The spectrum on the right shows the output when the input signal is such that there are exactly 127 cycles per record. The SFDR is now about 92dBc which is an improvement of 14dB. Signal-correlated quantization noise is highly undesirable in spectral analysis applications, where it becomes difficult to differentiate between real signals and system-induced spurious components, especially when searching the spectrum for the presence of low-level signals in the presence of large signals.

There are a number of ways to reduce this problem, but the easiest way is to add a small amount of broadband rms noise to the ADC input signal as shown in Figure 4.10. The rms value of this noise should be equal to about  $1/2$  LSB. The effect of this is to randomize the quantization noise and eliminate its possible signal-dependence. In many systems, there is usually enough random noise on the input signal and the sampling clock so that this happens automatically. This is especially likely when using high speed ADCs which have 12 or more bits of resolution and a relatively small input range of 2V p-p.



# EFFECTS OF SAMPLING A SIGNAL WHICH IS AN EXACT EVEN SUB-MULTIPLE OF THE ADC SAMPLING FREQUENCY (M = 4096, IDEAL 12-BIT ADC SIMULATION)

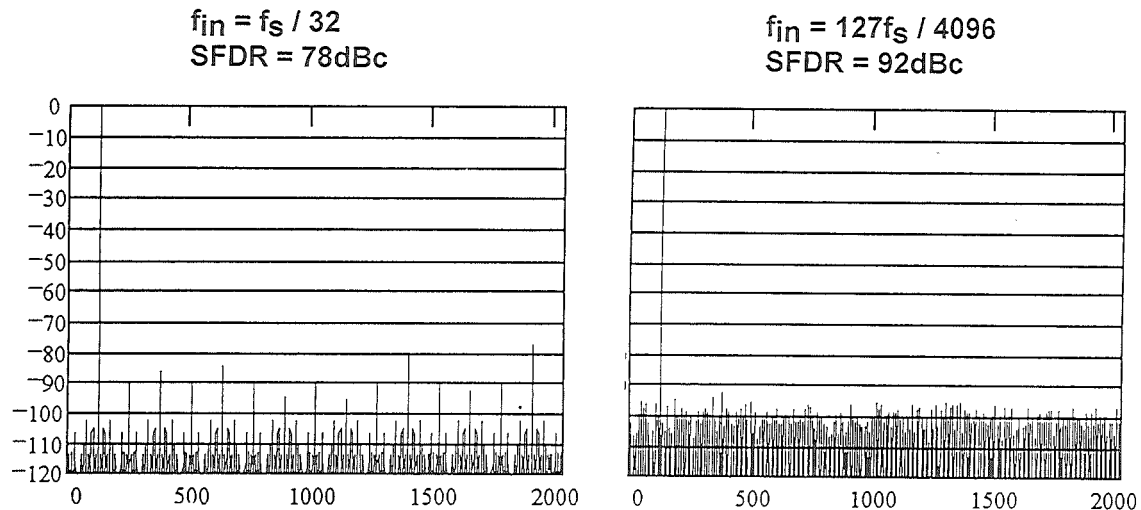


Figure 4.9

# THE ADDITION OF GAUSSIAN WIDEBAND NOISE TO THE ADC INPUT RANDOMIZES QUANTIZATION NOISE AND REMOVES INPUT SIGNAL DEPENDENCE

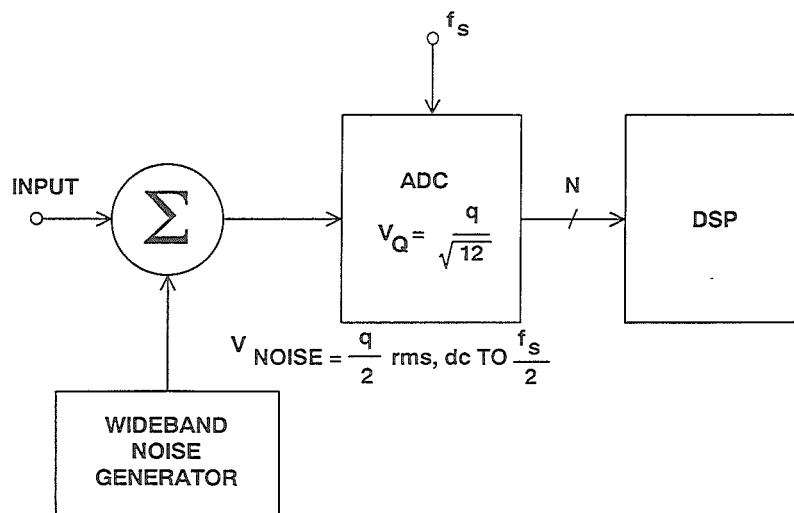


Figure 4.10

Quantization noise is therefore spread over the entire Nyquist bandwidth dc to  $f_s/2$ . The theoretical fullscale rms sinewave signal-to-noise ratio (SNR) may then be calculated using the well known formula,  $SNR = 6.02N + 1.76\text{dB}$ .

In actual practice, sampling ADCs are evaluated for their dynamic performance by first applying a spectrally pure sinewave input and then perform-

ing an FFT on the ADC output data as shown in Figures 4.11 and 4.12. The FFT output can be used to calculate harmonic distortion, THD, and SNR. The actual SNR is then compared to the theoretical SNR. The measured SNR may be substituted in the SNR formula, and the equation solved for N. The resulting value for N is called the *effective number of bits, or ENOBs*.

## ADC DYNAMIC TESTING

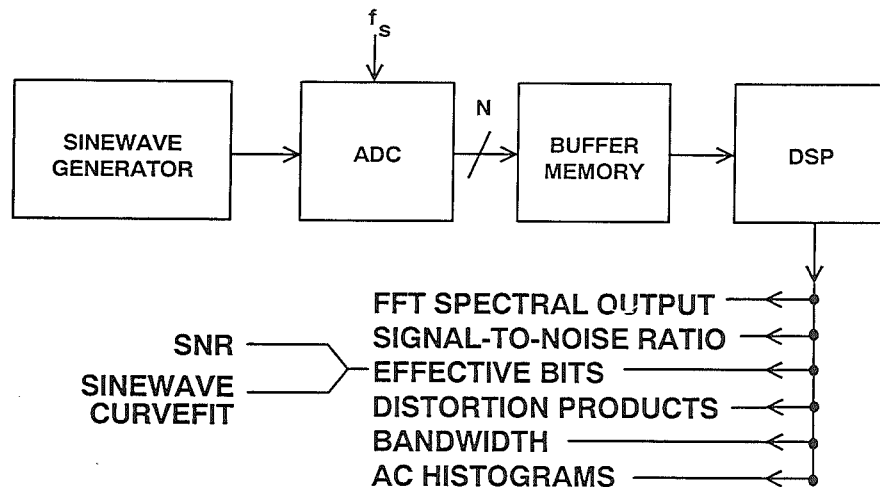


Figure 4.11

## 4096 POINT FFT OUTPUTS FOR AD9022 12-BIT, 20MSPS ADC

$F_S = 20 \text{ MSPS}$

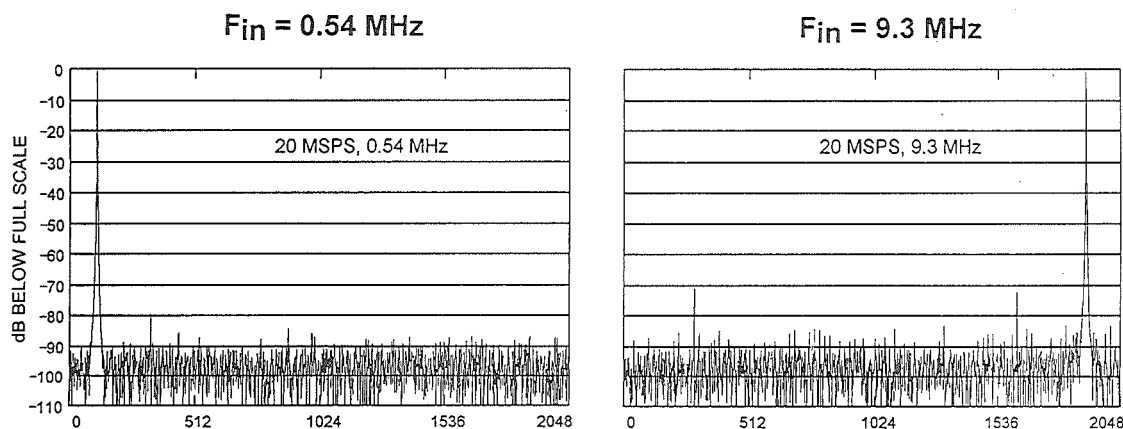


Figure 4.12

## QUANTIZATION THEORY BASICS

- RMS Quantization Noise in Nyquist Bandwidth, DC to  $f_S/2$ :  
 $q/\sqrt{12}$ ,  $q$  = LSB Weight

- Fullscale Sinewave RMS Signal to RMS Noise Ratio in Nyquist Bandwidth:

$$\text{SNR} = 6.02N + 1.76\text{dB}$$

- Effective Number of Bits (ENOB):

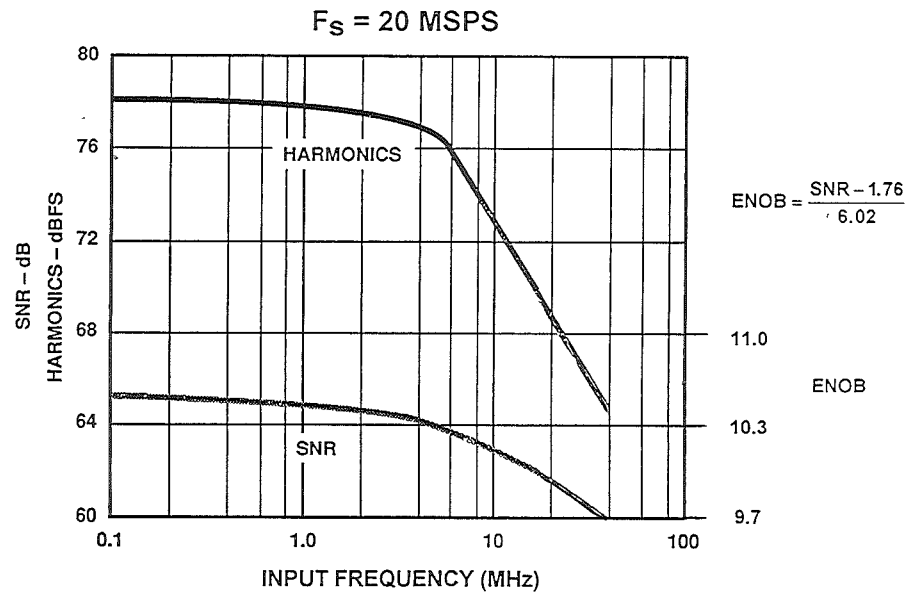
$$\text{ENOB} = \frac{\text{SNR}_{\text{ACTUAL}} - 1.76\text{dB}}{6.02}$$

Figure 4.13

The SNR and effective bits measurement is made for both low, intermediate, and high frequency input signals. All ADCs exhibit some degradation in SNR and ENOBs at higher input signal

frequencies due to various sources of nonlinearities. Figure 4.12 shows the  $S/(N + D)$  for the AD9022 12 bit, 20MSPS monolithic sampling ADC.

## S/(N+D) AND EFFECTIVE BIT PERFORMANCE OF AD9022 12-BIT, 20MSPS SAMPLING ADC



4

Figure 4.14

The AD9022 is representative of a class of high-performance *sampling* ADCs. Sampling ADCs have the sample-and-

hold function on-chip and are characterized in terms of both dc and ac specifications.

## MODERN SIGNAL-PROCESSING ADCs

- Most are *Sampling* ADCs Containing on-chip SHA Function as Opposed to *Encoders*, which have no SHA
- Interface Between SHA and ADC Handled on-chip
- Complete DC and AC Specifications Usually Provided: SNR, THD, SFDR, ENOB, Bandwidth, etc.
- Input Full-Power Bandwidth is Usually Much Greater than  $f_s/2$

Figure 4.15

The input bandwidth of the ADC should be considerably greater than the highest-frequency baseband signal of interest. The full-power bandwidth (FPBW) of an ADC is that input frequency at which the amplitude of the reconstructed FFT *fundamental* is reduced by 3dB for a fullscale input. Generally, though, there is considerable loss of

*resolution* at frequencies well below this. Full-power bandwidth must be examined in conjunction with SNR, ENOB, and THD in order to determine the actual dynamic performance of the ADC at the FPBW frequency. The small signal ADC bandwidth is approximately equal to the FPBW if there is no slewrate limiting. .

## ADC FULL-POWER BANDWIDTH

- The Frequency at Which the Amplitude of the *Fundamental* Component in the FFT Output is Down 3dB
- FPBW Usually  $> f_s$  (Except for  $\Sigma\Delta$  ADCs)
- Must Examine ENOB and THD at FPBW Frequency - Usually Much Reduced
- Example: AD9022 FPBW = 100MHz, 9.7 ENOB @ 40MHz INPUT
- Use FPBW or Small Signal BW (if Greater Than FPBW) for Noise Calculations

Figure 4.16

The next step in the process of determining the ADC resolution is to determine the effective bit (ENOB) requirement or SNR at the highest input frequency of interest,  $f_a$ . Most modern sampling ADCs have these specifications and also curves similar to that of Figure 4.14. Remember that the S/(N+D) calculation includes all distortion products as well as those due to quantization.

The *peak spurious* or peak harmonic component is the largest spectral com-

ponent excluding the input signal and dc (measured with FFT techniques). This value is expressed in dB relative to the rms value of the input signal. This specification is also referred to as *spurious free dynamic range*, or SFDR. In applications such as digital spectral analysis using FFT techniques, harmonic distortion, THD, or spurious free dynamic range (SFDR) may be of greater concern than the actual broadband rms noise level.

The FFT takes a discrete number of time samples,  $M$ , and converts them into  $M/2$  discrete spectral components. The spacing between the spectral lines is  $\Delta f = f_s/M$ . If an FFT is performed on broadband quantization noise which has a bandwidth of  $f_s/2$ , the average value of the noise contained in each FFT frequency cell is  $10\log_{10}(M/2)$  dB less than the rms value of the quantization noise. This is illustrated in Figure

4.17. This is equivalent to sweeping an analog spectrum analyzer from dc to  $f_s/2$  with the bandwidth set to  $\Delta f$ . The average value of the noise components in each frequency bin can be reduced 3dB by doubling the record length  $M$ . Using deeper FFTs, averaging the results of a number of FFTs, or other filtering techniques may also be used to reduce the rms noise floor and allow greater dynamic range.

**THE EFFECTIVE NOISE FLOOR OF AN M-POINT FFT  
(MEASUREMENT BANDWIDTH =  $f_s/M$ ) IS MUCH LESS THAN  
THE RMS VALUE OF THE QUANTIZATION NOISE  
(MEASUREMENT BANDWIDTH =  $f_s/2$ )**

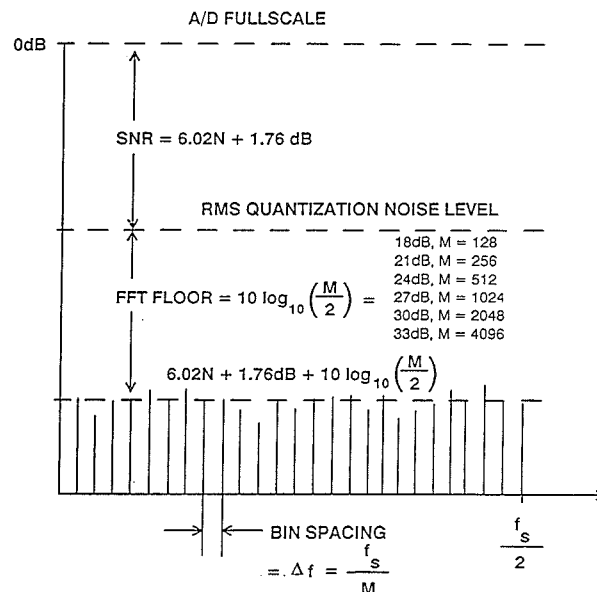


Figure 4.17

The SFDR of an ADC is generally a function of both input frequency and amplitude. Figure 4.18 shows the SFDR versus the input signal level for the AD9014 14 bit 10MSPS ADC. The data is given for two input frequencies:

4.3MHz and 9.9MHz. Notice that the SFDR at 4.3MHz reaches its maximum value at fullscale. For the 9.9MHz input, however, the point of maximum SFDR occurs several dB below fullscale.

## SPURIOUS FREE DYNAMIC RANGE AS A FUNCTION OF INPUT SIGNAL LEVEL FOR THE AD9014 14-BIT, 10MSPS ADC

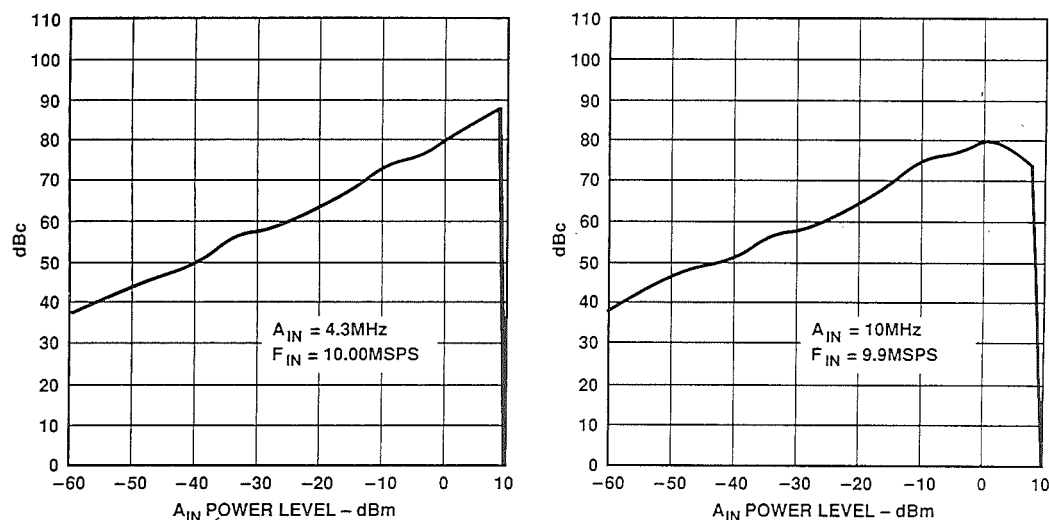


Figure 4.18

As discussed above, SFDR should not be confused with SNR. SNR depends more on the rms value of the quantization noise and is therefore a function of the number of ADC bits. SFDR, on the other hand, depends more on the linearity of the ADC and is relatively independent of the number of actual bits. This is dramatically illustrated in Figure 4.19, where SNR and SFDR is

shown for the AD9014 ADC. The top curve in the figure shows the SFDR of the AD9014 utilizing 14, 12, and 10 bits of the ADC. The bottom three curves show the SNR of the AD9014 operating with 14, 12, and 10 bits. The level of the internally generated spurs will not rise as bits are omitted, but the broadband rms noise floor rises for each bit that is dropped.

### AD9014 SFDR AND SNR VERSUS FREQUENCY FOR 14, 12, AND 10 ACTIVE BITS

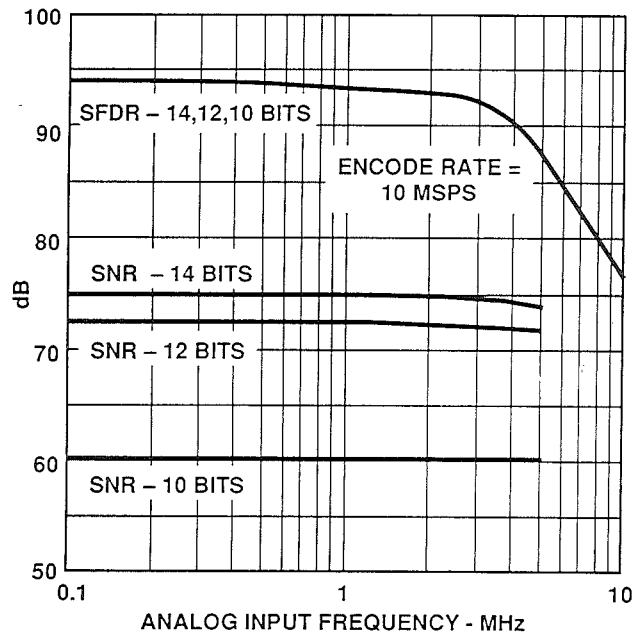


Figure 4.19

The distortion produced by an ADC cannot be analyzed in terms of second and third-order intercepts as in the case of an amplifier. This is because there are two components of distortion in a high performance ADC. One component is due to the non-linearity associated with the analog front end amplifier and the sample-and-hold. This non-linearity has the familiar “bow” or “s”-shaped curve shown in Figure 4.20. The distortion associated with this type of non-linearity is sometimes referred to as *soft*

distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner and is a function of signal level. In a practical ADC, however, the soft distortion is usually much less than the other component of distortion which is due to the nonlinearity of the encoder transfer function itself. This function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 4.20.



## TRANSFER CHARACTERISTICS FOR "SOFT" AND "HARD" DISTORTION

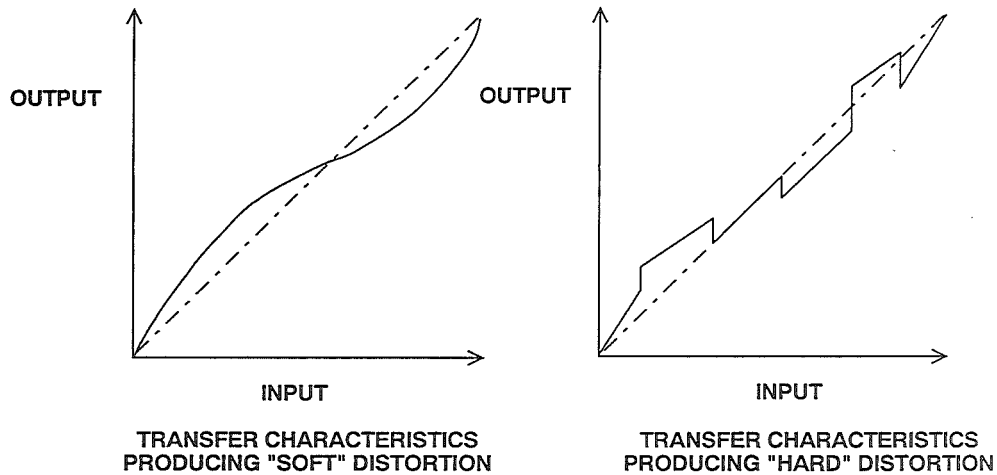


Figure 4.20

The actual location of the points of discontinuity depends on the particular ADC architecture, but nevertheless such discontinuities occur in practically all high speed ADCs. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level. For lower-amplitude signals, this constant level *hard* distortion causes the SFDR of the ADC to decrease as input amplitude decreases. The soft distortion

in a well-designed ADC generally only comes into play for high frequency large-amplitude input signals where it may rise above the hard distortion floor. This can be observed in Figure 4.18, where the 4.3MHz input data indicates a relatively constant hard distortion floor as the signal amplitude is increased to fullscale. The 9.9MHz data, however, indicates an increase in soft distortion as the input signal approaches fullscale.

## UNDERSAMPLING (SUPER-NYQUIST)

Many modern signal processing applications require ADCs with extremely wide dynamic range. The ADC is often the limiting factor in the performance of digital spectrum analyzers. In direct IF-to-digital receivers, the ADC must accurately digitize narrowband signals with a center frequency much greater than the Nyquist frequency of one-half the sampling rate. This is called *undersampling*, and often requires that a high-performance sample-and-hold be placed in front of the ADC to increase the dynamic range. The traditional sigma-delta architecture can be modified to yield a bandpass rather than a lowpass transfer function, thereby allowing it to be used to process IF signals well above 1MHz. Finally, variable gain, high speed, low distortion amplifiers may extend system dynamic range as in the case of ultrasound systems.

Digital techniques are common in modern signal intelligence (SIGINT) and other high performance radios. The information is extracted from the signals using fast FFTs, digital filtering, and other powerful DSP techniques. One of the important and often limiting characteristics of such receivers is the inherent spectral purity and noise of the ADC. Digital spectral analysis is an-

other application where the spectral purity and noise of the ADC may be the performance-limiting factor. In this section, we will examine the tradeoffs and illustrate some techniques which may be used to improve ADC performance.

Digital techniques have become widespread in radar receivers, broadband communications receivers, and mobile radio. A simplified block diagram of a traditional digital receiver using baseband sampling is shown in Figure 4.21. The mixer in the RF section of the receiver mixes the signal from the antenna with the RF frequency of the first local oscillator, LO1. The desired information is contained in relatively small bandwidth of frequencies  $\Delta f$ . In actual receivers,  $\Delta f$  may be as high as a few megahertz. The LO1 frequency is chosen such that the  $\Delta f$  band is centered about the IF frequency at the bandpass filter output. Popular IF frequencies are generally between 30 and 100MHz. The IF mixer then translates the  $\Delta f$  frequency band down to baseband where it is filtered and processed by a baseband ADC. Actual receivers generally have several stages of RF and IF processing, but the simple diagram serves to illustrate the concepts.

## SIMPLIFIED DIGITAL RECEIVER USING BASEBAND SAMPLING

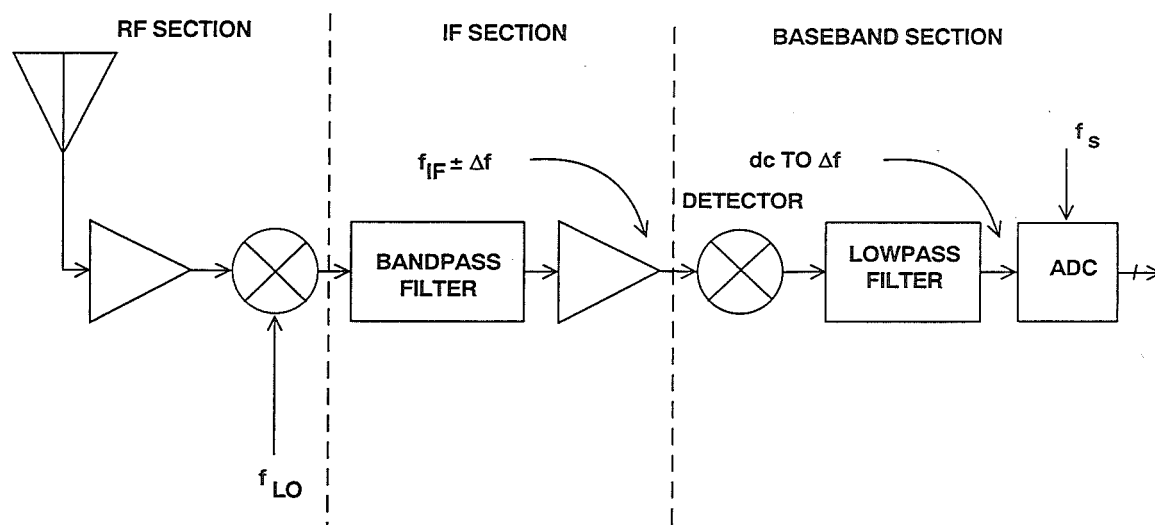


Figure 4.21

In a receiver which uses direct IF-to-digital techniques (IF sampling), the IF signal is applied directly to a wide bandwidth ADC as shown in Figure 4.22. The ADC sampling rate is chosen to be at least  $2\Delta f$ . The process of sampling the IF frequency at the proper rate causes one of the aliased components of  $\Delta f$  to appear in the dc to  $f_s/2$  Nyquist bandwidth of the ADC output. DSP techniques can now be used to process the digital baseband signal. This approach may yield an improvement in overall signal-to-noise ratio by eliminating the detector stage. There is

also more flexibility in the DSP because the ADC sampling rate can be shifted to tune the exact position of the  $\Delta f$  signal within the baseband. The obvious problem with this approach is that the ADC must now be able to accurately digitize signals which are well outside the dc to  $f_s/2$  Nyquist bandwidth which most ADCs were designed to handle. Special techniques are available, however, which can extend the dynamic range of ADCs to include IF frequencies. Before examining the ADC problem, we will first look at the basic theory behind undersampling.

## SIMPLIFIED DIGITAL RECEIVER USING IF SAMPLING

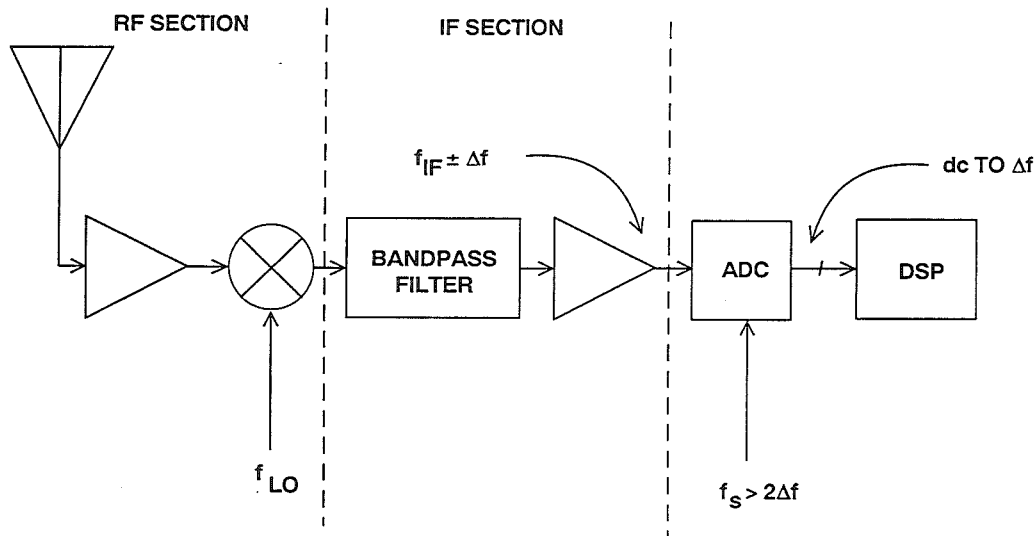


Figure 4.22

Figure 4.23 shows four cases where a signal having about a 1MHz bandwidth is located at different portions of the frequency spectrum. The minimum sampling rate required for no aliasing is also shown. In general, the sampling frequency must be at least twice the signal bandwidth, and the sampled signal must not cross an integer multiple of  $f_s/2$ .

In the first case, the signal occupies the band from dc to 1MHz, and therefore must be sampled at greater than

2MSPS. The second case shows a 1MHz signal which occupies the band from 0.5 to 1.5MHz. Notice that this signal must be sampled at a minimum of 3MHz to avoid aliasing. In the third case, the signal occupies the band from 1 to 2MHz, and the minimum required sampling rate for no aliasing drops back to 2MHz. The last case shows a signal which occupies the band from of 1.5 to 2.5MHz. This signal must be sampled at a minimum of 2.5MHz to avoid aliasing.

## MINIMUM SAMPLING RATE REQUIRED FOR NO ALIASING OF A 1MHz BANDWIDTH SIGNAL

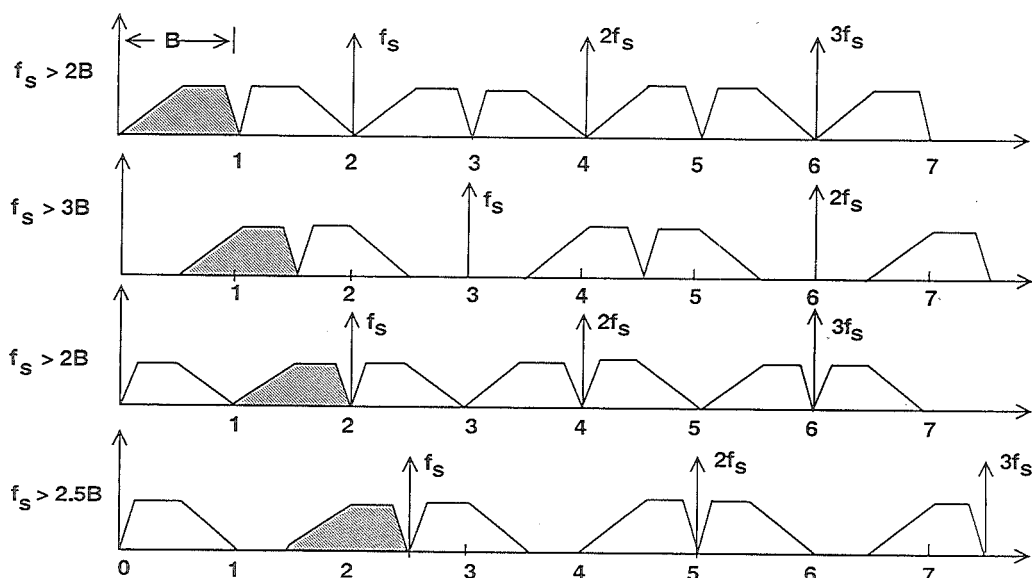


Figure 4.23

This analysis can be generalized as shown in Figure 4.24. The actual minimum required sampling rate is a func-

tion of the ratio of the highest frequency component to the total signal bandwidth.

## MINIMUM REQUIRED SAMPLING RATE AS A FUNCTION OF THE RATIO OF THE HIGHEST FREQUENCY COMPONENT TO THE TOTAL SIGNAL BANDWIDTH

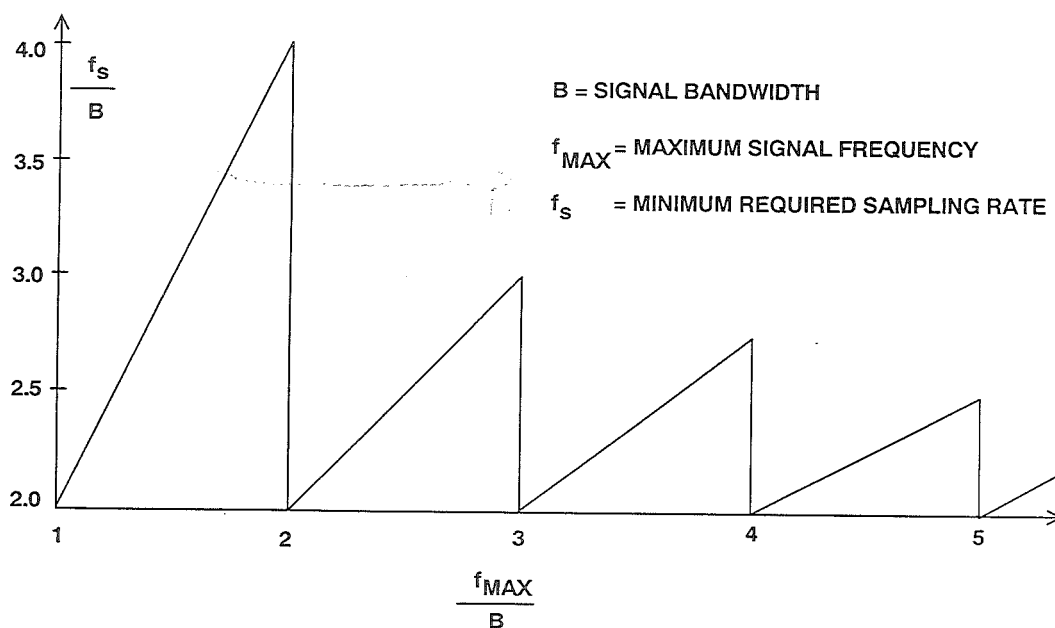


Figure 4.24

Let us now examine a signal which occupies a band between 6 and 7MHz as shown in Figure 4.25. Assume the ADC sampling rate is 2MHz. Notice that the sampling process generates aliases of this signal around multiples

of  $f_s$ . In the frequency spectrum, the alias component falling between 0 and 1MHz is an accurate representation of the original signal, assuming no ADC errors.

### INTERMEDIATE FREQUENCY (IF) SIGNAL BETWEEN 6 AND 7 MHz IS ALIASED BETWEEN DC AND 1 MHz BY SAMPLING AT 2MSPS

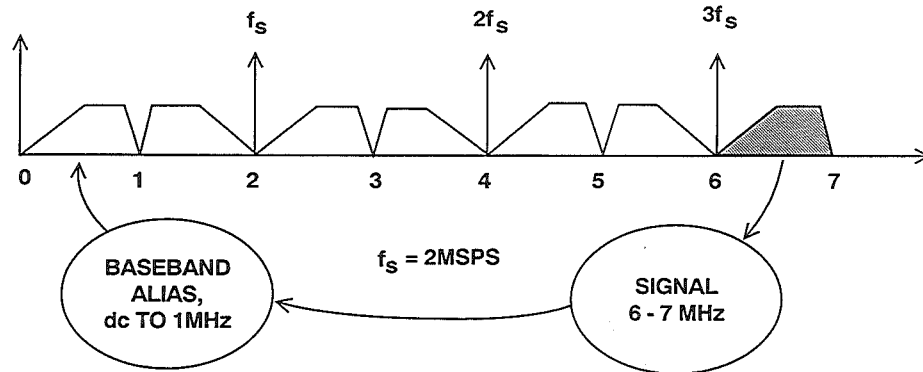


Figure 4.25

The above discussions show that although the concept of direct IF sampling is relatively straightforward, the implications for the ADC dynamic performance characteristics are significant.

Let us consider a typical example, where the IF frequency is 72.5MHz, and the desired signal occupies a bandwidth of 4MHz ( $B=4\text{MHz}$ ), centered on the IF frequency (see Figure 4.26). We know from the previous discussion that the minimum sampling rate must be greater than 8MHz, probably on the order of 10MHz in order to prevent

dynamic range limitations due to aliasing. If we place the sampling frequency at the lower band-edge of 70MHz ( $72.5-2.5$ ), we will definitely recover the aliased component of the signal in the dc to 5MHz baseband. There is, however, no need to sample at this high rate, so we may choose any sampling frequency 10MHz or greater which is an integer sub-multiple of 70MHz, i.e.,  $70 \div 2 = 35.000\text{MHz}$ ,  $70 \div 3 = 23.333\text{MHz}$ ,  $70 \div 4 = 17.500\text{MHz}$ ,  $70 \div 5 = 14.000\text{MHz}$ ,  $70 \div 6 = 11.667\text{MHz}$ , or  $70 \div 7 = 10.000\text{MHz}$ . We will therefore choose the lowest possible sampling rate of 10.000MHz ( $70 \div 7$ ).

# INTERMEDIATE FREQUENCY (IF) SIGNAL AT 72.5MHz ( $\pm 2$ MHz) IS ALIASED BETWEEN DC AND 5MHz BY SAMPLING AT 10MSPS

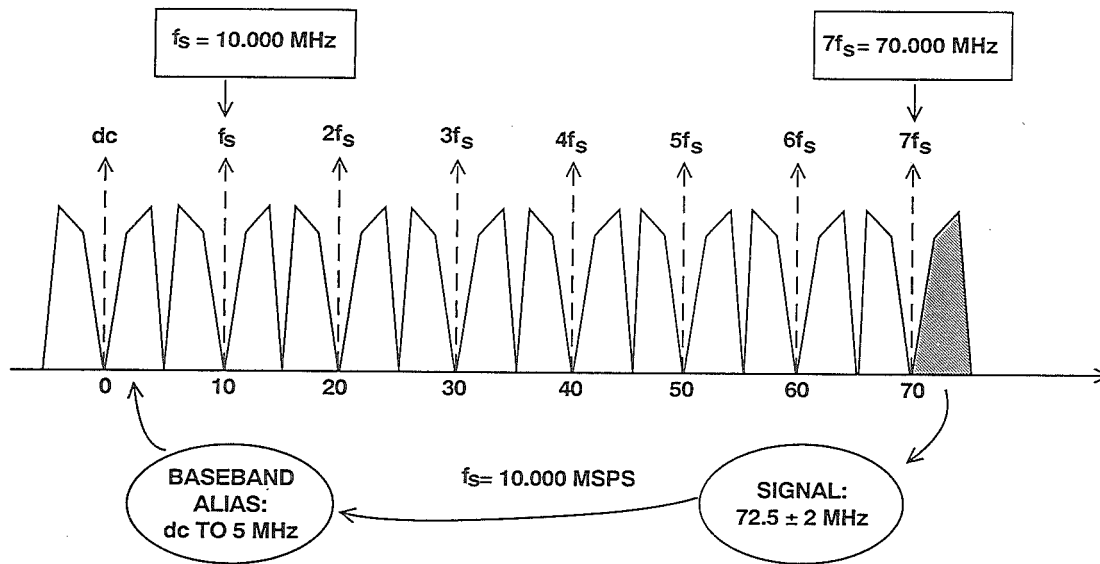


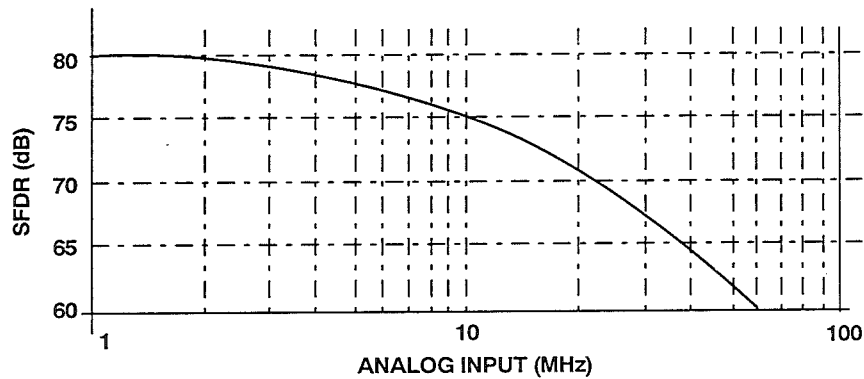
Figure 4.26

There is an advantage in choosing a sampling frequency which is a sub-multiple of the lower band-edge in that there is no frequency inversion in the baseband alias as would be the case for a sampling frequency equal to a sub-multiple of the ~~lower~~ <sup>upper</sup> band-edge. (Frequency inversion can be easily dealt with in the DSP software should it occur, so the issue is not very important).

The next step is to select an ADC which has sufficient dynamic range with a 70

to 75MHz input to meet our system requirement. In most radar receivers, a SFDR of 60 to 80dB is desirable. Unfortunately, this requirement will not be met with standard Nyquist-sampling ADCs due to degradations which occur at high input frequencies. Figure 4.27 shows the SFDR of the AD9022 12 bit, 20MSPS ADC, which represents one of the best monolithic designs available. Note that at 1MHz the SFDR is 80dB, but at the IF frequency of 70MHz, the SFDR of the device is less than 60dB.

## SPURIOUS FREE DYNAMIC RANGE OF THE AD9022 12-BIT, 20MSPS ADC FOR $f_s = 10\text{MSPS}$



4

Figure 4.27

Meeting this performance requirement of 80dB SFDR requires the addition of an external wide-bandwidth, low distortion sample-and-hold, such as the AD9100 as shown in Figure 4.28. The external SHA serves to hold the signal

constant during the ADC conversion cycle. The ADC sees a dc value during the hold-time of the external SHA. The process of optimizing the design for the best SFDR is not simple, and involves many tradeoffs.

## THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

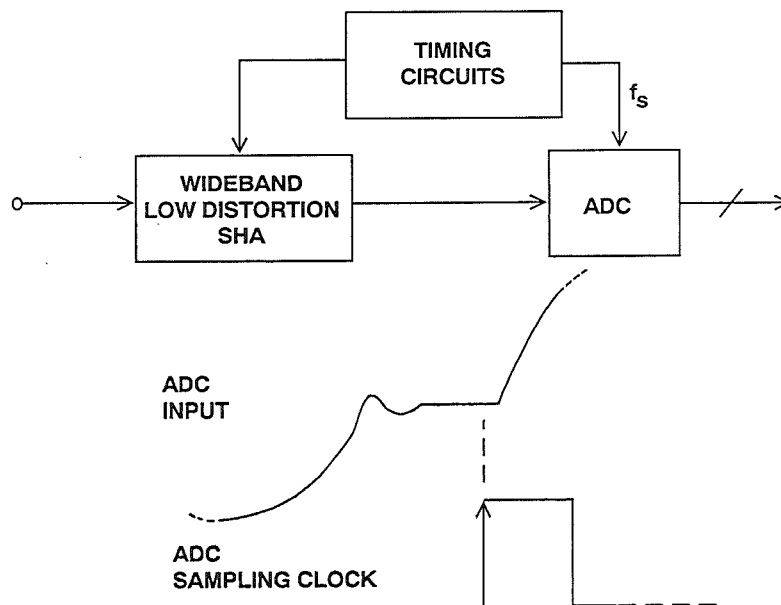


Figure 4.28



The first step in the process is to select an ADC which has sufficient SFDR at low frequencies. The low frequency distortion of an ADC is an indicator of the inherent non-linearity in the dc transfer function. The addition of an ideal external SHA will do nothing to improve on this basic performance. The best you can expect the SHA to do is to extend the low frequency performance of the ADC to higher frequencies. Because of its excellent low frequency distortion ( $-80\text{dBc}$  @  $1\text{MHz}$ ), the AD9022 is good choice.

The next step is to select a low distortion SHA which will maintain sufficient dynamic performance at the IF frequency. Most SHAs are specified for distortion when operating in the track mode. What is of real interest, however, is the signal distortion in the hold mode when the SHA is operating dynamically. The AD9100 and AD9101 are ultra-fast SHAs and are specified in terms of hold-mode distortion. The measurement is done using a high performance low distortion ADC (such as the AD9014 14-bit,  $10\text{MSPS}$ ) to digitize the held value of the SHA output. An FFT is performed on the ADC output, and the distortion is measured digitally. For sampling rates greater than  $10\text{MSPS}$ , the ADC is clocked at an integer sub-multiple of the SHA sampling frequency. This causes a frequency translation in the FFT output because of undersampling, but the distortion measurement still represents that of the SHA operating at the higher sampling rate.

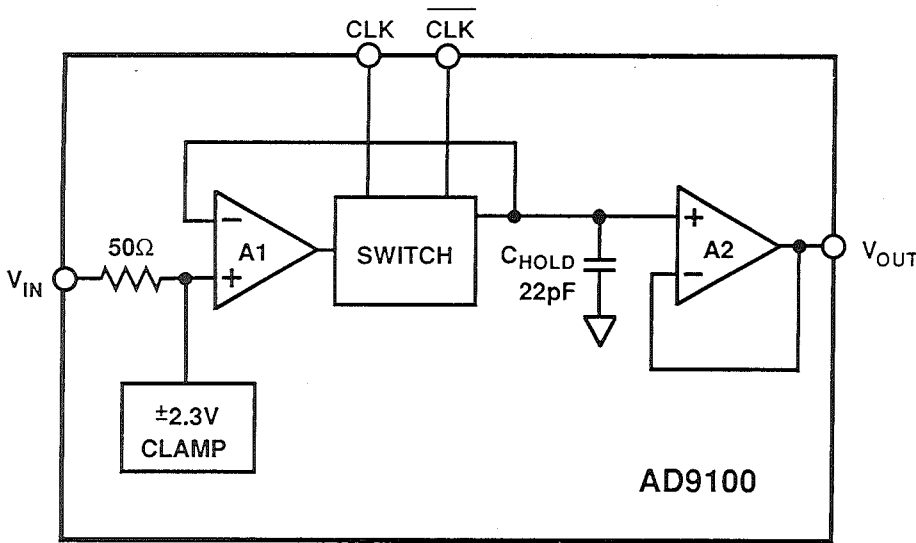
The AD9100 is optimized for low distortion operation up to  $30\text{MSPS}$ , while the AD9101 will provide low distortion performance up to a sampling rate of  $125\text{MSPS}$ .

A block diagram of the AD9100 track-and-hold is shown in Figure 4.29. The switching bridge is integrated into the first stage closed-loop input amplifier. This innovation provides error (distortion) correction for both the switch and amplifier, while still achieving slewrates representative of a more traditional open-loop design. The device has a  $250\text{MHz}$  input bandwidth and a  $16\text{ns}$  acquisition time to  $0.01\%$ .

However, the distortion performance of the AD9100 can be optimized by reducing the input signal level. This will decrease the signal-to-noise ratio, but will also reduce the distortion produced by the switching bridge nonlinearity.

The test configuration shown in Figure 4.30 was used to collect the AD9100 performance data for low amplitude input signals. The data shown in Figure 4.31 was taken at a  $10\text{MSPS}$  sampling rate for three input amplitudes. For each amplitude, the gain of the AD9618 op amp was adjusted so that its output exactly filled the  $2\text{V}$  p-p input range of the AD9014 ADC. Notice that the SFDR is optimum ( $70\text{dBc}$ ) for a  $200\text{mV}$  p-p input signal to the AD9100, and a corresponding post-amplifier gain of 10.

AD9100 MONOLITHIC 30MSPS TRACK-AND-HOLD



4

Figure 4.29

TEST CONFIGURATION AND TIMING FOR MEASURING AD9100 HOLD-MODE SFDR AT 10MSPS

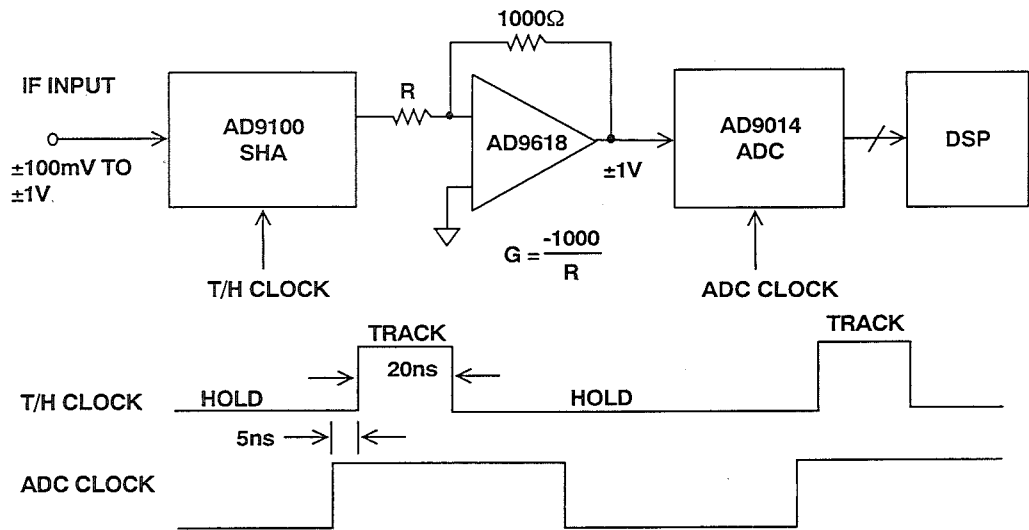


Figure 4.30

# AD9100 HOLD-MODE SFDR MEASURED WITH AD9014 ADC SAMPLING AT 10MSPS

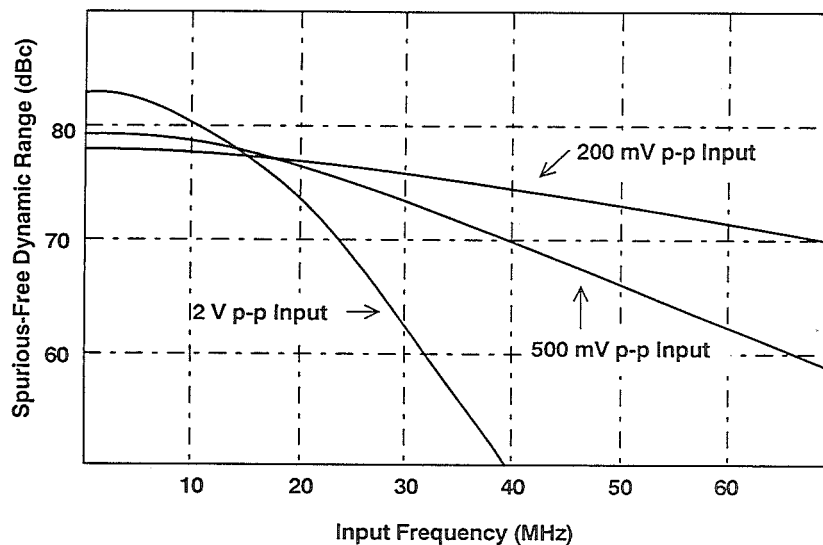


Figure 4.31

The performance of the AD9100 driving the AD9022 under identical conditions yielded the FFT spectrum shown in

Figure 4.32. The 72MHz SFDR is greater than 70dBc, and the measured SNR is 62dB.

## FFT OUTPUT FOR AD9100 DRIVING AD9022 ADC, INPUT = 200mV p-p, G = 10, $f_s = 10\text{MSPS}$ , $f_{in} = 71.4\text{MHz}$

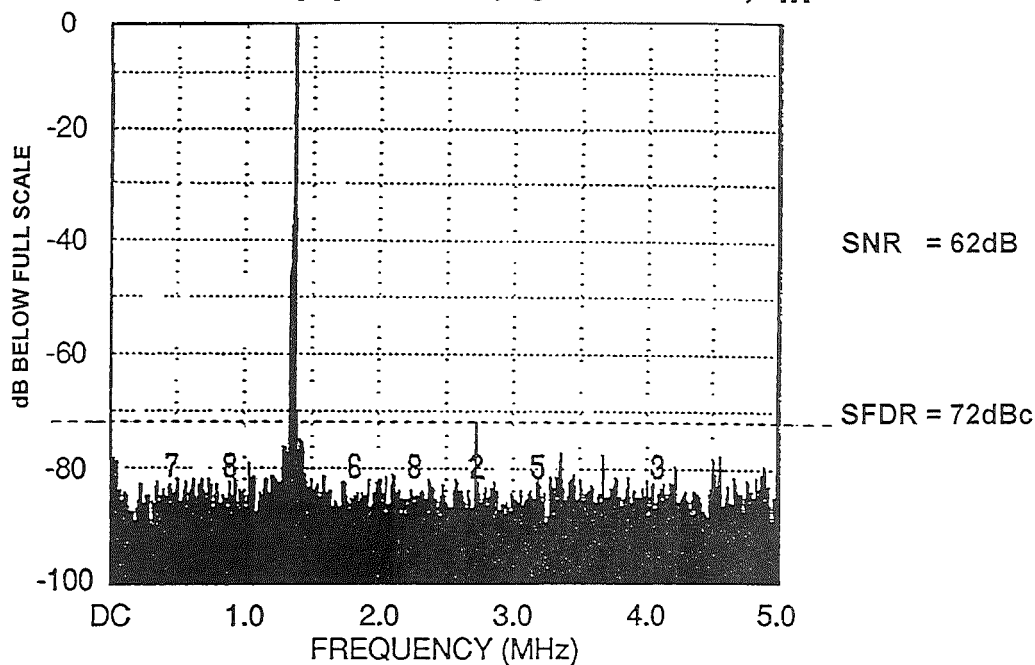


Figure 4.32

The tradeoff in optimizing the circuit for the best SFDR is the increase in overall noise resulting from the high-gain post-amplifier amplifying the hold-mode noise of the AD9100.

The other part of a successful wide-dynamic range design involves the optimization of the timing between the SHA and the ADC. This involves even more tradeoffs. The SHA acquisition time should be long enough to achieve the desired accuracy, but short enough to allow sufficient hold-time for the ADC front-end to settle and yield a low-distortion conversion. For the example above, the optimum performance was achieved using an acquisition time of 20ns and a track time of 80ns. As shown in Figure 4.30, the ADC is clocked close to the end of the SHA's

hold time. Best performance in designs such as these is always achieved by optimizing the timing in the actual circuit.

Similar dynamic range improvements can be achieved with high speed flash converters at higher sampling rates using the AD9101 SHA whose block diagram is shown in Figure 4.33. The AD9101 is a track-and-hold with an internal post-amplifier. This configuration allows the front end sampler to operate at relatively low signal amplitudes, resulting in dramatic improvement in hold-mode distortion at high input frequencies and sampling rates up to 125MSPS. The AD9101 has an input bandwidth of 350MHz and an acquisition time of 7ns to 0.1% and 11ns to 0.01%.

4

### AD9101 125MSPS SAMPLING AMPLIFIER

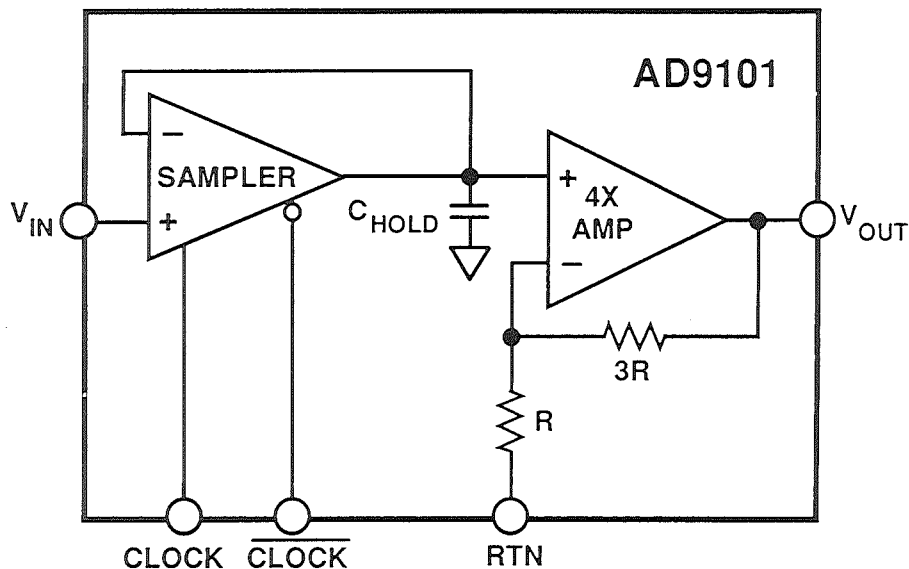


Figure 4.33

A block diagram and a timing diagram is shown for the AD9101 driving the AD9002 8 bit flash converter at 125MSPS (see Figure 4.34). The corre-

sponding dynamic range with and without the AD9101 is shown in Figure 4.35.



## AD9002 DYNAMIC PERFORMANCE WITH AND WITHOUT AD9101 SHA



tions as will be described in the next section.

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## SECTION 5

### DATA CONVERTERS

- DC Errors in Data Converters
- AC Errors in Data Converters
- AC Errors in DACs
- AC Errors in ADCs
- Components and Processes for Data Converters
- DAC Structures
- DAC Logic
- ADC Structures:
  - Comparators, Flash or Parallel ADCs, Subranging ADCs, Integrating ADCs, Voltage-to-Frequency Converter/Counter ADCs, Tracking ADCs, Successive Approximation ADCs, Sigma-Delta ADCs, Sample-and-Hold Amplifiers (SHAs)



## SECTION 5

## DATA CONVERTERS

*James Bryant, Walt Kester*

## INTRODUCTION

This section is intended as an introduction to the techniques used in the design of digital-to-analog and analog-to-digital converters (DACs and ADCs, respectively). There is a common misconception that as digital computing becomes more ubiquitous and less expensive, analog circuitry will soon disappear altogether. In fact, nothing could be further from the truth - the entire universe above the quantum level is analog, and the more ubiquitous digital computers become, the more analog transducers and circuitry will be necessary to interface them to the real world.

DACs and ADCs are these interfaces between the analog and digital worlds. A DAC is a device which gives an ana-

log output related to a digital input, while an ADC gives a digital output in response to an analog input (see Figure 5.1). While DACs and ADCs do exist which have intentionally nonlinear transfer characteristics, they are not common, and will not be considered here. If we disregard such nonlinear exceptions, we can say that a DAC is a circuit whose analog output is proportional to both its analog reference and to the value of its digital input. Conversely, an ADC is a circuit whose digital output is proportional to the ratio of its analog input to its analog reference. (Often, but by no means always, the scaling factor between the analog reference and the analog signal is unity, so the digital signal represents the normalized ratio of the two.)

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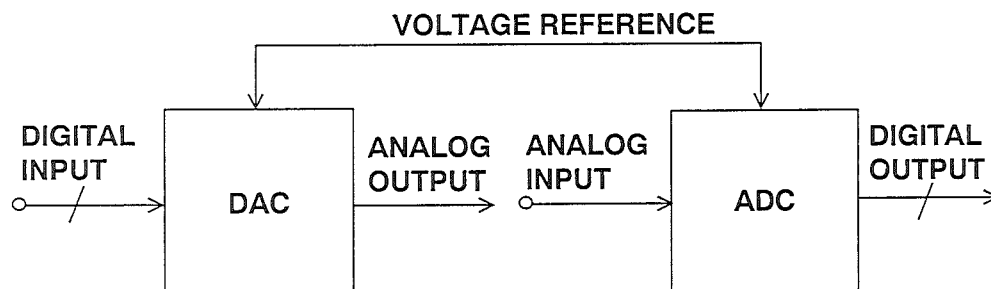
DIGITAL-TO-ANALOG AND  
ANALOG-TO-DIGITAL CONVERTERS

Figure 5.1

The most important thing to remember about both DACs and ADCs is that one of the signals is digital, and therefore quantized. That is, an N-bit word represents one of  $2^N$  possible states, and therefore an N-bit DAC (with a fixed reference) can have only  $2^N$  possible analog outputs, and an N-bit ADC can have only  $2^N$  possible digital outputs.

The analog signals will generally be voltages or currents, but may be resistance, and can be any analog quantity, not necessarily an electrical one. Such cases, where a transducer is integrated with a data converter, are less common, but certainly not unknown. The most

common are optical: DACs with light output and ADCs with integral photocells.

The resolution of data converters may be expressed in several different ways: The weight of the Least Significant Bit (LSB), parts per million of full scale (ppm FS), millivolts (mV), etc. Different devices (even from the same manufacturer) will be specified differently, so converter users must learn to translate between the different types of specifications if they are to compare devices successfully. The size of the least significant bit for various resolutions is shown in Figure 5.2.

### THE SIZE OF A LEAST SIGNIFICANT BIT (LSB)

RESOLUTION N	$2^N$	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	-12
4-bit	16	625 mV	62,500	6.25	-24
6-bit	64	156 mV	15,625	1.56	-36
8-bit	256	39.1 mV	3,906	0.39	-48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	-60
12-bit	4,096	2.44 mV	244	0.024	-72
14-bit	16,384	610 $\mu$ V	61	0.0061	-84
16-bit	65,536	153 $\mu$ V	15	0.0015	-96
18-bit	262,144	38 $\mu$ V	4	0.0004	-108
20-bit	1,048,576	9.54 $\mu$ V (10 $\mu$ V)	1	0.0001	-120
22-bit	4,194,304	2.38 $\mu$ V	0.24	0.000024	-132
24-bit	16,777,216	596 nV*	0.06	0.000006	-144

\* 600nV is the Johnson Noise in a 10kHz BW of a 2.2k $\Omega$  Resistor @ 25°C

Remember: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%  
All other values may be calculated by powers of 2

Figure 5.2

Before we can consider the various architectures used in data converters, it is necessary to consider the performance to be expected, and the specifications which are important. The next three parts of this section will consider

the definitions of errors and specifications used for data converters, so that when we consider particular architectures, we can understand their strengths and weaknesses.

## DC ERRORS IN DATA CONVERTERS

The first applications of data converters were in measurement and control applications where the exact timing of the conversion was usually unimportant, and the data rate was slow. In such applications, the DC specifications of converters are important, but timing and AC specifications are not. Today many, if not most, converters are used in "sampling" and "reconstruction" systems where AC specifications are critical (and DC ones may not be) - these will be considered in the next part of this section.

Figure 5.3 shows the ideal transfer characteristics for a 3-bit unipolar DAC, and Figure 5.4 a 3-bit unipolar ADC. In a DAC, both the input and the output are quantized, and the graph consists of eight points - while it is reasonable to discuss the line through these points, it is very important to remember that the actual transfer characteristic is *not* a line, but a number of discrete points.

### TRANSFER FUNCTION FOR IDEAL 3-BIT DAC

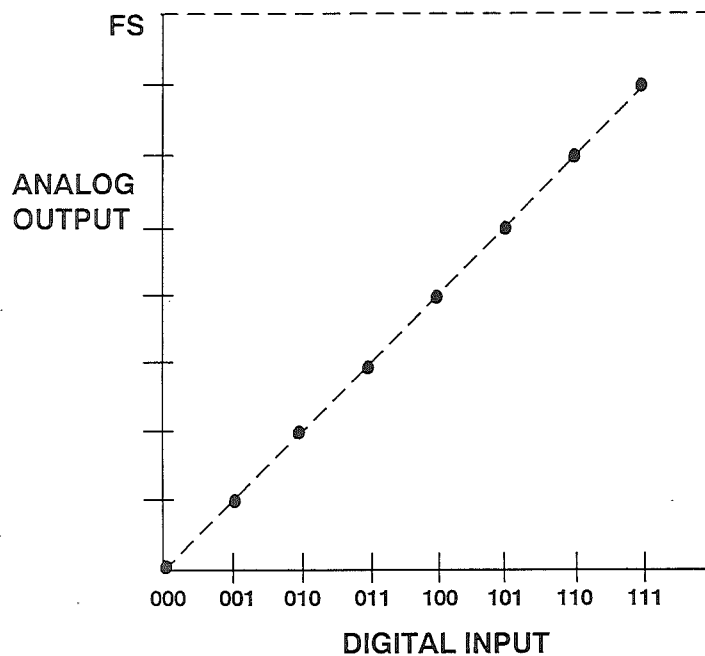


Figure 5.3

## TRANSFER FUNCTION FOR IDEAL 3-BIT ADC

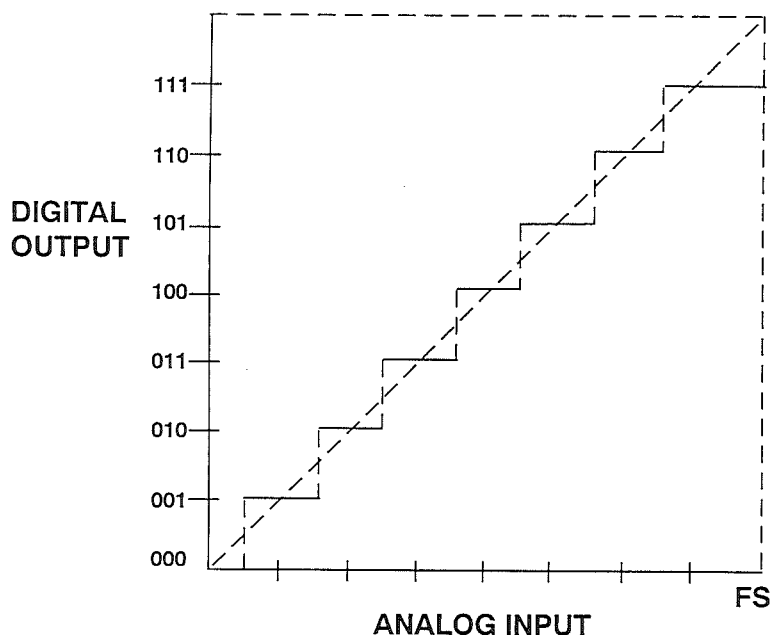


Figure 5.4

The input to an ADC is analog and is not quantized, but its output is quantized. The transfer characteristic therefore consists of eight horizontal steps (when considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps).

In both cases, digital full scale (all "1"s) corresponds to 1 LSB below the analog full scale (the reference, or some multiple thereof). This is because, as mentioned above, the digital code represents the *normalized* ratio of the analog signal to the reference. If this were unity, the digital code would be all "0"s and "1" in the bit *above* the Most Significant Bit (MSB).

The (ideal) ADC transitions take place at  $\frac{1}{2}$  LSB above zero, and thereafter every LSB, until  $\frac{1}{2}$  LSB below analog full scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to  $\frac{1}{2}$  LSB between the actual analog input and the exact value of the digital output. This is known as the "quantization error" or "quantization uncertainty" as shown in Figure 5.5. In AC (sampling) applications this quantization error gives rise to "quantization noise" which will be discussed in the next section.

**AN ANALOG INPUT OF  $\pm 1/2$  LSB ON NOMINAL  
GIVES THE SAME DIGITAL OUTPUT --  
THIS IS THE *QUANTIZATION UNCERTAINTY***

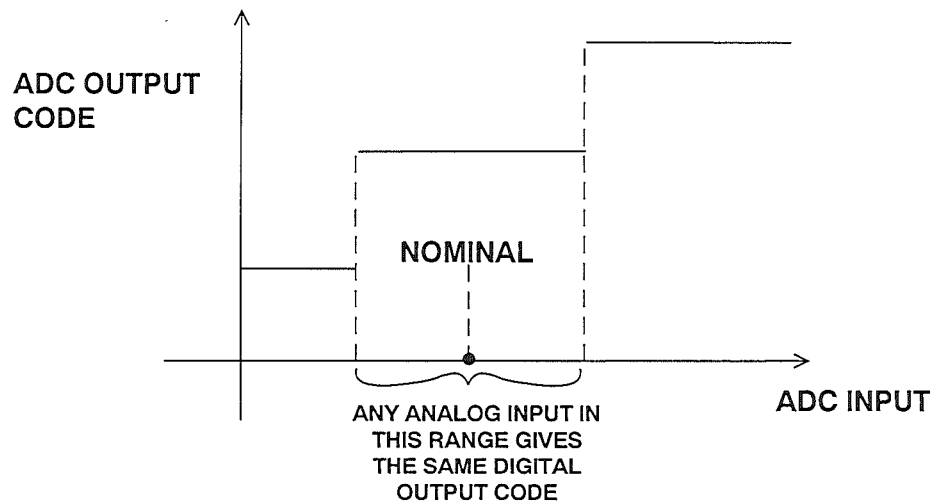


Figure 5.5

There are many possible digital coding schemes for data converters: *binary*, *offset binary*, *1's complement*, *2's complement*, *gray code*, *BCD* and others. This section, being devoted mainly to the *analog* issues surrounding data converters, will use simple *binary* and *offset binary* in its examples and will not consider the merits and disadvantages of these, or any other, forms of digital code.

The examples in Figures 5.3 and 5.4 use unipolar converters, whose analog port has only a single polarity. These are the simplest type, but bipolar converters are more generally useful. There are two types of bipolar con-

verter: the simpler is merely a unipolar converter with an accurate 1 MSB of negative offset (and many converters are arranged so that this offset may be switched in and out so that they can be used as either unipolar or bipolar converters at will), but the other, known as a *sign-magnitude* converter is more complex, and has N bits of magnitude information and an additional bit which corresponds to the sign of the analog signal. Sign-magnitude DACs are quite rare, and sign magnitude ADCs are found mostly in digital voltmeters (DVMs). Figure 2.6 shows the transfer functions for these unipolar, offset bipolar, and sign-magnitude bipolar codes.



## UNIPOLAR AND BIPOLAR CONVERTER CODES

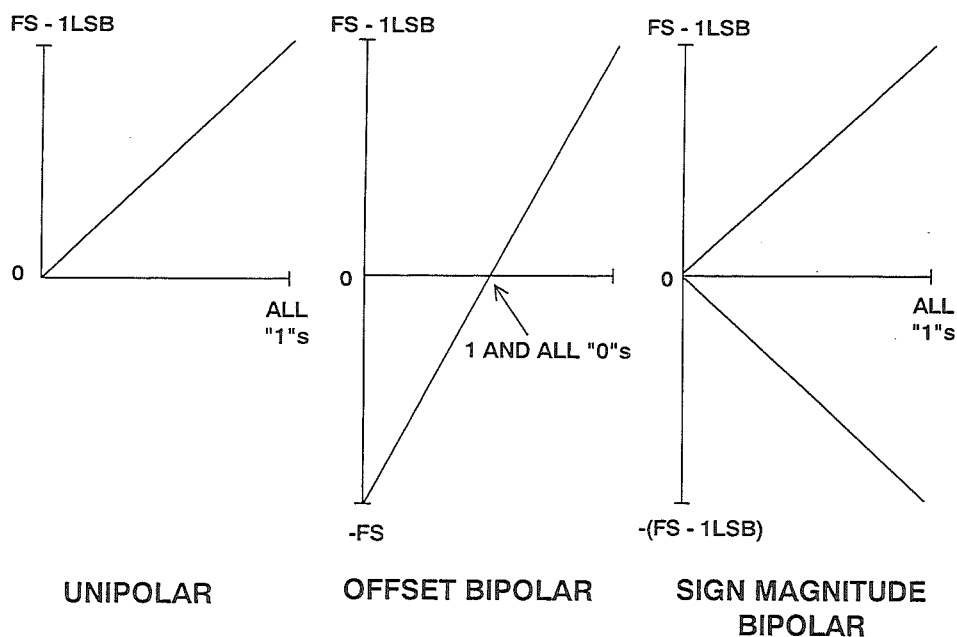


Figure 5.6

The four DC errors in a data converter are offset error, gain error, and two types of linearity error. Offset and gain errors are analogous to offset and gain errors in amplifiers (see Figure 5.7). (Though offset error and zero error, which are identical in amplifiers and unipolar data converters, are not identical in bipolar converters and should be carefully distinguished.) The transfer characteristics of both DACs and ADCs may be expressed as  $D = K + GA$ , where  $D$  is the digital code,  $A$  is the analog signal, and  $K$  and  $G$  are constants. In a unipolar converter,  $K$  is zero, and in an offset bipolar converter, it is  $-1$  MSB.

The offset error is the amount by which the actual value of  $K$  differs from its ideal value. The gain error is the amount by which  $G$  differs from its ideal value, and is generally expressed as the percentage difference between the two, although it may be defined as the gain error contribution (in mV or LSB) to the total error at full scale. These errors can usually be trimmed by the data converter user. Note, however, that amplifier offset is trimmed at zero input, and then the gain is trimmed near to full scale. The trim algorithm for a bipolar data converter is not so straightforward.

## CONVERTER OFFSET AND GAIN ERROR

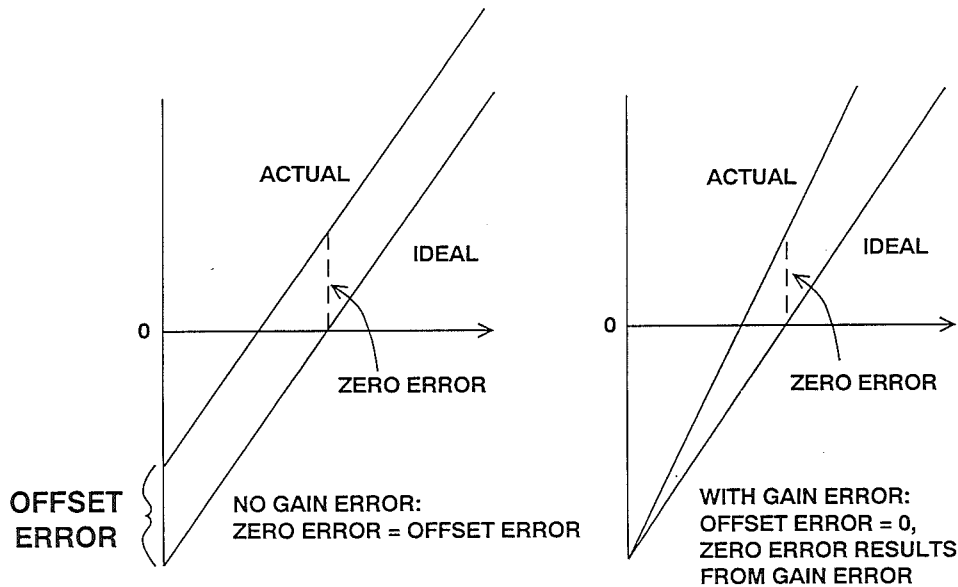


Figure 5.7

The integral linearity error of a converter is also analogous to the linearity error of an amplifier, and is defined as the maximum deviation of the actual transfer characteristic of the converter from a straight line, and is generally

expressed as a percentage of full scale (but may be given in LSBs). There are two common ways of choosing the straight line: *end point* and *best straight line* (see Figure 5.8).

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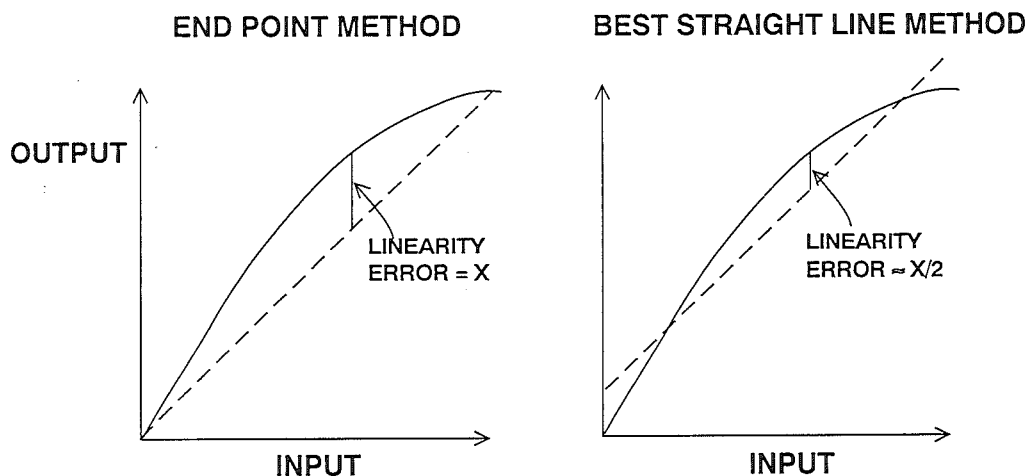
METHOD OF MEASURING INTEGRAL LINEARITY ERRORS  
(SAME CONVERTER ON BOTH GRAPHS)

Figure 5.8

In the end point system, the deviation is measured from the straight line through the origin and the full scale point (after gain adjustment). This is the most useful integral linearity measurement for measurement and control applications of data converters (since error budgets depend on deviation from the ideal transfer characteristic, not from some arbitrary "best fit"), and is the one normally adopted by Analog Devices Inc.

The best straight line, however, does give a better prediction of distortion in AC applications, and also gives a lower value of "linearity error" on a data sheet. The best fit straight line is drawn through the transfer characteristic of the device using standard curve fitting techniques, and the maximum deviation is measured from this line. In general, the integral linearity error measured in this way is only 50% of the value measured by end point methods. This makes the method good for producing impressive data sheets, but it is less useful for error budget analysis. For AC applications, it is even better to specify distortion than DC linearity, so it is rarely necessary to use the best straight line method to define converter linearity. Analog Devices uses this definition on data sheets only in the case of second-source products where the original manufacturer's data sheet used best straight line, rather than end point, linearity.

The other type of converter non-linearity is "differential non-linearity" (DNL). This relates to the linearity of the code transitions of the converter. In the ideal

case, a change of 1 LSB in digital code corresponds to a change of exactly 1 LSB of analog signal. In a DAC, a change of 1 LSB in digital code produces exactly 1 LSB change of analog output, while in an ADC there should be exactly 1 LSB change of analog input to move from one digital transition to the next.

Where the change in analog signal corresponding to 1 LSB digital change is more or less than 1 LSB, there is said to be a DNL error. The DNL error of a converter is normally defined as the maximum value of DNL to be found at any transition.

If the DNL of a DAC is less than  $-1$  at any transition (see Figure 5.9), the DAC is "non-monotonic" i.e., its transfer characteristic contains one or more maxima or minima. A DNL greater than  $+1$  does not cause non-monotonicity, but is still undesirable. In many DAC applications (especially closed-loop systems where non-monotonicity can change negative feedback to positive feedback), it is critically important that DACs are monotonic. DAC monotonicity is often explicitly specified on data sheets, although if the DNL is guaranteed to be less than 1 LSB (i.e.,  $|DNL| \leq 1\text{LSB}$ ) then the device must be monotonic, even without an explicit guarantee.

ADCs can be non-monotonic, but a more common result of excess DNL in ADCs is missing codes (see Figure 5.10). Missing codes (or non-monotonicity) in an ADC are as objectionable as non-monotonicity in a DAC. Again, they result from  $DNL > 1\text{LSB}$ .

### TRANSFER FUNCTION OF NON-IDEAL 3-BIT DAC SHOWS DIFFERENTIAL NON-LINEARITY AND NON-MONOTONICITY

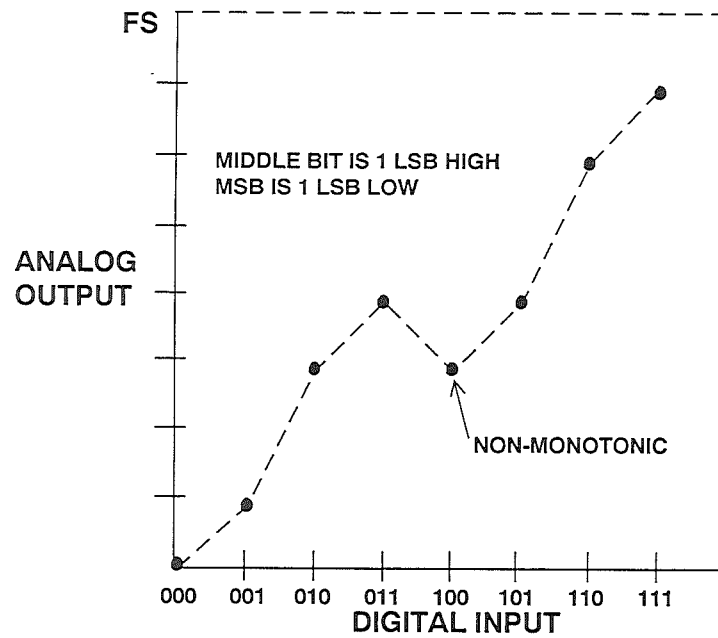


Figure 5.9

### TRANSFER FUNCTION OF NON-IDEAL 3-BIT ADC SHOWS DIFFERENTIAL NON-LINEARITY AND MISSING CODE

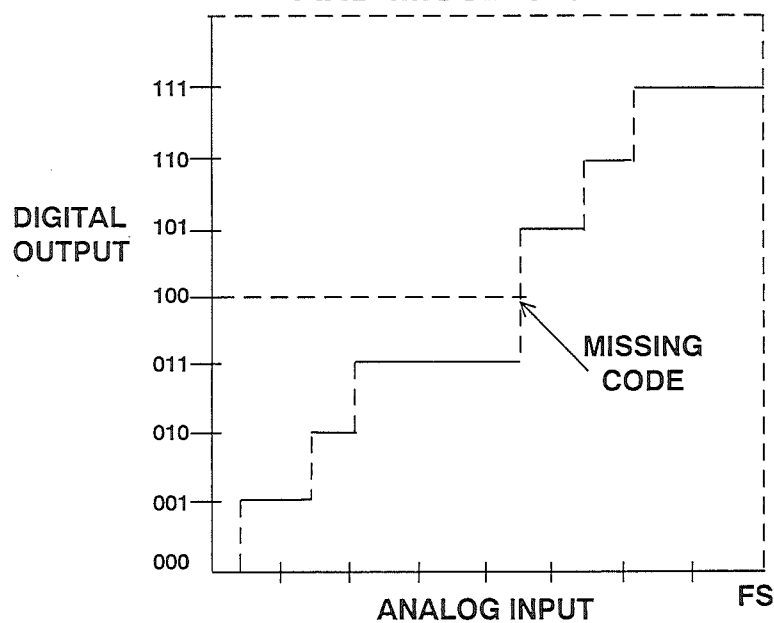


Figure 5.10

Defining missing codes is more difficult than defining non-monotonicity. All ADCs suffer from some transition noise as shown in Figure 5.11 (think of it as the flicker between adjacent values of the last digit of a DVM). As resolutions become higher, the range of input over which transition noise occurs may approach, or even exceed, 1 LSB. In such a case, especially if combined with

a negative DNL error, it may be that there are some (or even all) codes where transition noise is present for the whole range of inputs. There are therefore some codes for which there is no input which will guarantee that code as an output, although there may be a range of inputs which will sometimes produce that code.

### COMBINED EFFECTS OF ADC CODE TRANSITION NOISE AND DNL

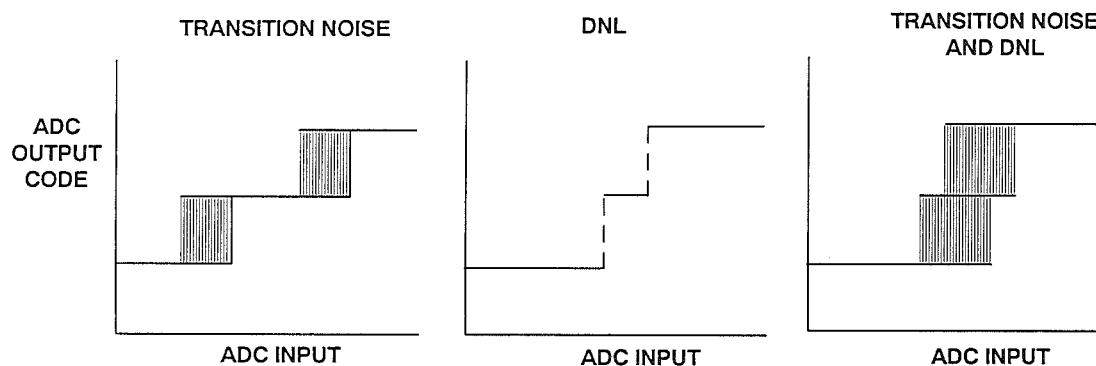


Figure 5.11

For lower resolution ADCs, it may be reasonable to define “no missing codes” as a combination of transition noise and DNL which guarantees some level (perhaps 0.2 LSB) of noise-free code for all codes. However, this is impossible to achieve at the very high resolutions achieved by modern sigma-delta ADCs, or even at lower resolutions in wide

bandwidth sampling ADCs. In these cases, the manufacturer must define noise levels and resolution in some other way. Which method is used is less important, but the data sheet should contain a clear definition of the method used and the performance to be expected.

## AC ERRORS IN DATA CONVERTERS

Over the last decade, the major application of data converters has shifted from DC measurement and control applications to AC sampling and reconstruction. Detailed descriptions and definitions of sampled data systems are beyond the scope of this section, but they are thoroughly discussed in Reference 1 and in Section 4 of this book. In very simple terms, a “sampled data system” is a system where the instantaneous value of an AC waveform is sampled at regular intervals (see Figure 5.12). The resulting digital codes may

be used to store the waveform (as in CDs and DATs), or intensive computation on the samples (Digital Signal Processing, or DSP) may be used to perform filtering, compression, and other operations. The inverse operation, “reconstruction”, occurs when a series of digital codes are fed to a DAC to reconstruct an AC waveform - an obvious example of this is a CD or DAT player, but the technique is very widely used indeed in telecommunications, radio, synthesizers, and many other applications.

### SAMPLED AND RECONSTRUCTED WAVEFORMS

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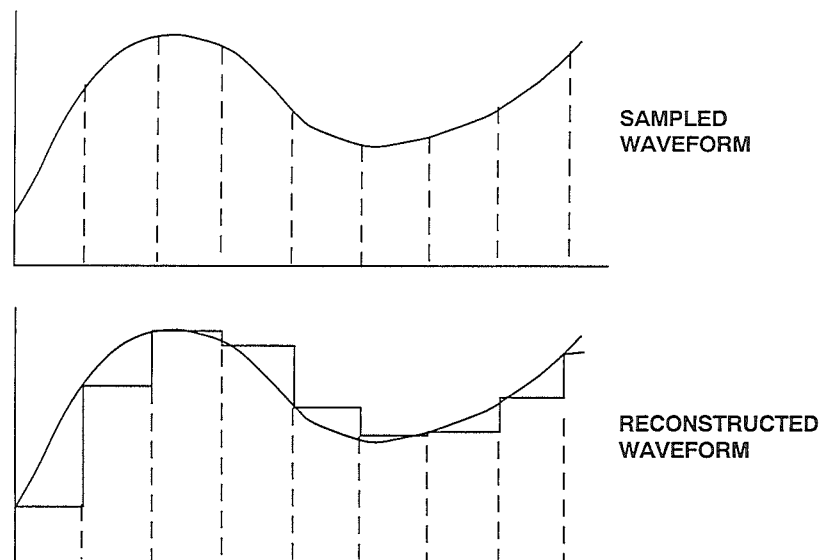


Figure 5.12

The data converters used in these applications must have good performance with AC signals, but may not require good DC specifications. The first high performance converters to be designed for such applications were often manufactured with good AC specifications but poor, or unspecified, DC performance. Today the design tradeoffs are better understood, and

most converters will have good, and guaranteed, AC and DC specifications. DACs for digital audio, however, which must be extremely competitive in price, are generally sold with comparatively poor DC specifications — not because their DC performance is poor, but because it is not tested during manufacture.

While it is easier to discuss the DC parameters of both DACs and ADCs together, their AC specifications are

sufficiently different to deserve separate consideration.

## AC ERRORS IN DACs

The AC specifications which are most likely to be important with DACs are *settling time*, *glitch*, *distortion*, *Spurious Free Dynamic Range (SFDR)*, and *phase noise*.

The settling time of a DAC is the time from a change of digital code to when

the output comes within *and remains within* some error band as shown in Figure 5.13. With amplifiers, it is hard to make comparisons of settling time, since their error bands may differ from amplifier to amplifier, but with DACs the error band will almost invariably be  $\pm 1$  or  $\pm \frac{1}{2}$  LSB.

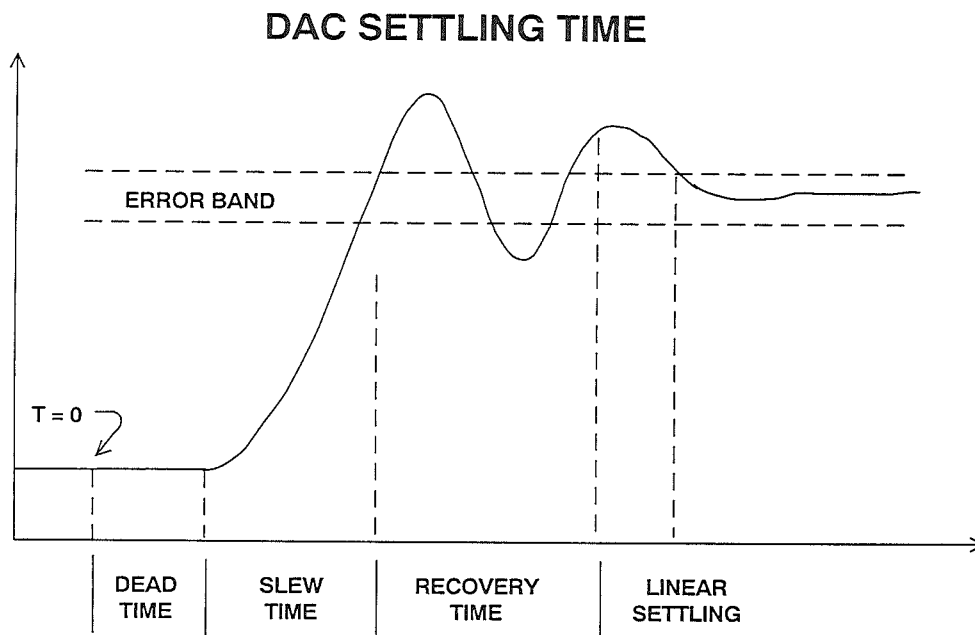


Figure 5.13

The settling time of a DAC is made up of four different periods: the *switching time* or *dead time* (during which the digital switching, but not the output, is changing), the *slewing time* (during which the rate of change of output is limited by the slew rate of the DAC output), the *recovery time* (when the DAC is recovering from its fast slew and may overshoot), and the *linear settling time* (when the DAC output approaches

its final value in an exponential or near-exponential manner). If the slew time is short compared to the other three (as is usually the case with current output DACs), then the settling time will be largely independent of the output step size. On the other hand, if the slew time is a significant part of the total, then the larger the step, the longer the settling time.

Ideally, when a DAC output changes it should move from one value to its new one monotonically. In practice, the output is likely to overshoot, undershoot, or both (see Figure 5.14). This uncontrolled movement of the DAC output during a transition is known as

*glitch*. It can arise from two mechanisms: capacitive coupling of digital transitions to the analog output, and the effects of some switches in the DAC operating more quickly than others and producing temporary spurious outputs.

### DAC TRANSITIONS (SHOWING GLITCH)

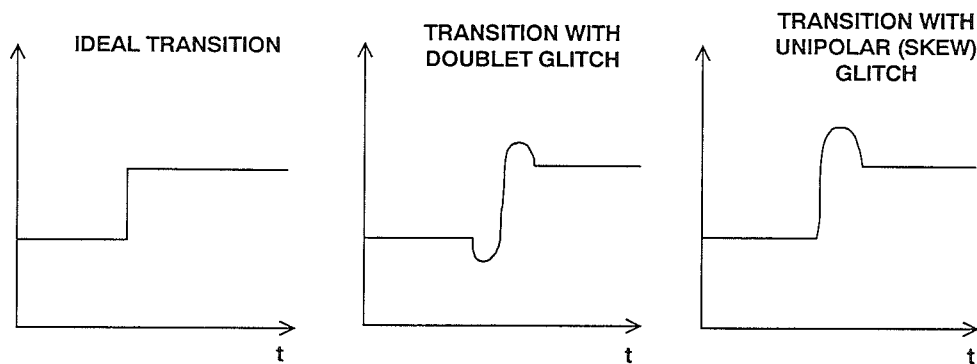


Figure 5.14

Capacitive coupling frequently produces roughly equal positive and negative spikes (sometimes called a *doublet glitch*) which more or less cancel in the longer term. These glitches occur whether or not a reference voltage is present on the DAC. The glitch produced by switch timing differences is generally unipolar, much larger, and does not occur in the absence of a reference (so the effects of capacitive coupling and switch timing may often be observed separately).

Glitch is generally (inaccurately) defined in terms of *glitch energy*. The term

is a misnomer, since the unit is Volt-seconds (or more probably  $\mu\text{V}\cdot\text{sec}$  or  $\text{pV}\cdot\text{sec}$ ), and the magnitude of a glitch is better referred to as the *glitch impulse area*, or simply, *glitch impulse*. The midscale glitch produced by the transition between the codes 1000...000 and 0111...111 is usually the worst glitch. Glitches at other code transition points (such as 1/4 and 3/4 full scale) are generally less. Figure 5.15 shows the midscale glitch for a fast low-glitch DAC.



# AD9720/AD9721 DAC MIDSCALE GLITCH SHOWS 1.34pV-S NET IMPULSE AREA AND SETTLING TIME OF 4.5ns

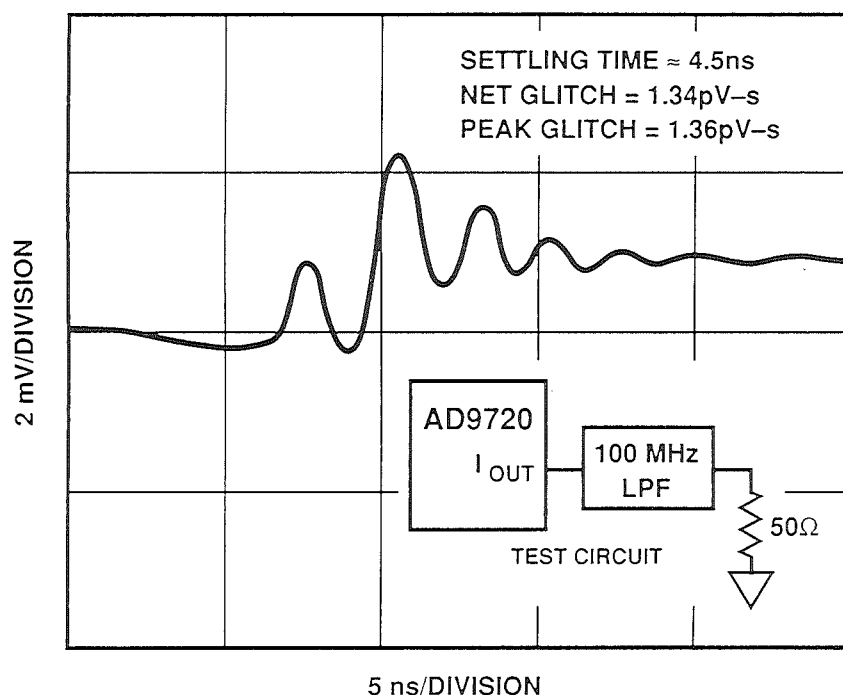


Figure 5.15

If we consider the spectrum of a waveform reconstructed by a DAC from digital data, we find that in addition to the expected spectrum (which will contain one or more frequencies, depending on the nature of the reconstructed waveform), there will also be noise and distortion products. Distortion may be specified in terms of harmonic distortion, Spurious Free Dynamic Range (SFDR), intermodulation distortion, or all of the above. Harmonic distortion is defined as the ratio of harmonics to fundamental when a (theoretically) pure sine wave is reconstructed, and is the most common specification. Spurious free dynamic range is the ratio of the worst spur (usually, but not necessarily always a

harmonic of the fundamental) to the fundamental.

Code-dependent glitches will produce both out-of-band and in-band harmonics when the DAC is reconstructing a digitally generated sinewave (as in a Direct Digital Synthesis (DDS) system). The midscale glitch occurs twice during a single cycle of a reconstructed sinewave (at each midscale crossing), and will therefore produce a second harmonic of the sinewave, as shown in Figure 5.16. Note that the higher order harmonics of the sinewave, which alias back into the Nyquist bandwidth (DC to  $f_s/2$ ), cannot be filtered.

## EFFECTS OF CODE-DEPENDENT DAC GLITCHES ON SPECTRAL OUTPUT

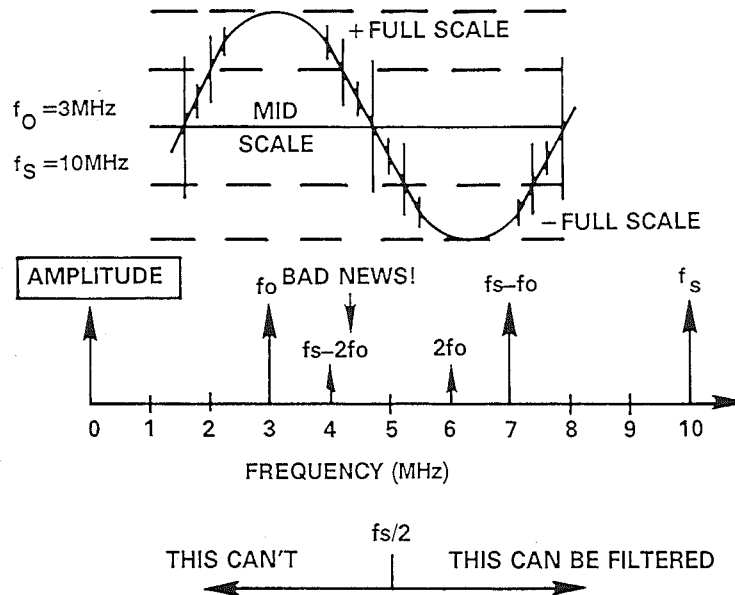


Figure 5.16

It is difficult to predict the harmonic distortion or SFDR from the glitch specification alone. Other factors, such as the overall linearity of the DAC, also contribute to distortion. It is therefore customary to test reconstruction DACs in the frequency domain (using a spectrum analyzer) at various clock rates and output frequencies. Typical spectral outputs for the AD9721 10 bit DAC are shown in Figure 5.17. The clock rate is 50MSPS, and the output frequencies are 5.10MHz and 16.60MHz, respectively. The AD9955 DDS chip is used to

generate the digital sinewave. A detailed discussion of such systems is beyond the scope of this section; however a complete discussion of high speed DACs and DDS may be found in Section 17 of Reference 2.

DACs also produce spurious frequency domain products because of the quantization process (dividing the DAC output signal range into  $2^N$  discrete values). Because quantization theory is identical for both ADCs and DACs, it is discussed in the next section.

# AD9955 DDS AND AD9721 DAC SPECTRAL OUTPUT FOR CLOCK FREQUENCY OF 50MSPS

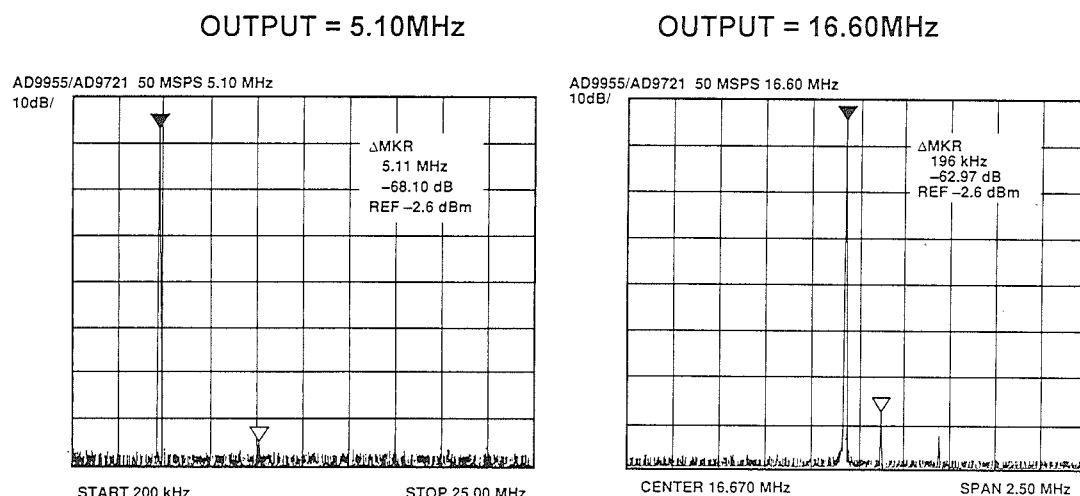


Figure 5.17

## AC ERRORS IN ADCs

The AC specifications of ADCs include *harmonic* and *intermodulation distortion*, *Spurious Free Dynamic Range* (SFDR), *full-power bandwidth* (FPBW), *effective number of bits* (ENOB), and *sampling clock jitter*. We must also consider quantization noise.

When we discussed the DC performance of ADCs, we pointed out that the input of an ADC is analog and therefore has infinite resolution, but the output is quantized into  $2^N$  steps. The difference between analog input and the exact value of the digital output it produces is the quantization error. The same phenomenon occurs in AC systems, producing quantization noise. Mathematically predicting the precise spectral content of the quantization noise as a function of the input signal is quite difficult. In many cases, however, the quantization noise is relatively uncorrelated to the input signal. When this is the case, the quantization noise behaves as broad-band noise with a uniform spectral

density between DC and one-half the sampling frequency.

The rms quantization noise voltage of an ADC in the Nyquist band ( $DC - f_s/2$ ) is  $q/\sqrt{12}$ , where  $q$  is the value of the LSB. From this, we can calculate that the signal-to-noise ratio (SNR) of a perfect  $N$ -bit ADC with a full scale sine wave input signal is limited to  $(6.02N + 1.76)$  dB by quantization noise. Like the Johnson noise of a perfect resistor, quantization noise is a fundamental, and cannot be improved by changes in converter design. However, again like Johnson noise, we can redesign systems so that its effects are less damaging.

Quantization noise may be fundamental, but most high resolution ADCs have noise or distortion sources that are larger than the quantization noise, and which reduce their effective resolution to less than the number of bits given on their data sheets.

## QUANTIZATION NOISE

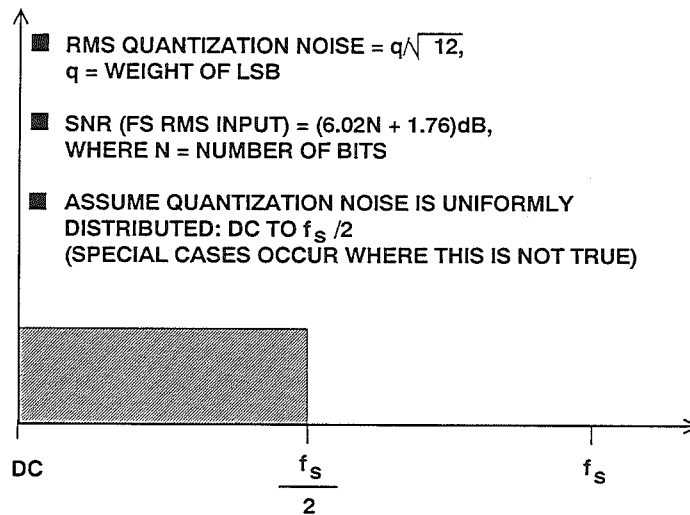


Figure 5.18

If we plot the gain of an amplifier with a small signal of a few millivolts or tens of millivolts, we find that as we increase the input frequency, there is a frequency at which the gain has dropped by 3 dB. This frequency is the upper limit of the “small signal bandwidth” of the amplifier and is set by the internal pole(s) in the amplifier response. If we drive the same amplifier with a large signal so that the output stage swings with its full rated peak to peak output voltage, we *may* find that the upper 3 dB point is at a lower frequency, being limited by the slew rate of the amplifier output stage. This high level 3 dB point defines the “large signal bandwidth” of the amplifier. When defining the large signal bandwidth of an amplifier, a number of variables must be considered, including the power supply, the

output amplitude (if slew rate is the only limiting factor, it is obvious that if the signal amplitude is halved, the “large signal bandwidth” is doubled), and the load. Thus “large signal bandwidth” is a rather uncertain parameter in an amplifier, since it depends on so many uncontrolled variables - in cases where the large signal bandwidth is less than the small signal bandwidth, it is better to define the output slew rate and calculate the maximum output swing at any particular frequency. In an ADC, however, the maximum swing is always full-scale, and the load seen by the signal is defined. It is therefore quite reasonable to define the large signal bandwidth (or full-power bandwidth) of an ADC and report it on the data sheet.

## ADC LARGE SIGNAL (OR FULL POWER) BANDWIDTH

- With Small Signal, the Bandwidth of a Circuit is limited by its Overall Frequency Response.
- At High Levels of Signal the Slew Rate of Some Stage May Control the Upper Frequency Limit.
- In Amplifiers There are so many Variables that *Large Signal Bandwidth* needs to be Redefined in every Individual Case, and *Slew Rate* is a more Useful Parameter for a Data Sheet.
- In ADCs the Maximum Signal Swing is the ADC's Full Scale Span, and is therefore Defined, so *Full Power Bandwidth* (FPBW) may Appear on the Data Sheet.
- HOWEVER the FPBW Specification Says Nothing About Distortion Levels. Effective Number of Bits (ENOB) is Much More Useful in Practical Applications.

Figure 5.19

However, the large signal bandwidth tells us the frequency at which the amplitude response of the ADC drops by 3 dB — it tells us nothing at all about the relationship between distortion and frequency. If we study the behavior of an ADC as its input frequency is increased, we discover that, in general, noise and distortion increase with frequency. This reduces the resolution that we can obtain from the ADC.

If we draw a graph of the ratio of signal to noise plus distortion of a converter against its input frequency, we find a much more discouraging graph than that of its frequency response. The ratio of signal to noise plus distortion can be expressed in dB or as an effective number of bits (ENOB). As we have seen above, the SNR of a perfect N-bit ADC (with a full-scale sine input) is

$(6.02N + 1.76)$  dB. If we have an ADC with an SNR of X dB with a particular input, then we can solve the equation:

$$\text{ENOB} = \frac{\text{XdB} - 1.76\text{dB}}{6.02\text{dB}}$$

and determine the *effective* resolution of the converter with that input. A graph of ENOB against variations of input amplitude and frequency can be depressing when we see just how little of the DC resolution of the ADC can actually be used, but can sometimes show interesting features: the ADC in Figure 5.21, for instance, has a larger ENOB for signals at 10% of FS at 1 MHz than for FS signals of the same frequency - a simple frequency response curve cannot have plots crossing in this way.

## EFFECTIVE NUMBER OF BITS (ENOB) INDICATES DYNAMIC PERFORMANCE OF ADCs

- $\text{SNR} = 6.02N + 1.76\text{dB}$  (THEORETICAL)
- ADC ACHIEVES  $\text{SNR} = X\text{dB}$  (ACTUAL)
- $\text{ENOB} = \frac{X\text{dB} - 1.76\text{dB}}{6.02\text{dB}}$
- ENOB INCLUDES: NOISE AND DISTORTION, DC TO  $f_s/2$

5

Figure 5.20

## ADC GAIN AND ENOB VERSUS FREQUENCY SHOWS IMPORTANCE OF ENOB SPECIFICATION

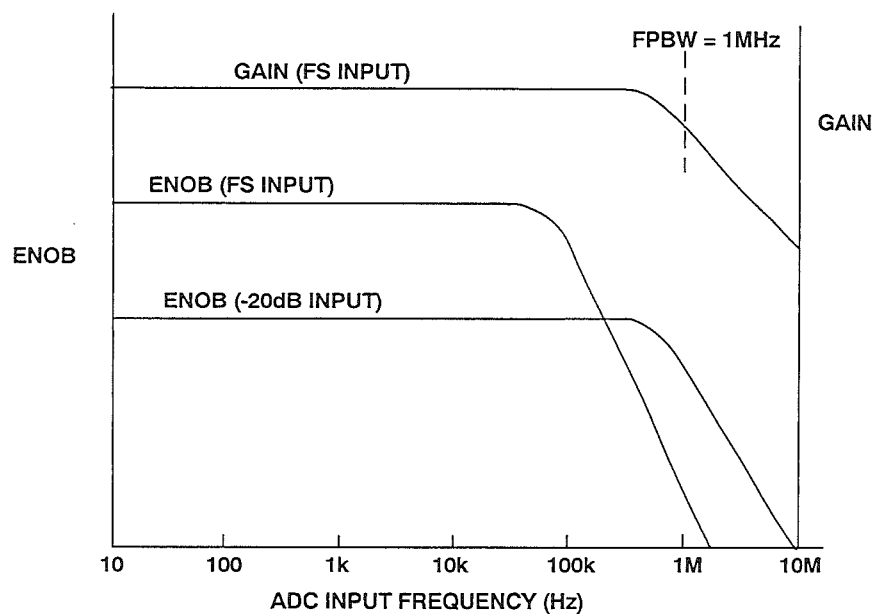


Figure 5.21

The causes of the loss of ENOB at higher input frequencies are varied. The linearity of the ADC transfer function probably degrades as the input frequency increases, thereby causing higher levels of distortion. Another reason that the SNR of an ADC decreases with input frequency may be deduced from Figure 5.22, which shows the effects of phase jitter on the sampling clock of an ADC. The phase jitter causes a voltage error which is a function of slew rate and results in an overall degradation in SNR as shown in Figure 5.23. This is quite serious, especially at higher input/output frequencies. Therefore, extreme care must

be taken to minimize phase noise in the sampling/reconstruction clock of any sampled data system. This care must extend to all aspects of the clock signal: the oscillator itself (for example, a 555 timer is absolutely inadequate, but even a quartz crystal oscillator can give problems if it uses an active device which shares a chip with noisy logic); the transmission path (these clocks are very vulnerable to interference of all sorts), and phase noise introduced in the ADC or DAC. A very common source of phase noise in converter circuitry is aperture jitter in the integral sample-and-hold (SHA) circuitry.

## EFFECTS OF APERTURE AND SAMPLING CLOCK JITTER

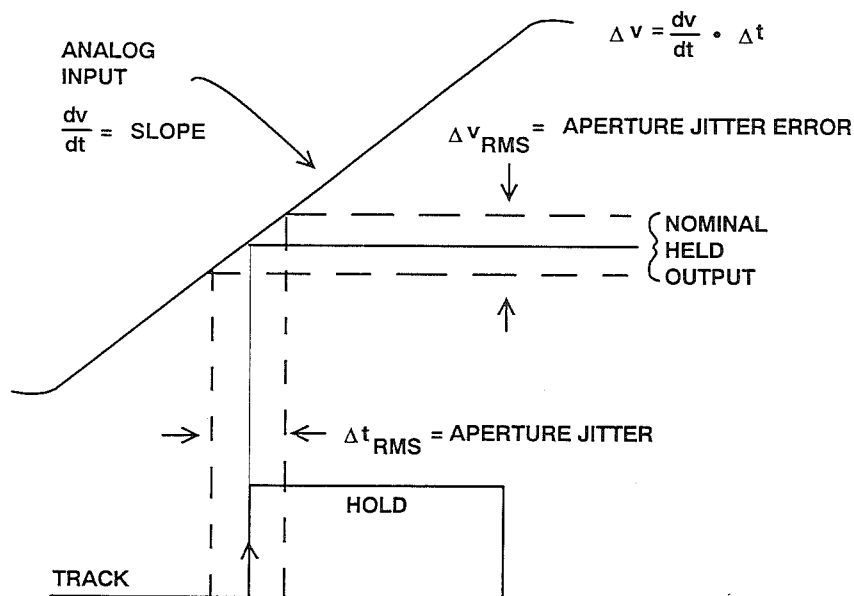


Figure 5.22

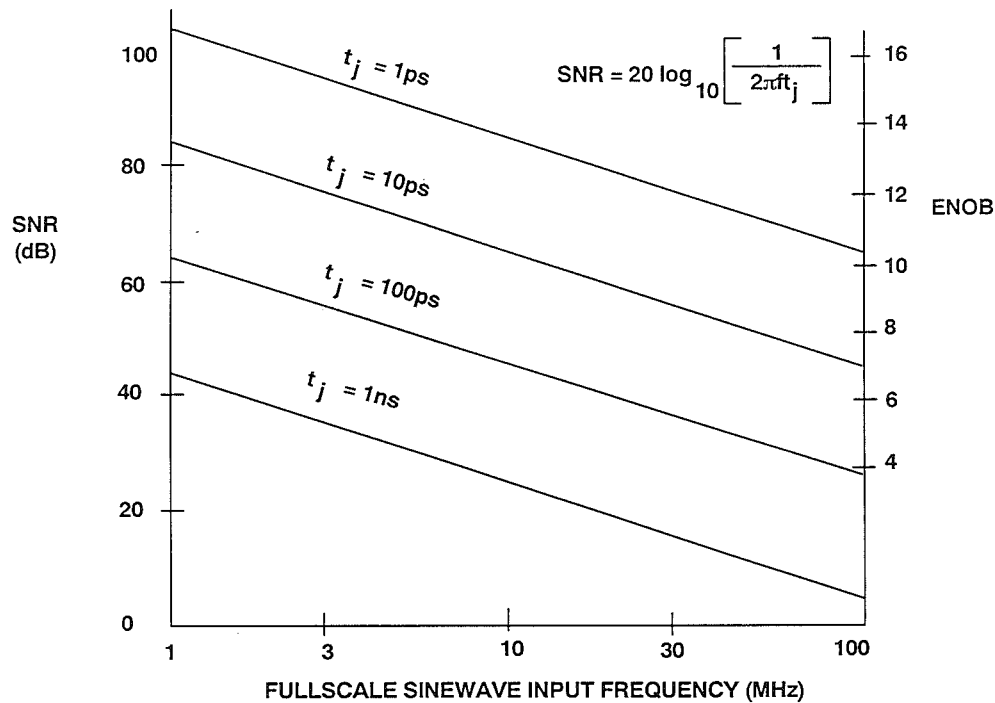
SNR DUE TO SAMPLING CLOCK JITTER ( $t_j$ )

Figure 5.23

A decade or so ago sampling ADCs were built up from a separate SHA and ADC. Interface design was difficult, and a key parameter was aperture jitter in the SHA. Today, most sampled data systems use *sampling* ADCs which contain an integral SHA. The aperture jitter of the SHA may not be specified as such, but this is not a cause of concern if the SNR or ENOB is clearly specified, since a guarantee of a specific SNR is an implicit guarantee of an adequate aperture jitter specification. However, the use of an additional high-performance SHA will sometimes improve the high-frequency ENOB of a sampling ADC, and may be more cost-effective than replacing the ADC with a more expensive one.

It should be noted that there is also a fixed component which makes up the ADC aperture time. This component, usually called *effective aperture delay time*, does not produce an error. It simply results in a time offset between the time the ADC is asked to sample and when the actual sample takes place (see Figure 5.24). The variation or tolerance placed on this parameter from part to part is important in simultaneous sampling applications or other applications such as I and Q demodulation where several ADCs are required to track each other.



## EFFECTIVE APERTURE DELAY TIME

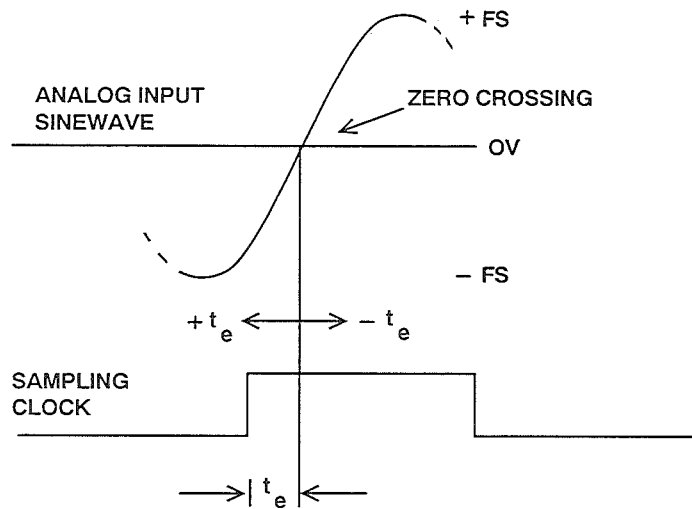


Figure 5.24

The distortion produced by an ADC or DAC cannot be analyzed in terms of second and third-order intercepts, as in the case of an amplifier. This is because there are two components of distortion in a high performance data converter. One component is due to the non-linearity associated with the analog circuits within the converter. This non-linearity has the familiar “bow” or “s”-shaped curve shown in Figure 5.23. (It may be polynomial or logarithmic in form). The distortion associated with this type of non-linearity is sometimes

referred to as *soft* distortion and produces low-order distortion products. This component of distortion behaves in the traditional manner, and is a function of signal level. In a practical data converter, however, the soft distortion is usually much less than the other component of distortion, which is due to the differential nonlinearity of the transfer function. The converter transfer function is more likely to have discrete points of discontinuity across the signal range as shown in Figure 5.25.

## TRANSFER CHARACTERISTICS FOR "SOFT" AND "HARD" DISTORTION IN DATA CONVERTERS

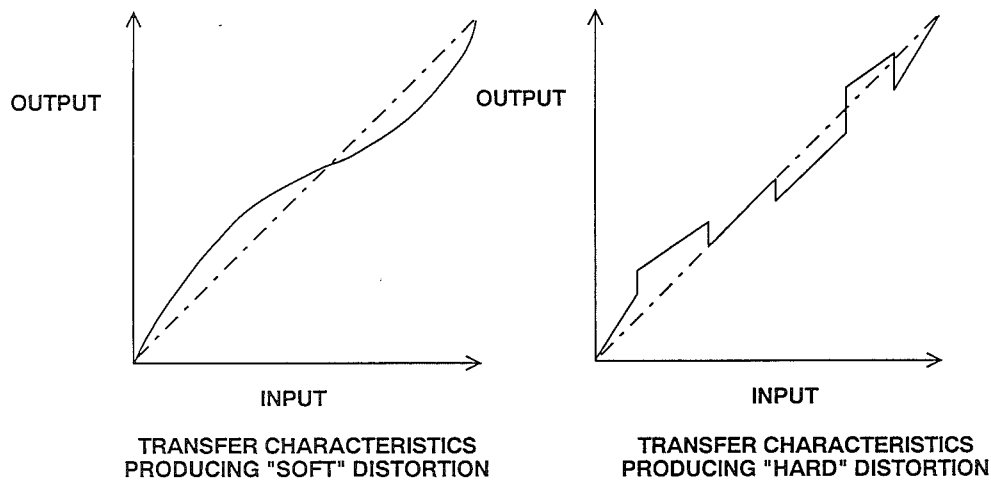


Figure 5.25

The actual location of the points of discontinuity depends on the particular data converter architecture, but nevertheless, such discontinuities occur in practically all converters. Non-linearity of this type produces high-order distortion products which are relatively unpredictable with respect to input signal level, and therefore such specifications as *third order intercept point*

may be less relevant to converters than to amplifiers and mixers. For lower-amplitude signals, this constant level *hard* distortion causes the SFDR of the converter to *decrease* as input amplitude decreases. The soft distortion in a well-designed converter is only significant for high frequency large-amplitude signals where it may rise above the hard distortion floor.

## COMPONENTS AND PROCESSES FOR DATA CONVERTERS

Data converters may be constructed with a wide range of technologies, although the majority are monolithic integrated circuits (ICs) of various types. There are many IC technologies,

and many tradeoffs between them. In general, data converters require logic circuitry, switches, and some precision analog circuitry.

### COMPONENTS FOR DATA CONVERTERS

■ Data Converter Component Requirements:

◆ Good Logic, Good Switches

◆ Good Analog Circuitry:

Amplifiers, Comparators,  
References, Resistors

Figure 5.26

This precision analog circuitry may include stable, accurate voltage or current references, stable precision-matched resistors, and precision amplifiers and comparators. The processes used to manufacture good amplifiers, comparators and references do not, in general, make good logic, so manufacturers of early data converters used multi-chip hybrids to overcome these process limitations. Hybrid technology tends to be expensive, so converter manufacturers have been in the forefront of the development of IC processes capable of both analog and digital performance, so that data converters can be manufactured on a single

chip. In general, they have been successful, but even today, some of the highest performance converters require chips from more than one process.

Since the name *hybrid* is perceived as implying *expensive*, some of these converters have had their process renamed. Where two monolithic chips from different technologies share a package, but do not require a ceramic substrate or any other integrated components, the structure, which is much less expensive than a classical hybrid, is sometimes known as *compound monolithic* rather than *hybrid*.

## HYBRID CONVERTERS

- Early Data Converters used hybrid technology to achieve performance unavailable from any single monolithic technology.
- Even today, some of the best converters cannot use any available monolithic technology and are hybrid.
- *Compound Monolithic* is a term for a simpler (and cheaper) hybrid technology where two monolithic chips from different technologies are mounted together in a single package, but without a ceramic substrate or other components.

5

Figure 5.27

In general, bipolar processes make good, stable, low-noise amplifiers, comparators and references. Bipolar logic, however, though fast, occupies large chip areas and is therefore expensive. Also, processes which make good bipolar logic tend to be noisier than analog processes. CMOS is capable of making high-density, low-power logic very efficiently, but although it can also make good analog switches, it is not very suitable for amplifiers, and almost incapable of making references.

These considerations caused process technologists to combine bipolar and CMOS processes to achieve both low-power, high density logic and high-accuracy, low-noise analog circuitry on a single chip. The resulting processes are more complex, and therefore more expensive, than simple bipolar and CMOS processes, but do have better mixed performance. They include BIMOS processes which are basically bipolar processes to which CMOS structures have been added, and linear compatible CMOS (LC<sup>2</sup>MOS or

LCCMOS) which is basically CMOS with added bipolar capability. However, the compromises necessary to combine features mean that neither BIMOS nor LCCMOS offers quite as good performance as its parent process does in its specialty. Thus, BIMOS and LCCMOS have not replaced bipolar or CMOS technology, but designers now have four processes from which to choose when designing a data converter.

Of course, to suggest that there is only *one* of each of these process is a gross simplification, and omits all considerations of such process developments as complimentary bipolar (CB) and dielectrically isolated (DI) processes. Since this section is concerned with converter structures, however, it is not really appropriate to discuss IC processes in detail. There is, however, one process technology which does deserve special mention, since it is crucial to the manufacture of any data converter requiring stable precision resistors. This is thin-film resistor technology.

## MONOLITHIC CONVERTER PROCESSES

- *Bipolar* processes have good analog performance but less good logic and switches.
- *CMOS* processes make excellent logic and switches but relatively poor amplifiers and references.
- Processes combining the two (*BiMOS*, *LCCMOS*, etc.) tend to be more complex and expensive and have slightly less performance than the sum of the two but are very convenient.
- Good designers choose the best process for the circuit to be designed.

Figure 5.28

Analog Devices has spent many man-years of effort developing the ability to deposit stable thin-film resistors on integrated circuit chips, and yet more man-years in learning to laser trim them. All the processes mentioned above can incorporate such resistors. They have stability of  $<20$  ppm/ $^{\circ}\text{C}$ , and matching to within 0.005%. Actually, the resistors can be made to match to

within 0.01% or better without laser trimming, but to achieve this they must be very large. In practice, if resistors must match to better than 0.1 or 0.05%, it is more economical to laser trim them than to design them to meet the specification without trimming. Most of the resistors in the next sections are these laser-trimmed SiCr thin-film resistors.

## THIN FILM RESISTORS

- One of the key technologies for making many types of monolithic data converters is the ability to deposit accurate, stable SiCr resistors on monolithic chips.
- Some converters use these resistors as fabricated, others require the additional accuracy and economy of laser trimming.
- Parameters include:
  - ◆ Matching to 0.005%
  - ◆ Temperature Coefficient < 20ppm/°C
  - ◆ Differential TC < 0.2ppm/°C
  - ◆ Long Term Stability  $\leq 1\text{ppm}/1000\text{ hours}$  (drunkard's walk)

5

Figure 5.29

## DAC STRUCTURES

It is reasonable to consider a changeover switch, switching an output between a reference and ground, or between equal positive and negative reference voltages, as a 1-bit DAC (see Figure 5.30). Such a simple device is a component of many more complex DAC structures and is used, with oversampling, as the basic analog component in the sigma-delta DAC we shall discuss later. Nevertheless, it is a little too simple to require discussion, and it is more rewarding to consider more complex structures.

The DACs most commonly used as examples of simple DAC structures are

binary weighted DACs or ladder networks, but these, though simple in structure, require quite complex analysis. The simplest structure of all, after the changeover switch mentioned above, is the Kelvin divider shown in Figure 5.31. An N-bit version of this DAC simply consists of  $2^N$  equal resistors in series. The output is taken from the appropriate tap by closing one of the  $2^N$  switches (there is some slight digital complexity involved in decoding to 1 of  $2^N$  switches from N-bit data, but digital circuitry is comparatively cheap).

## A CHANGEOVER SWITCH IS A 1-BIT DAC

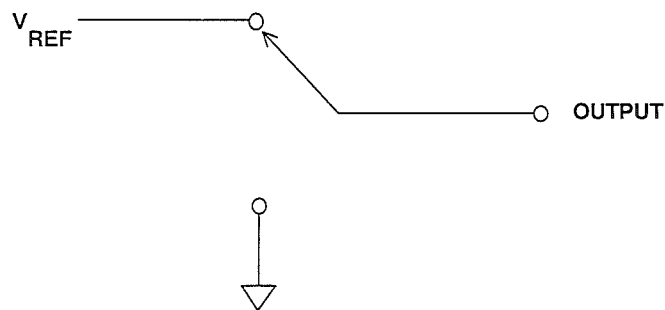


Figure 5.30

## SIMPLEST MULTI-BIT DAC: THE KELVIN DIVIDER

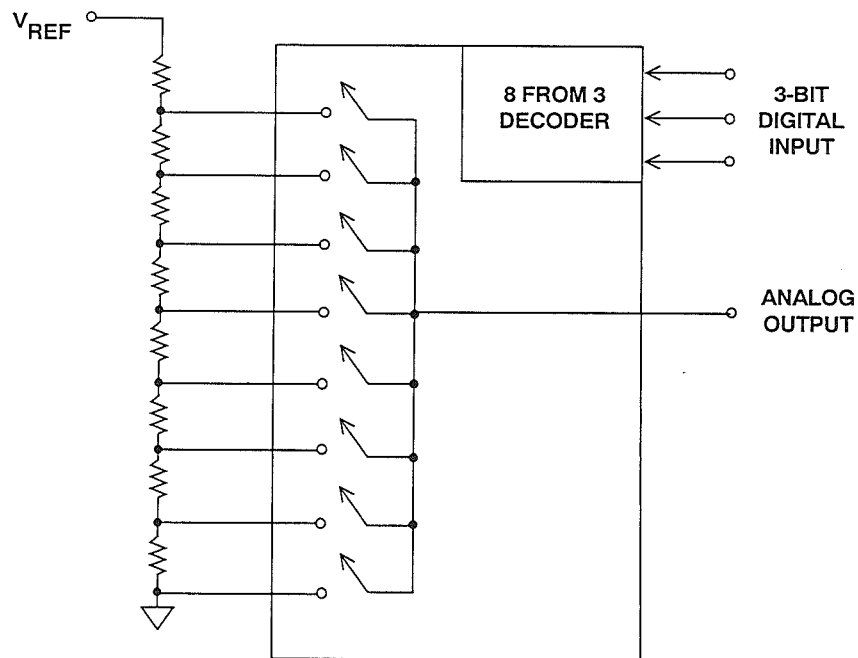


Figure 5.31

This architecture is simple, has a voltage output (but a code-varying  $Z_{OUT}$ ), and is inherently monotonic (even if a resistor is zero,  $OUTPUT_N$  cannot exceed  $OUTPUT_{N+1}$ ). It is linear if all the resistors are equal, but may be made deliberately non-linear if a non-linear DAC is required. Since only two switches operate during a transition, it is a low-glitch architecture. Its major drawback is the large number of resistors required for high resolution, and as a result it is not commonly used (the

only commercially available DAC of this type is a fast, low-glitch 8-bit device from Philips) — but, as we shall see later, it is used as a component in more complex DAC structures.

There is an analogous current output DAC which consists, again, of  $2^N$  resistors (or current sources), but in this case they are all connected in parallel between the reference voltage input and the virtual ground output (see Figure 5.32).

### THE SIMPLEST CURRENT OUTPUT DAC

5

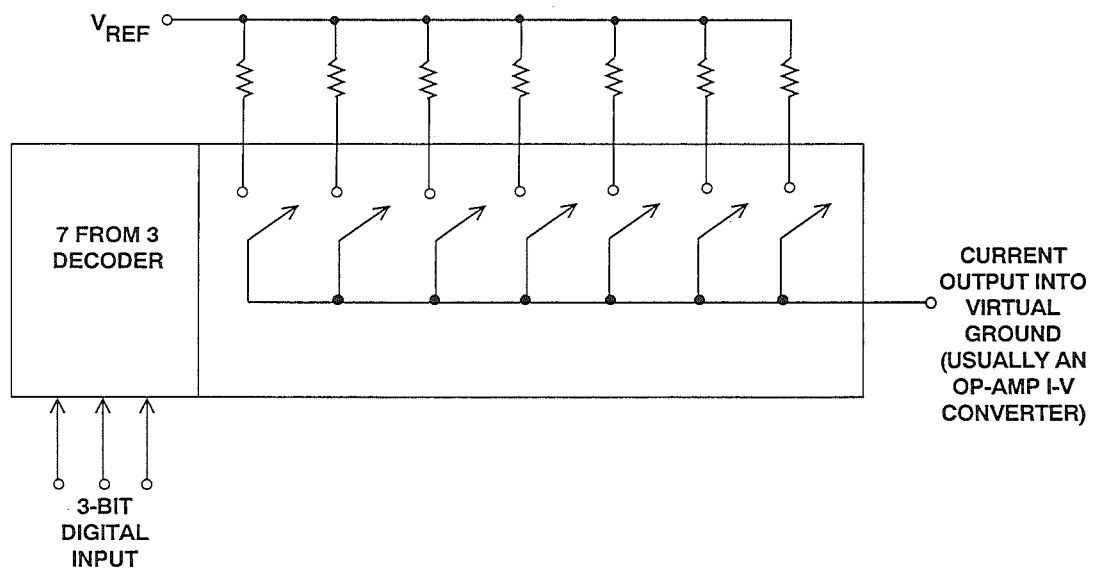


Figure 5.32

In this DAC, once a resistor is switched into circuit by increasing digital code, any further increases do not switch it out again. The structure is thus inherently monotonic, irrespective of inaccuracies in the resistors, and like the previous case, may be made intentionally non-linear where a specific non-

linearity is required. Again, as in the previous case, the architecture is rarely, if ever, used to fabricate a complete DAC because of the large numbers of resistors and switches required. However, it is often used as a component in a more complex DAC structure.



Unlike the Kelvin divider, this type of DAC does not have a unique name, although both types are referred to as “fully decoded DACs” or “thermometer DACs”.

Fully-decoded DACs are often used as components of more complex DACs. The most common are “segmented DACs” where part of the output of a fully decoded DAC is further subdivided. The structure is used because the fully decoded DAC is inherently monotonic, so if the subdivision is also monotonic, the whole resulting DAC is also monotonic.

A voltage segmented DAC (see Figure 5.33) works by further sub-dividing the voltage across one resistor of a Kelvin divider. The sub-division may be done with a further Kelvin divider (in which case the whole structure is known as a

“Kelvin-Varley divider”, or with some other DAC structure. Commercial 16-bit DACs exist with both arrangements: the AD569 uses two cascaded 8-bit Kelvin dividers in a Kelvin-Varley structure, a total of 512 resistors, to give a 16-bit monotonic but only 13-bit linear DAC (this linearity problem is one of resistor size - with 512 resistors on a chip, they are too small to laser trim, let alone to be intrinsically matched to 16-bits), and the AD7846 uses a 12-bit ladder network in the voltage mode connected across one resistor of a 4-bit Kelvin divider.

In a true current-segmented DAC using fully-decoded MSBs (see Figure 5.34), each current source has a three-way switch and is switched off, or to a further current steering DAC, or directly to the output. This architecture, too, is inherently monotonic.

## SEGMENTED VOLTAGE DACs

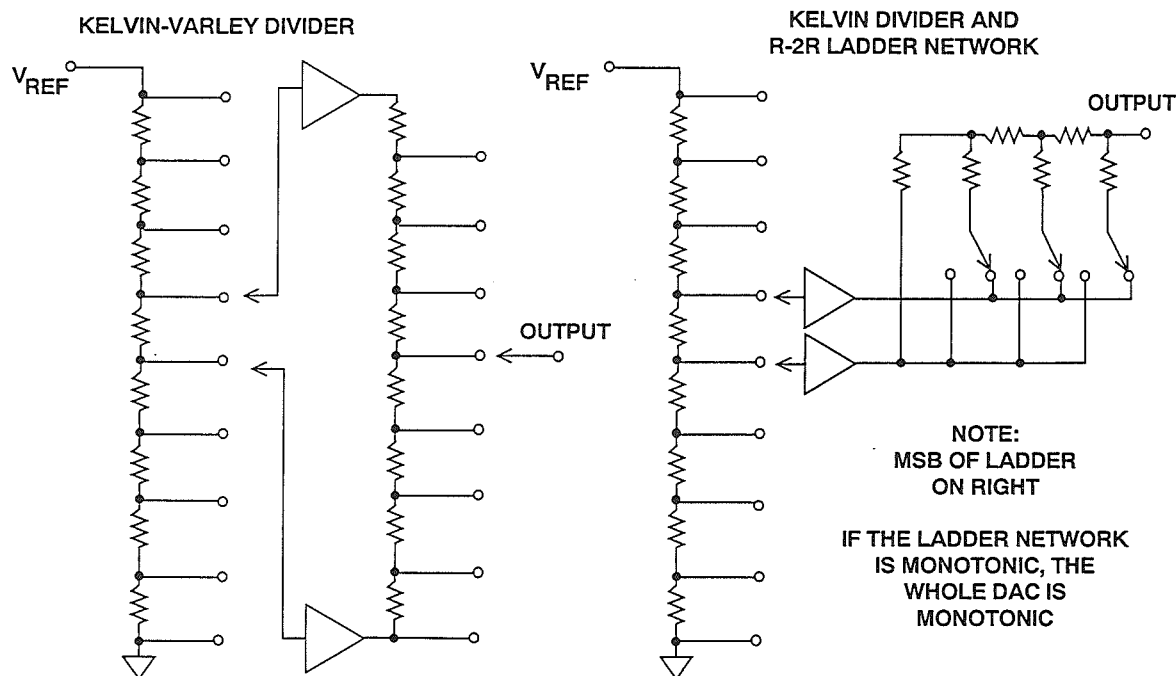


Figure 5.33

## SEGMENTED 4-BIT CURRENT OUTPUT DAC

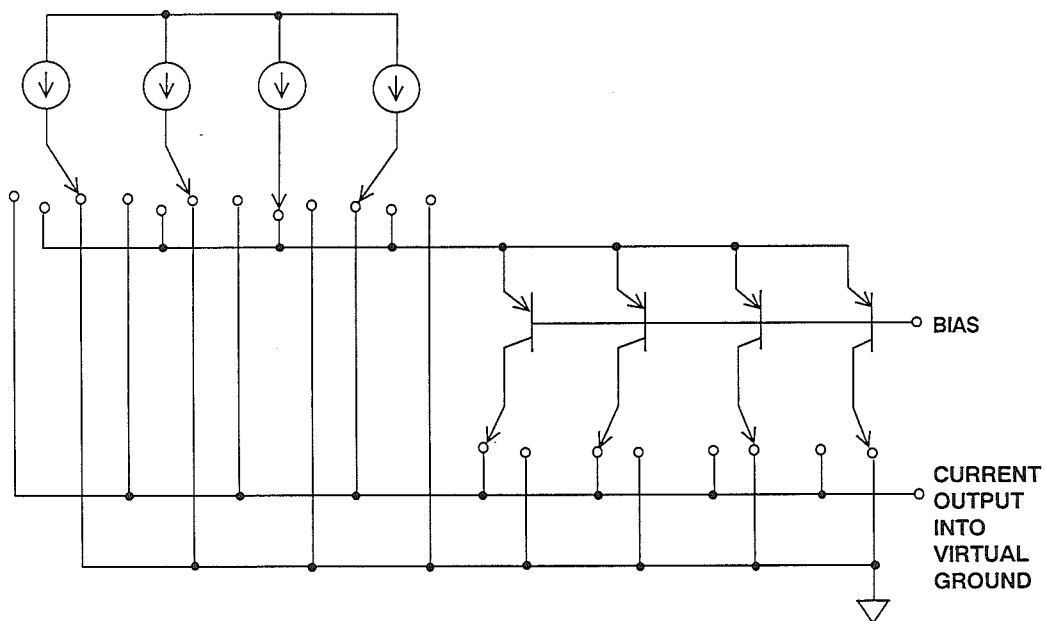
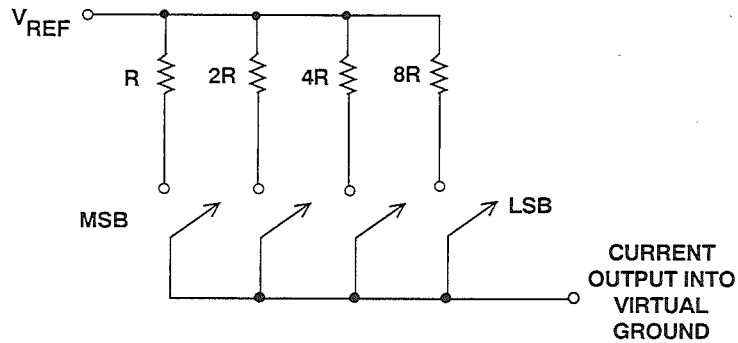


Figure 5.34

The simplest textbook example of a DAC, the binary-weighted DAC shown in Figure 5.35 is not inherently monotonic and is very hard to manufacture successfully. An  $N$ -bit DAC of this type consists of  $N$  resistors in the ratio  $1:2:4:8:\dots:2^{N-1}$ . The LSB switches the  $2^{N-1}$  resistor, the MSB the 1 resistor,

etc. The theory is simple, but the practical problems of manufacturing an IC of an economical size with resistor ratios of even 128:1 for an 8-bit DAC are enormous, especially as the resistors must have matched temperature coefficients.

## BINARY WEIGHTED CURRENT OUTPUT DAC



■ DIFFICULT TO FABRICATE IN IC FORM DUE TO LARGE RESISTOR RATIO

Figure 5.35

## DAC USING CASCADED BINARY QUADS

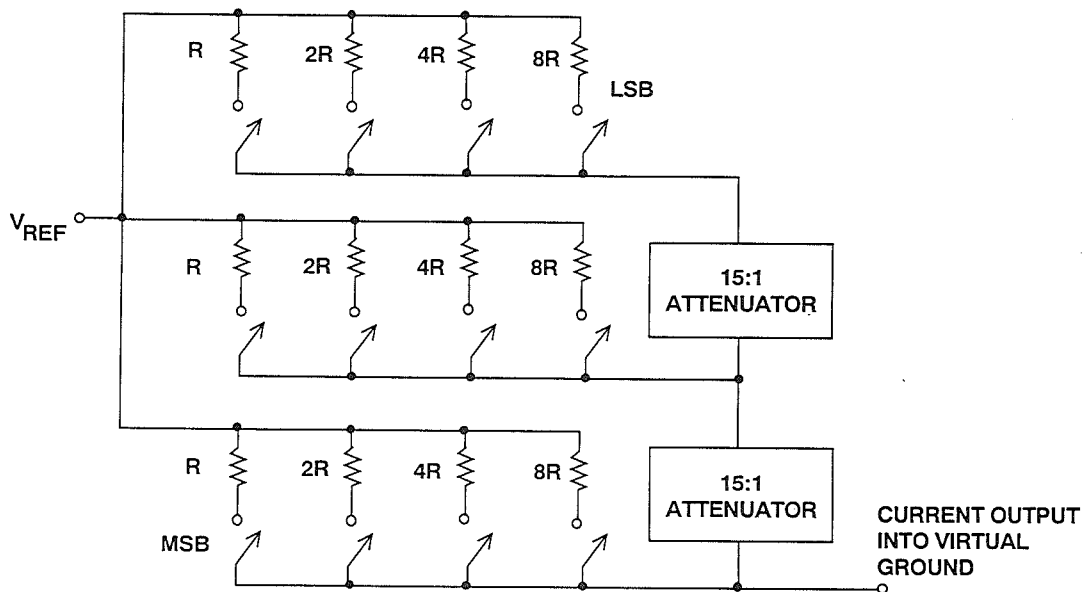


Figure 5.36

If the MSB resistor is even a little high in value, the MSB current will be less than the sum of all the other bit currents, and the DAC will not be monotonic (the differential non-linearity of most types of DAC is worst at major bit transitions). This architecture is never used in integrated circuit DACs, although, again, it has been used as a component of a more complex structure.

Figure 5.36 shows a 12-bit DAC made from three 4-bit binary weighted DACs with attenuators. In the early days of IC DACs, this architecture was some-

times used, but it was less than ideal, requiring 15:1 resistor ratios. The ideal resistor ratio for precision is as close as possible to 1:1, and the R:2R ladder network is not too far from this.

The R:2R ladder is shown in Figure 5.37 and uses resistors of only two different values: their ratio is 2:1. An N-bit DAC requires  $2^N - 1$  resistors. There are two ways in which the R:2R ladder network may be used as a DAC, known respectively as the voltage mode, and the current mode. Each has its advantages and disadvantages.

#### 4-BIT R-2R LADDER NETWORK

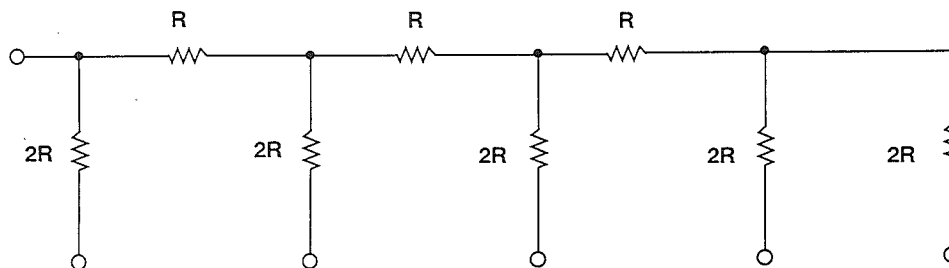


Figure 5.37

In the voltage mode, the “rungs” or arms of the ladder are switched between  $V_{\text{ref}}$  and ground, and the output is taken from the end of the ladder, as shown in Figure 5.38. The output may be taken as a voltage, but the output impedance is independent of code, so it may equally well be taken as a current into a virtual ground.

The voltage output is an advantage of this mode, as is the constant output impedance, which eases the stabilization of any amplifier on the output node. Additionally, the switches switch

the arms of the ladder between a low impedance  $V_{\text{ref}}$  connection and ground, so capacitive glitch currents tend not to flow in the load. On the other hand, the switches must operate over a wide voltage range ( $V_{\text{ref}}$  to ground), which is difficult from a design and manufacturing viewpoint, and the reference input impedance varies widely with code, so that the reference input must be driven from a very low impedance, and the gain of the DAC cannot be adjusted with a preset resistor in series with the  $V_{\text{ref}}$  terminal.

### VOLTAGE-MODE LADDER NETWORK DAC

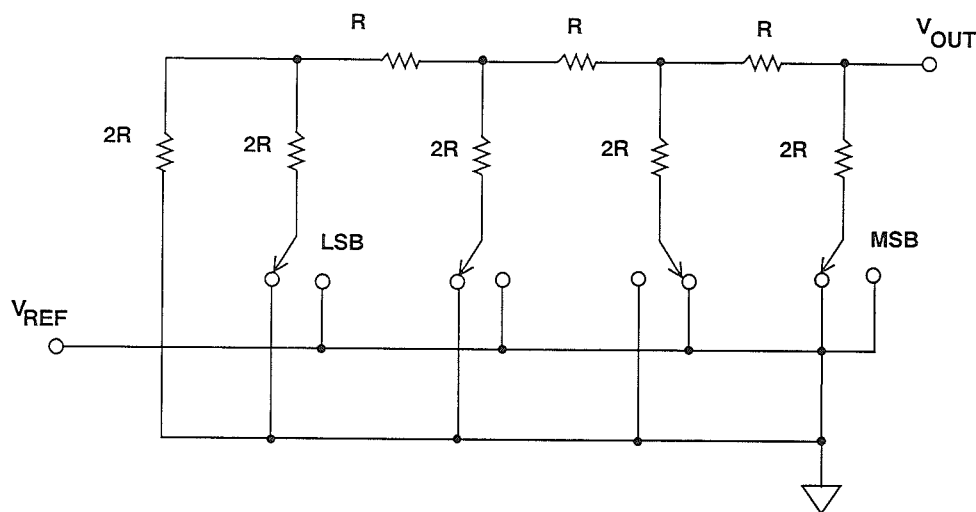


Figure 5.38

The gain of a DAC in the current mode configuration shown in Figure 5.39 may be adjusted with a series resistor since, in the current mode, the end of the ladder, with its code-independent impedance, is used as the  $V_{\text{ref}}$  terminal, and the ends of the arms are switched between ground and an output line

(which must be held at ground potential). The normal connection of a current mode ladder network output is to an op-amp configured as an I-V converter, but stabilization of this op-amp may be complicated by the DAC output impedance variation with code.

## CURRENT-MODE LADDER NETWORK DAC

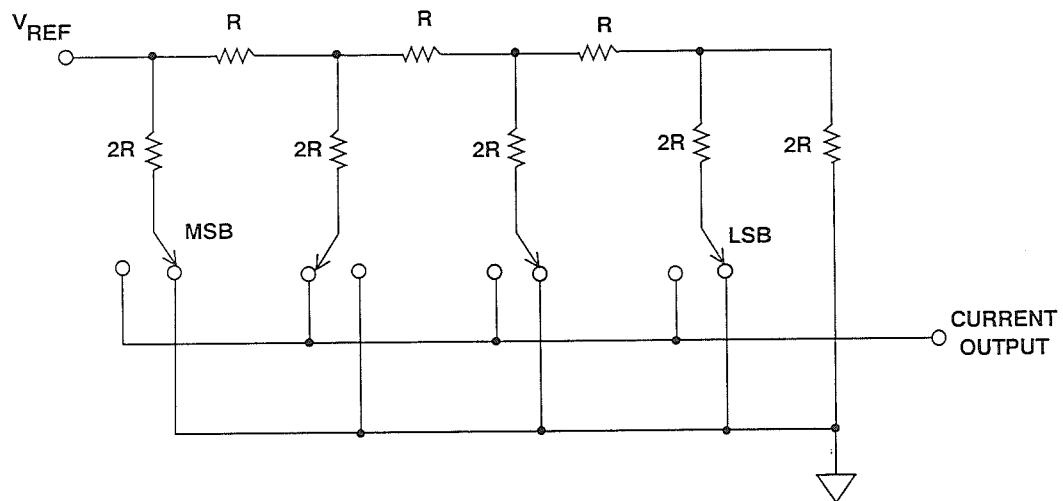


Figure 5.39

Current mode operation has higher glitch, though, since the switches connect directly to the output line, but as the switches of a current-mode ladder network are always at ground potential, their design is less demanding and, in particular, their voltage rating does not affect the reference voltage rating. If switches capable of carrying current in either direction (such as MOS devices) are used, the reference voltage may have either polarity, or may even be AC. Such a structure is one of the most common types of multiplying DAC (MDAC).

In all DACs, the output is the product of the reference voltage and the digital

code, so in that sense, all DACs are multiplying DACs, but many DACs operate well only over a limited range of  $V_{\text{ref}}$ . True MDACs, however, are designed to operate over a wide range of  $V_{\text{ref}}$ . A strict definition of a multiplying DAC demands that its reference voltage range includes 0V, and many, especially current mode ladder networks with CMOS switches, permit positive, negative, and AC  $V_{\text{ref}}$ . DACs which do not work down to 0V  $V_{\text{ref}}$  are still useful, however, and types where  $V_{\text{ref}}$  can vary by 10:1 or so are often called MDACs, although a more accurate description might be “semi-multiplying” DACs.

## MULTIPLYING DACs (MDACs)

- In all DACs the output is the product of the reference voltage and the digital code.
- Most DACs work over a limited range of reference voltages.
- DACs which work well with reference voltages which include zero volts are known as *Multiplying DACs*.
- Many MDACs work with bipolar and AC reference voltages.
- DACs which work with a large range of reference voltages, but not down to zero, are not true MDACs but are sometimes called MDACs. It is better to use the term *semi-multiplying DACs*.

Figure 5.40

The ladder network is certainly the most common DAC architecture. Where higher resolutions are required, however, trimming a ladder network can be demanding. A common way of minimiz-

ing the problem is to build a current mode DAC with 2 or 3 fully decoded MSBs, and a ladder network for the remainder of the structure as shown in Figure 5.41.

## A SEGMENTED LADDER DAC

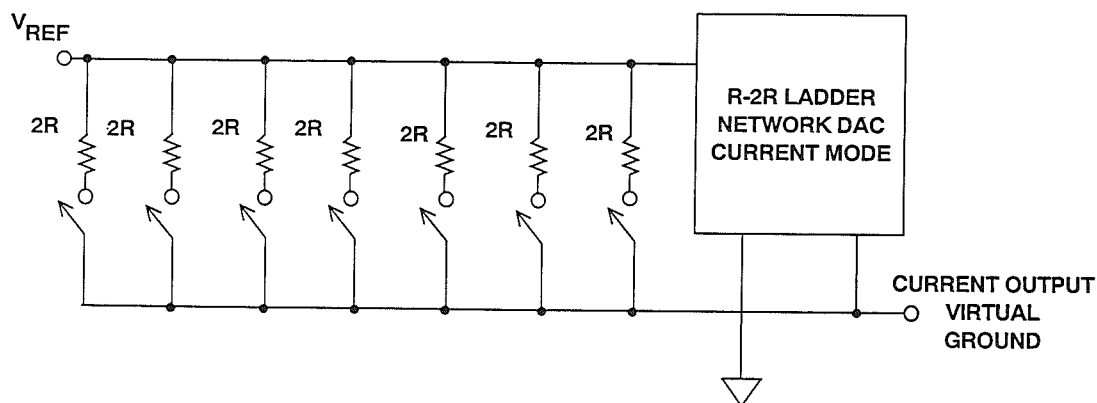


Figure 5.41

This arrangement is sometimes referred to as a *segmented* DAC, but the description is not strictly accurate, as even if the ladder network is monotonic, it is not inherently certain that the overall DAC will be, although it is comparatively easy to laser trim such an arrangement to monotonicity.

Digital audio requires DACs with resolutions of over 16-bits, good linearity, and low cost. One way to make them is to use a ladder with several decoded MSBs as described above, but

this is likely to have comparatively large DNL at the MSB transition, which is just where low DNL is needed for low-level audio distortion. This problem can be avoided by using a digital adder to put a digital offset in the DAC code, so that the MSB transition of the input code is well offset from the mid-point of the DAC transfer characteristic, and then using an analog offset on the DAC output to restore the DC level at the crossover (see Figure 5.42).

## 20-BIT AUDIO DAC WITH OFFSET MSB TRANSITION

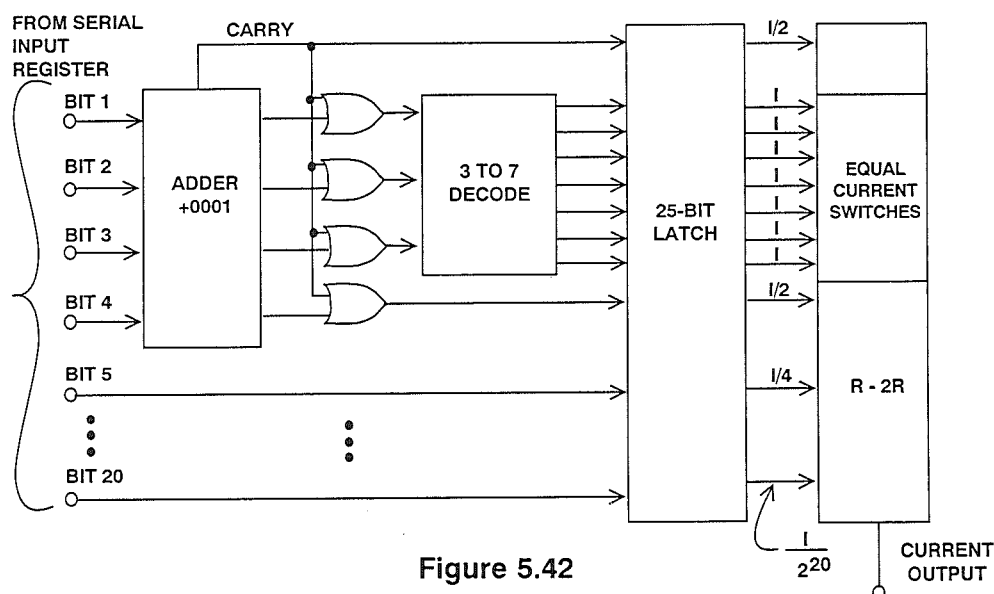


Figure 5.42

Another way of obtaining high resolution is to use oversampling techniques and a 1-bit DAC. The technique, known as sigma-delta ( $\Sigma$ - $\Delta$ ), is computation intensive, so has only recently become practical for the manufacture of high resolution DACs, but since it uses a 1-bit DAC, it is intrinsically linear and monotonic.

A  $\Sigma$ - $\Delta$  DAC, unlike the  $\Sigma$ - $\Delta$  ADC we shall discuss later, is entirely digital (see Figure 5.43). It consists of an "interpolation filter" (a digital circuit

which accepts data at a low rate, inserts zeros at a high rate, and then applies a digital filter algorithm and outputs data at high rate), a  $\Sigma$ - $\Delta$  modulator (which effectively acts as a low pass filter to the signal but as a high pass filter to the quantization noise, and converts the resulting data to a high speed bit stream), and a 1-bit DAC (which, as we mentioned earlier, is simply a changeover switch) connected to equal positive and negative reference voltages. The output is filtered in an external analog LPF.



## SIGMA-DELTA ( $\Sigma\Delta$ ) DAC

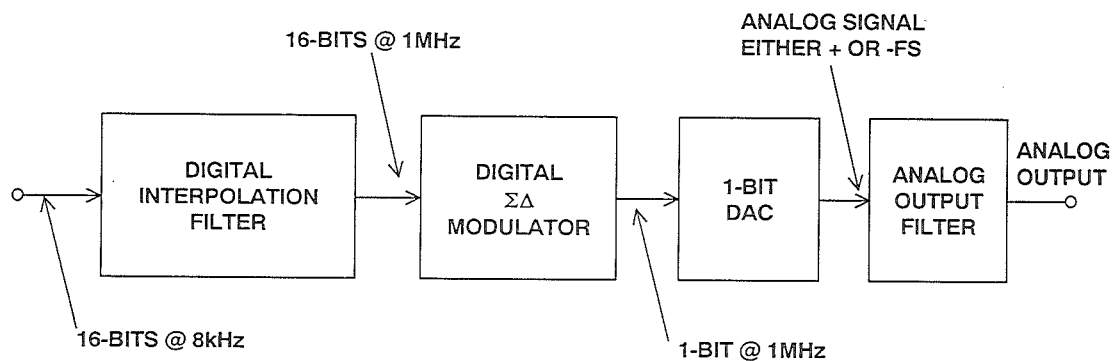


Figure 5.43

In theory, a  $\Sigma\Delta$  DAC is perfectly linear and has very low noise. In practice, they are very good, but, because of the difficulty of having an adequately fast clock with low enough phase noise and still separating digital noise from the analog signal, are still (as of mid 1994)

marginally less good for the highest quality digital audio than the best traditional DACs. Nevertheless,  $\Sigma\Delta$  DACs are the optimum choice for a large number of low price, medium to high quality reconstruction DAC applications.

## DAC LOGIC

The earliest monolithic DACs contained little, if any, logic circuitry, and parallel data had to be maintained on the digital input to maintain the digital output. Today almost all DACs are latched, and data need only be written once, not maintained.

There are innumerable variations of DAC input structure which will not be discussed here, but the majority today are “double-buffered”. A double-buffered DAC has two sets of latches. Data is initially latched in the first rank and subsequently transferred to the second as shown in Figure 5.44. There are two reasons why this arrangement is useful.

The first is that it allows data to enter the DAC in many different ways. A DAC without a latch, or with a single latch, must be loaded with all bits at once, in parallel, since otherwise its output during loading may be totally different from what it was or what it is to become. A double-buffered DAC, on the other hand, may be loaded with parallel data, or with serial data, or with 4-bit or 8-bit words, or whatever, and the output will be unaffected until the new data is completely loaded and the DAC receives its update instruction.

5

### DOUBLE-BUFFERED DAC PERMITS COMPLEX INPUT STRUCTURES AND SIMULTANEOUS UPDATE

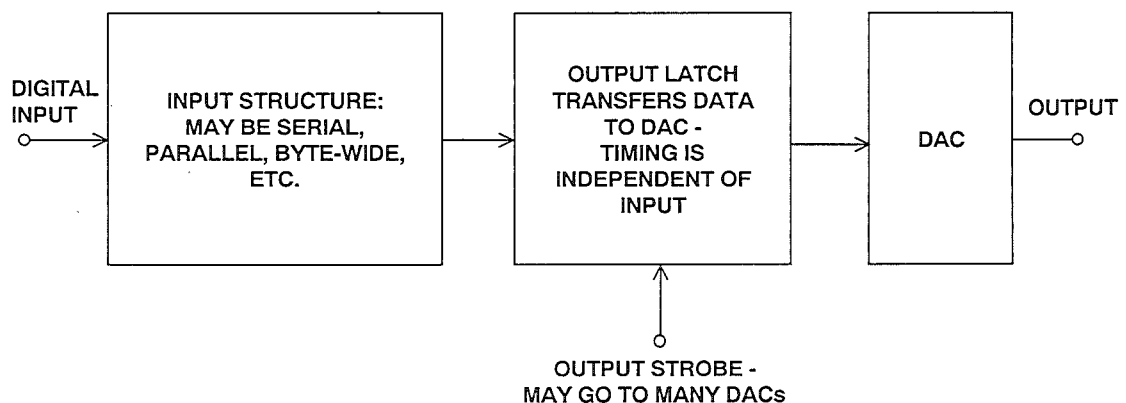


Figure 5.44

The other convenience of the double-buffered structure is that many DACs may be updated simultaneously: data is loaded into the first rank of each DAC in turn, and when all is ready, the output buffers of all DACs are updated at once. There are many DAC applications where the output of several DACs must change simultaneously, and the double-buffered structure allows this to be done very easily.

Most early monolithic high resolution DACs had parallel or byte-wide data ports and tended to be connected to parallel data buses and address decoders and addressed by microprocessors as if they were very small write-only memories (some DACs are not write-only, but can have their contents

read as well - this is convenient for some applications but is not very common). A DAC connected to a data bus is vulnerable to capacitive coupling of logic noise from the bus to the analog output, and many DACs today have serial data structures. These are less vulnerable to such noise (since fewer noisy pins are involved), use fewer pins and therefore take less space, and are frequently more convenient for use with modern micro-processors, many of which have serial data ports. Some, but not all, of such serial DACs have data outputs as well as data inputs so that several DACs may be connected in series and data clocked to them all from a single serial port. The arrangement is referred to as "daisy-chaining".

## **SERIAL DACS**

- If data is loaded serially into a DAC it requires fewer data pins.
- This saves space and also reduces capacitive noise coupling from data lines to the analog output.
- If the shift register of serial DAC has an output pin, a number of DACs may be connected in series (*daisy chained*) to a single serial data port.

**Figure 5.45**

Another development in DACs is the ability to make several on a single chip, which is useful to reduce PCB sizes and assembly costs. Today (mid-1994) it is possible to buy sixteen 8-bit, eight

12-bit, four 14-bit, or two 16-bit or 18-bit DACs in a single package. In the future, even higher densities are probable.

## MULTIPLE DACS SAVE SPACE

- Several DACs on one chip are cheaper, smaller, and simpler to interface than several packages.
- Present limits (mid-1994) are:

16 × 8-bit

8 × 12-bit

2 × 16-bit or 18-bit

(Stereo Audio)

5

Figure 5.46

## ADC STRUCTURES

In this section, we shall consider the structures and conversion algorithms of eight types of ADC, but, as in the DAC section, we shall not be concerned with many details of their digital interfaces, save to point out that if logic is cheap the results of an A-D conversion may easily be reformatted in any convenient way; parallel, serial or byte-wide. This

means that it is generally possible to find a general purpose ADC with integral logic to provide an output data format well-suited to any particular application. Special purpose ADCs (high speed, high resolution, etc.) may only be available with a more limited range of options.

## TYPES OF ANALOG-TO-DIGITAL CONVERTERS

- *Comparator*: A 1-bit ADC
- *Flash* : Fast, low-resolution, high power
- *Subranging*: Fast, high-resolution, complex
- *Integrating*: Slow, accurate, low power
- *Voltage-to-Frequency (VFC)*: High-resolution, low power, ideal for telemetry
- *Tracking*: Fast and slow, high-resolution
- *Successive Approximation*: Versatile, general purpose
- *Sigma-Delta*: Complex, low power, high-resolution

Figure 5.47

There are one or two practical points which are worth remembering about the logic of ADCs. On power-up, many ADCs do not have logic reset circuitry and may enter an anomalous logical state. One or two conversions may be necessary to restore their logic to proper operation so: (a) the first and second conversions after power-up should never be trusted, and (b) control outputs (EOC, DRDY, etc.) may behave in unexpected ways at this time (and not necessarily in the same way at each power-up), and (c) care should be taken to ensure that such anomalous behavior cannot cause system latch-up. For example, EOC (End Of Conversion) should not be used to initiate conversion if there is any possibility that EOC will not occur until the first conversion has taken place, as otherwise initiation will never occur.

Another detail which can cause trouble is the difference between EOC and DRDY (Data Ready). EOC indicates

that conversion has finished, DRDY that data is available at the output. In some ADCs, data is not valid until several tens of nanoseconds *after* the EOC has become valid, and if EOC is used as a data strobe, the results will be unreliable.

As a final example, some ADCs use CS (Chip Select) edges to reset internal logic, and it may not be possible to perform another conversion without asserting or reasserting CS (or it may not be possible to read the same data twice, or both).

For more detail, it is important to read the whole data sheet before using an ADC since there are innumerable small logic variations from type to type. Unfortunately, many data sheets are not as clear as one might wish, so it is also important to understand the general principles of ADCs in order to interpret data sheets correctly. That is one of the purposes of this section.

## BEWARE OF ADC LOGIC PITFALLS

- After power-up one or two conversions may be required before it runs right. The EOC (end of conversion) cannot always be trusted at this time.
- An ADC may not behave the same way every time it starts.
- EOC says conversion is finished.  
DRDY (data ready)says that data is valid.  
There may be tens of nanoseconds difference between the two.
- CS (Chip Select) may not just enable the data. It may reset things for the next conversion.  
In some converters, you *must* read the data!  
In some converters, you can't read the data twice!  
In some converters, you can't strap CS and forget it!
- READ THE DATA SHEET!!!

5

Figure 5.48

## Comparators

As a changeover switch is a 1-bit DAC, so a comparator is a 1-bit ADC. If the input is above a threshold, the output has one logic value, below it has an-

other. Moreover, there is no ADC architecture which does not use at least one comparator of some sort.

## A COMPARATOR IS A 1-BIT ADC, AND ALL TYPES OF ADCs ARE BUILT WITH COMPARATORS

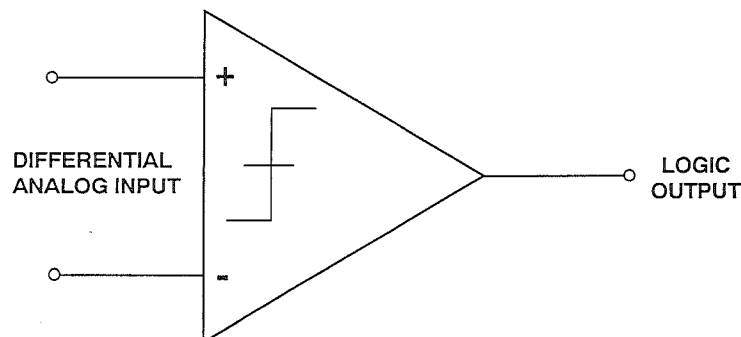


Figure 5.49

The most common comparator has some resemblance to an operational amplifier in that it uses a “long-tailed pair” of transistors or FETs as its input stage, but unlike an op amp, it does not use external feedback, and its output is a logic level indicating which of the two inputs is at the higher potential. Some comparators have a millivolt or two of hysteresis to encourage “snap” action and to prevent local feedback from causing instability in the transition region.

## Flash or Parallel ADCs

Flash ADCs (sometimes called *parallel* ADCs) are the fastest type of ADC and use large numbers of comparators. An  $N$ -bit flash ADC consists of  $2^N$  resistors and  $2^N - 1$  comparators arranged as in Figure 5.50. It is clear that each comparator has a reference voltage which is 1 LSB higher than that of the one below it in the chain. For a given input voltage, all the comparators below a certain point will have their input larger than their reference and a “1” logic output, and all the comparators above that point will have a reference larger than input and a “0” logic output. The  $2^N - 1$  comparator outputs therefore behave in a way analogous to a mercury thermometer, and the output code at this point is sometimes called a *thermometer* code. Since  $2^N - 1$  data outputs are not really practical, they are processed by a priority encoder to an  $N$ -bit output.

The signal is applied to all the comparators at once, so the thermometer output is delayed by only one comparator delay from the input, and the encoder  $N$ -bit output by only a few gate delays on top of that, so the process is very fast. However, the system uses large numbers of resistors and comparators for

It is not usual to use a discrete comparator as an element in a more complex ADC so this paper will not discuss the structure or use of comparators in detail (but more information may be found in Reference 3 and Section 8 of this book). Where comparators are incorporated into IC ADCs, their design must consider resolution, speed, overload recovery, power dissipation, offset voltage, bias current, and the chip area occupied by the architecture which is chosen.

quite low resolutions, and if it is to be fast, each comparator must run at relatively high power levels. Hence, the problems of flash ADCs include limited resolution, high power dissipation (especially at sampling rates greater than 50MSPS), and relatively large (and therefore expensive) chip sizes. In addition, the resistance of the reference resistor chain must be kept low to supply adequate bias current to the fast comparators, so the voltage reference has to source quite large currents ( $>10$  mA).

In practice, flash converters are available up to 10-bits (12 bit flash converters have been made, but are not commercially viable), but more commonly they have 8-bits of resolution. Their maximum sampling rate can be as high as 500 MSPS, and input full-power bandwidths in excess of 300 MHz are not uncommon.

But as we mentioned earlier, full-power bandwidths are not necessarily full-resolution bandwidths. Ideally, the comparators in a flash converter are well matched both for DC and AC characteristics. Because the strobe is

applied to all the comparators simultaneously, the flash converter is inherently a sampling converter. In practice, there are delay variations between the comparators and other AC mismatches which cause a degradation in ENOB at high input frequencies.

The input to a flash ADC is applied in parallel to a large number of comparators. Each has a voltage variable junction capacitance, and we must also

consider the inductance of the long conductor tracks on the chip from the pad to the comparators. The combination of inductance and non-linear signal-dependent capacitance results in all flash ADCs having reduced ENOB at high input frequencies as shown in Figure 5.51, the exact amount of degradation will vary from type to type, but the basic problem is inherent in the architecture.

## FLASH OR PARALLEL ADC

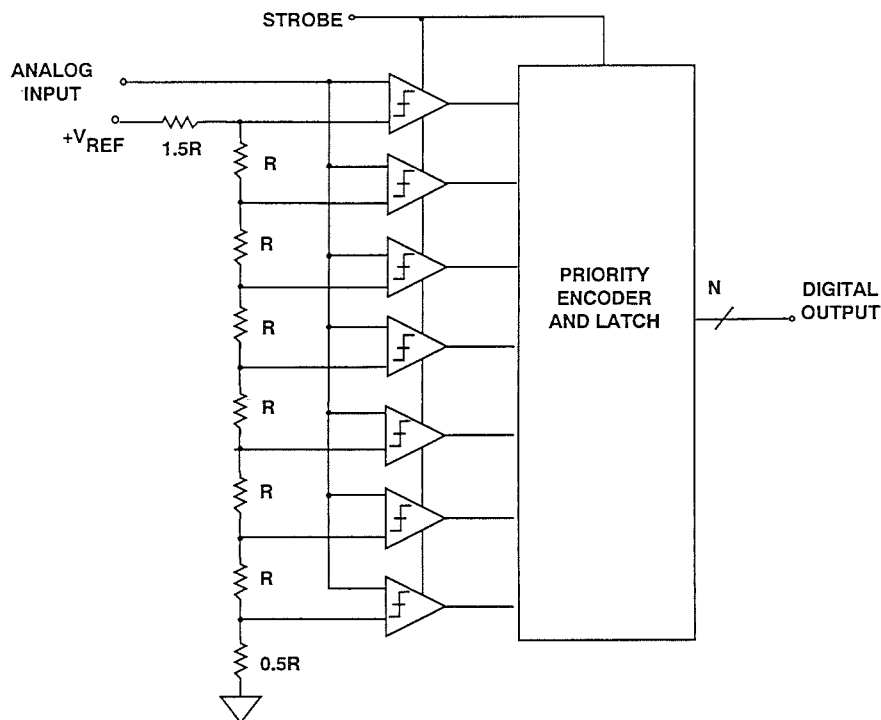


Figure 5.50



## INPUT CIRCUIT MODEL FOR FLASH ADC AND ITS EFFECT ON DISTORTION

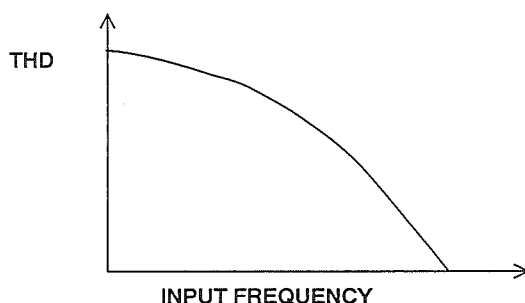
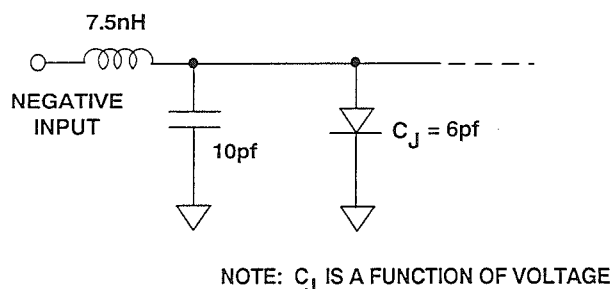


Figure 5.51

## Subranging ADCs

Although it is not practical to make flash ADCs with high resolution, flash ADCs are used as subsystems in “subranging” ADCs (sometimes known as “half-flash ADCs”), which are capable of much higher resolutions (up to 16-bits).

Figure 5.52 shows a basic subranging architecture. The analog signal is applied to an N-bit flash converter. The result of the conversion is applied to an

N-bit DAC with  $>2N$ -bit accuracy. The analog output from the DAC is subtracted from the original signal, and the remainder is amplified and applied to another N-bit flash ADC (or it could be switched to the same ADC that was used for the first conversion). The first conversion obtains the N MSBs. The D/A conversion and subtraction removes the MSB information from the analog signal, and the second A/D conversion provides the N LSBs.

## SUBRANGING (HALF-FLASH) ADC

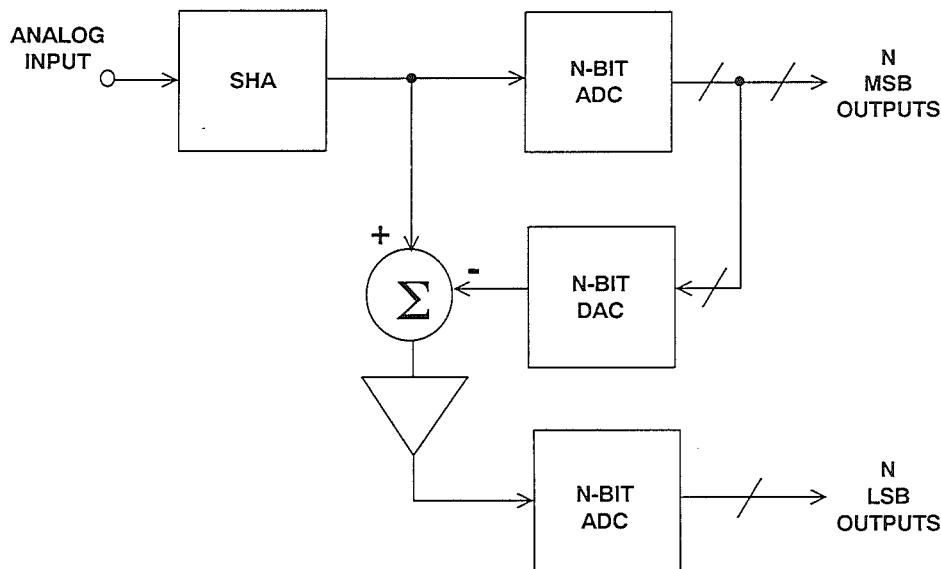


Figure 5.52

Obviously, such a procedure is not as fast as a simple flash conversion, but it is much faster than a successive approximation routine. Furthermore, the complexity and power for a given resolution is much less than for a flash converter. Subranging converters can have resolutions up to 16-bits and conversion rates of 50 MSPS (although not both together at the time of writing - mid 1994).

One of the limitations on the speed of a subranging converter is the settling

time and the accuracy of the first A/D conversion and the D/A conversion. Although the first stage conversion is only N bits, it must be performed to greater than 2N bits of accuracy. Any mismatch between the two stages, or any error in the first conversion will show up as errors in the overall ADC transfer function. An alternate architecture which is known as *subranging with digital error correction* relaxes the accuracy and settling time requirements on the first stage and allows faster operation (see Figure 5.53).

## SUBRANGING (HALF-FLASH) ADC WITH DIGITAL ERROR CORRECTION

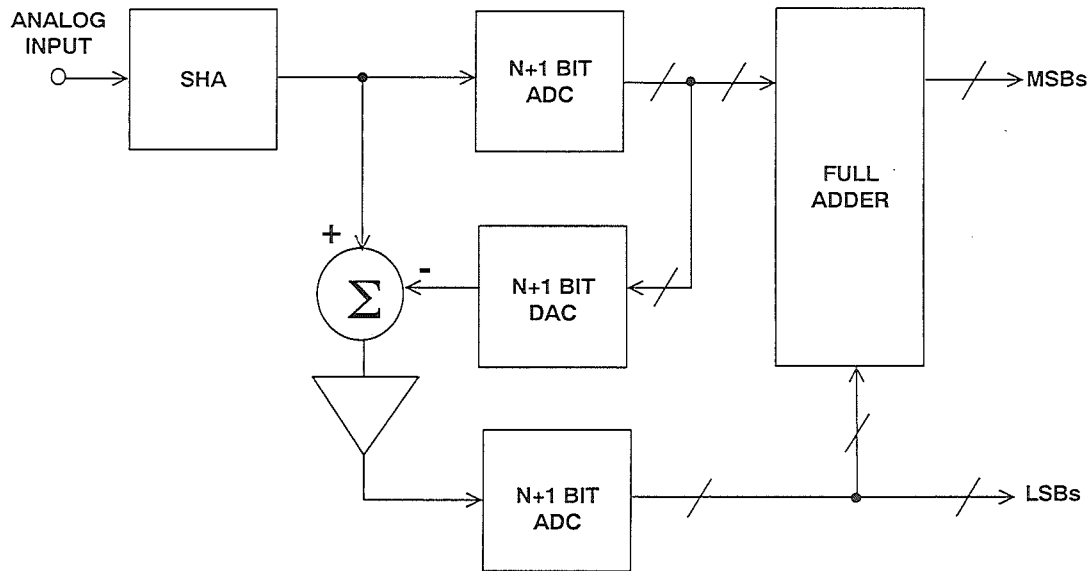


Figure 5.53

The basic architecture is unchanged, but the resolution of the two A/D conversions and the D/A conversion are increased by 1-bit. The first A/D conversion and the D/A conversion are performed more quickly, and there is some loss of accuracy due to inadequate settling time. However, the second A/D conversion is higher resolution and contains enough data to correct the error in the MSB conversion. The simplest way to do this is by use of a full adder. The increase in complexity is small, and the increase in speed and improvement in accuracy can be substantial.

So far, we have considered only two-stage subranging ADCs, as these are easiest to analyze. There is no reason to stop at two stages, however. Indeed, a successive approximation

ADC might be considered the limiting case of a multi-stage subranging ADC, although we do not propose to analyze it in this way. However, three-pass and four-pass subranging ADCs are quite common, and can be made in many different ways, with or without digital error correction.

As examples of just two of the many arrangements possible, Figure 5.54 shows a block diagram of the AD1671, a 1.25 MSPS ADC using 4-pass conversion with digital error correction, two separate DACs and four separate flash ADCs. The AD779, which achieves 14-bits at 128 KSPS with a single 4-bit flash ADC and one DAC is shown in Figure 5.55. Study of Reference 4 will reveal examples of many other structures.

The diagram illustrates a 12-bit digital-to-analog converter architecture. It begins with an **ANALOG INPUT** connected to a **SHA** (Successive Approximation Register) block. The SHA's output is fed into a summing junction ( $\Sigma$ ) with a positive sign. The output of this first summing junction is then fed into a second summing junction, also with a positive sign. The output of the second summing junction is connected to an **8-BIT DAC**. The output of the 8-BIT DAC is fed into a **4-BIT ADC**, which in turn provides feedback to the second summing junction with a negative sign. The output of the 4-BIT ADC is also fed into the **CONTROL AND CORRECTION LOGIC** block. The output of the 8-BIT DAC is also fed into the **CONTROL AND CORRECTION LOGIC** block. The output of the 4-BIT ADC is fed into another **4-BIT ADC**, which provides feedback to the first summing junction with a negative sign. The output of this final 4-BIT ADC is fed into the **CONTROL AND CORRECTION LOGIC** block. The output of the **CONTROL AND CORRECTION LOGIC** block is connected to the **OUTPUT LATCHES**, which provide a 12-bit output.

Figure 5.55

The block diagram illustrates the architecture of the SHA-1-based digital-to-analog converter. It features the following components and signal flow:

- ANALOG INPUT:** Provides a reference voltage to the SHA block.
- SHA (SHA-1 Processor):** Receives the analog input and outputs a 12-bit digital signal to the adder.
- Adder ( $\Sigma$ ):** A circular block with a '+' sign at the top and a '-' sign at the bottom, where the 12-bit signal from the SHA and the 12-bit feedback signal from the DAC are summed.
- PGA (Programmable Gain Amplifier):** Receives the output of the adder and provides gain control to the 4-bit ADC.
- 4-BIT ADC:** Converts the amplified signal into a 4-bit digital output.
- CONVERSION AND CONTROL LOGIC:** Receives the 4-bit output from the ADC and generates a 14-bit control signal for the DAC and a 14-bit output signal for the latches.
- 12-BIT DAC:** Receives the 12-bit feedback signal from the control logic and outputs a 12-bit digital signal to the adder.
- OUTPUT LATCHES:** Receive the 14-bit output signal from the control logic and provide the final 14-bit digital output.

Figure 5.55

## Integrating ADCs

Flash and subranging ADCs are fast, complex, power hungry, and are not inherently linear or free of missing codes. Integrating ADCs are simple,

linear, very accurate, free of missing codes, and consume very little power, but they are slow (see Figure 5.56).

### INTEGRATING ADC

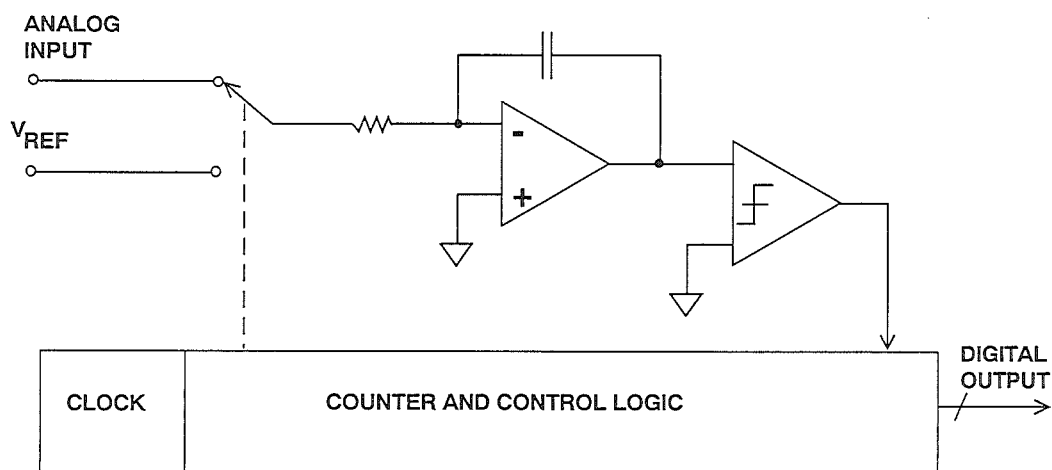


Figure 5.56

The integrator is charged from the unknown voltage for a fixed time defined by the converter clock. It is then fully discharged (connected to the reference voltage), and the discharge time measured by the same clock. The ratio of the input to the reference is the ratio of discharge to charge times. Since the integrator and the clock are the same during charge and discharge, they do not contribute to errors, although offset and bias currents do. However, these may be canceled out by using four charge/discharge cycles instead of two; the resulting conversion is very accurate.

Simple monolithic integrating ADCs using CMOS, which is not renowned for

its analog amplifier or comparator performance, are quite capable of 16-bit accuracy. The technique is used in most DVMs (digital voltmeters) from portable 2½ digit ones operating for hundreds of hours from a pair of button cells, to 6½ digit transfer standards. Another advantage of the technique for DVM applications is that if the input changes during a measurement the result of the conversion is the mean value of the input over the conversion cycle. If a suitable conversion time is chosen, 50Hz or 60Hz line ripple will essentially be ignored by an integrating ADC (see Figure 5.57).

## FREQUENCY RESPONSE OF INTEGRATING ADC

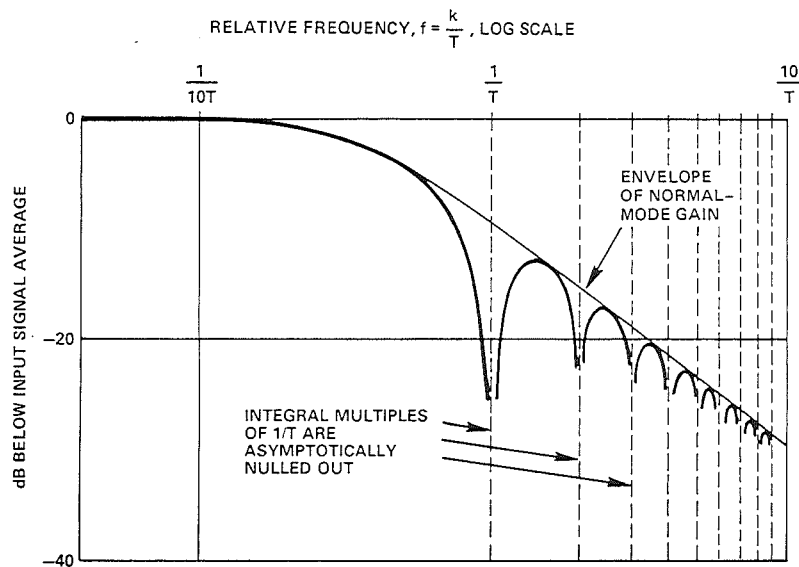


Figure 5.57

## Voltage-to-Frequency Converter (VFC) / Counter ADCs

Another integrating ADC consists of a VFC (voltage to frequency converter) and a frequency counter.

A VFC is an oscillator whose frequency is linearly proportional to a control voltage. The VFC/counter ADC is monotonic and free of missing codes,

integrates noise, and can consume very little power. It is also very useful for telemetry applications, since the VFC, which is small, cheap and low-powered can be mounted on the experimental subject (patient, wild animal, artillery shell, etc.) and communicate with the counter by a telemetry link.

## VOLTAGE-TO-FREQUENCY CONVERTER (VFC) AND FREQUENCY COUNTER MAKE A LOW-COST, VERSATILE, HIGH-RESOLUTION ADC

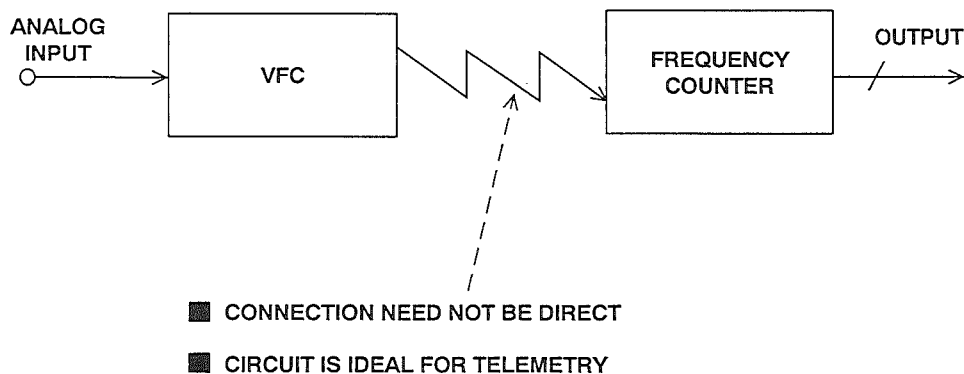


Figure 5.58

There are two common VFC architectures (there are many more VFO [variable frequency oscillator] architectures, including the ubiquitous 555, but the key feature of VFCs is linearity — few VFOs are very linear): the current steering multivibrator and the charge-balance VFC. The charge-balanced VFC may be made in asynchronous or synchronous (clocked) forms.

The current steering multivibrator is actually a current-frequency converter rather than a VFC, but, as shown in Figure 5.59, practical circuits invariably contain a voltage-current converter at

the input. The principle of operation is evident: the current discharges the capacitor until a threshold is reached, and when the capacitor terminals are reversed, the half-cycle repeats itself. The waveform across the capacitor is a linear tri-wave, but the waveform on either terminal with respect to ground is the more complex waveform shown.

Practical VFCs of this type have linearities around 14-bits, and comparable stability, although they may be used in ADCs with higher resolutions without missing codes. The performance limits are set by comparator threshold noise, threshold temperature coefficient,

and the stability and dielectric absorption (DA) of the capacitor, which is generally a discrete component. The comparator/voltage reference structure shown in the diagram is more of a representation of the function performed than the actual circuit used, which is much more integrated with the switching, and correspondingly harder to analyze.

This type of VFC is simple, inexpensive, and low-powered, and most run from a

wide range of supply voltages. They are ideally suited for low cost medium accuracy ADC and data telemetry applications.

The charge balance VFC is more complex, more demanding in its supply voltage and current requirements, and more accurate. It is capable of 16-18 bit linearity.

### A CURRENT-STEERING VFC

5

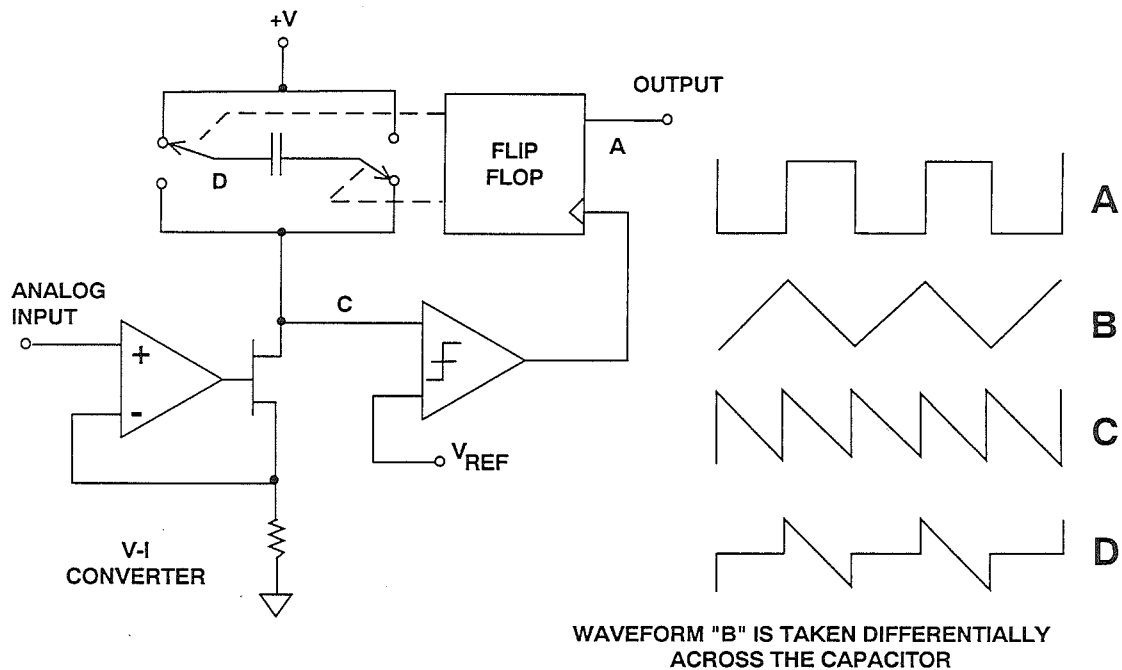


Figure 5.59



# CHARGE-BALANCE VFC

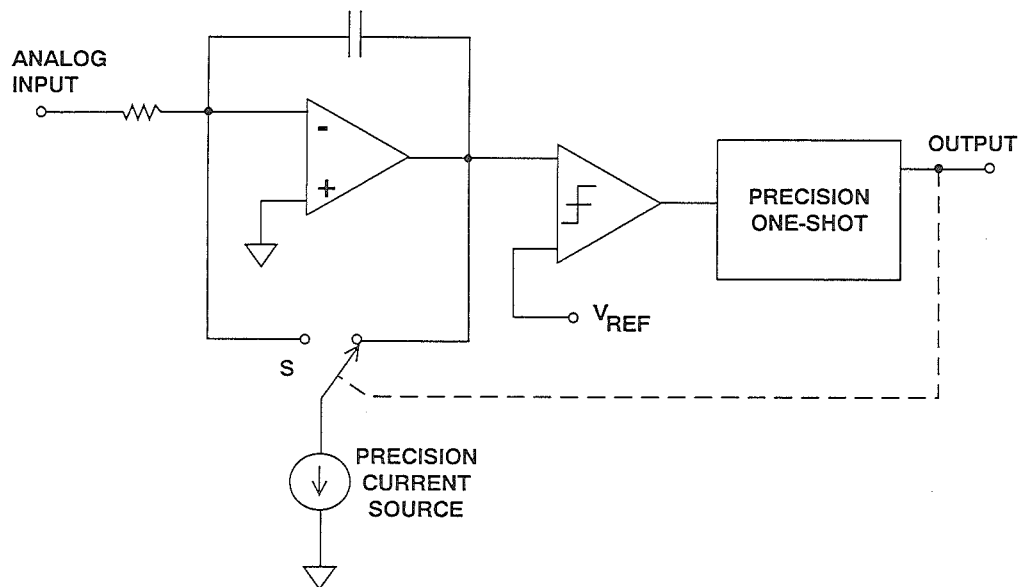


Figure 5.60

The integrator capacitor charges from the signal as shown in Figure 5.60. When it passes the comparator threshold, a fixed charge is removed from the capacitor, but the input current continues to flow during the discharge so no input charge is lost. The fixed charge is defined by the precision current source and the pulse width of the precision monostable. The output pulse rate is thus accurately proportional to the rate at which the integrator charges from the input.

At low frequencies, the limits on the performance of this VFC are set by the stability of the current source and the monostable timing (which depends on the monostable capacitor, among other things). The absolute value and temperature stability of the integration

capacitor do not affect the accuracy, although its leakage and dielectric absorption (DA) do. At high frequencies, second-order effects, such as switching transients in the integrator and the precision of the monostable when it is retriggered very soon after the end of a pulse, take their toll on accuracy and linearity.

The changeover switch in the current source addresses the integrator transient problem. By using a changeover switch instead of the on/off switch more common on older VFC designs: (a) there are no on/off transients in the precision current source and (b) the output stage of the integrator sees a constant load — most of the time the current from the source flows directly in the output stage; during charge balance, it still

flows in the output stage, but through the integration capacitor.

The stability and transient behavior of the precision monostable present more problems, but the issue may be avoided by replacing the monostable with a clocked bistable multivibrator. This arrangement is known as a *synchronous* VFC or SVFC and is shown in Figure 5.61.

The difference from the previous circuit is quite small, but the charge balance pulse length is now defined by two successive edges of the external clock. If this clock has low jitter, the charge will be very accurately defined. The output pulse will also be synchronous with the clock. SVFCs of this type are capable of up to 18-bit linearity and excellent temperature stability.

### SYNCHRONOUS VFC (SVFC)

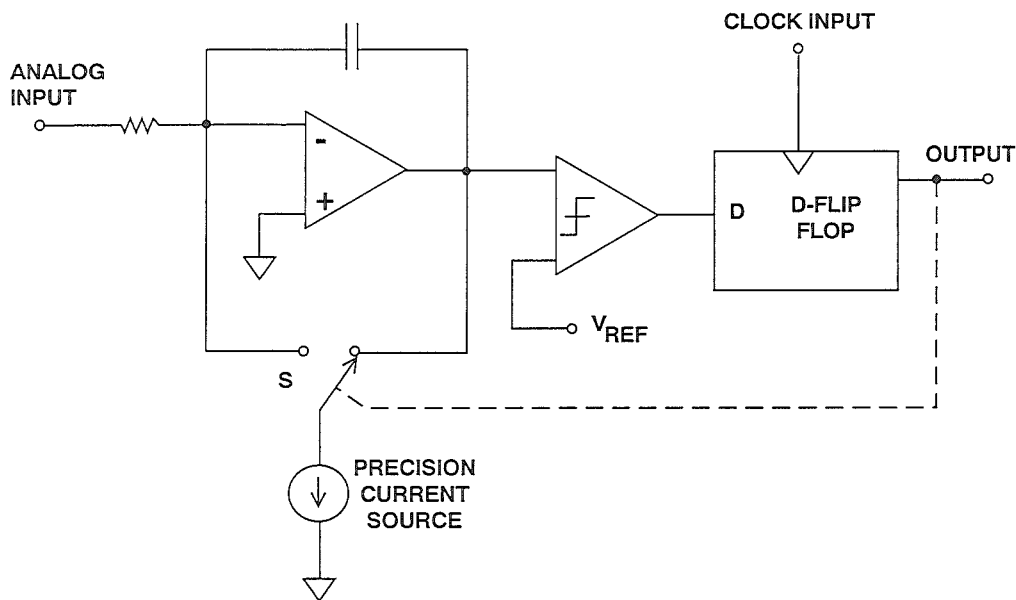


Figure 5.61

This synchronous behavior is convenient in many applications, since synchronous data transfer is often easier to handle than asynchronous. It does mean, however, that the output of an SVFC is not a pure tone (plus harmonics, of course) like a conventional VFC,

but contains components harmonically related to the clock frequency. The display of an SVFC output on an oscilloscope is especially misleading and is a common cause of inquiries to the Applications Department: a change of input to a VFC produces a smooth change in

the output frequency, but a change to an SVFC produces a change in probability density of output pulses  $N$  and  $N+1$  clock cycles after the previous output

pulse, which is often perceived by inexperienced users as severe jitter and a sign of a faulty device (see Figure 5.62).

## VFC AND SVFC WAVEFORMS

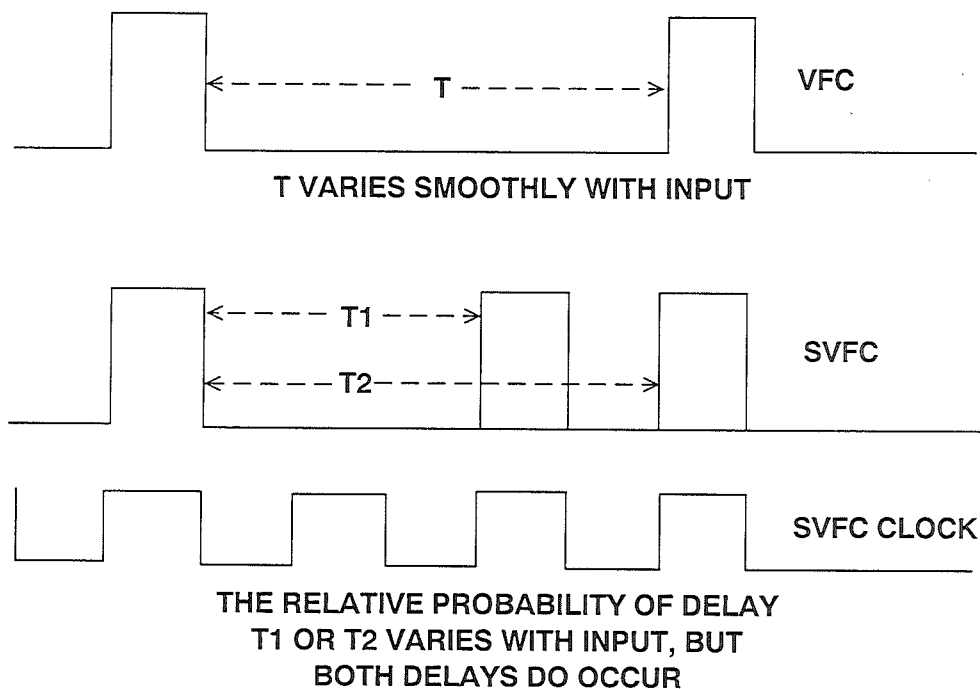


Figure 5.62

Another problem with SVFCs is non-linearity at output frequencies related to the clock frequency. If we study the transfer characteristic of an SVFC, we find non-linearities close to sub-harmonics of the clock frequency  $F_C$  as shown in Figure 5.63. They can be found at  $F_C/3$ ,  $F_C/4$ , and  $F_C/6$ . This is due to stray capacitance on the chip (and in the circuit layout!) and coupling the clock signal into the SVFC comparator which causes the device to behave as an injection-locked phase-locked loop (PLL). This problem is intrinsic to

SVFCs, but is not often serious: if the circuit card is well laid out, and clock amplitude and  $dV/dT$ s kept as low as practical, the effect is a discontinuity in the transfer characteristic of less than 8 LSBs (at 18-bit resolution) at  $F_C/3$  and  $F_C/4$ , and less at other sub-harmonics. This is frequently tolerable, since the frequencies where it occurs are known. Of course, if the circuit layout or decoupling is poor, the effect may be much larger, but this is the fault of poor design and not the SVFC itself.

## SVFC NON-LINEARITY

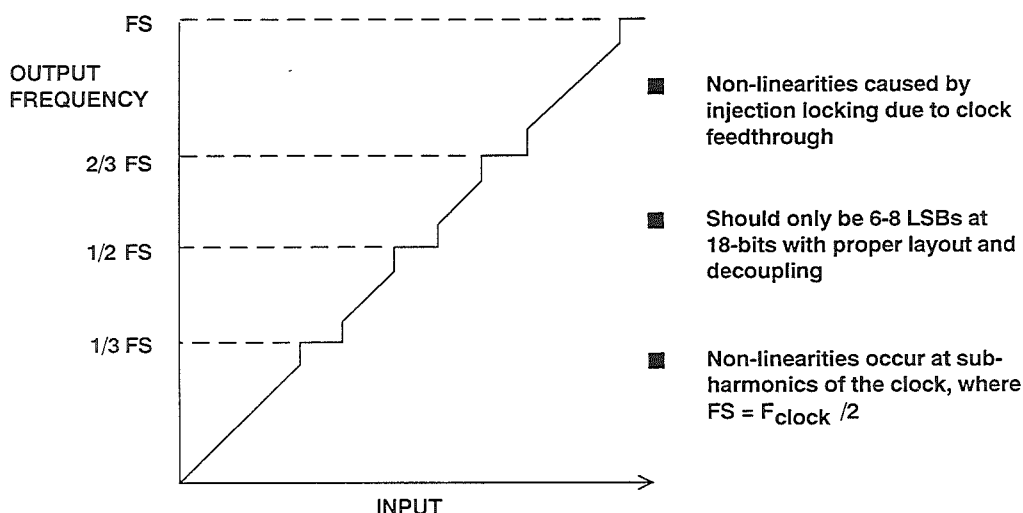


Figure 5.63

It is evident that the SVFC is quantized, while the basic VFC is not. It does NOT follow from this that the counter/VFC ADC has higher resolution (neglecting non-linearities) than the counter/SVFC ADC, because the clock in the counter also sets a limit to the resolution.

When a VFC has a large input, it runs quickly and (counting for a short time) gives good resolution, but it is hard to get good resolution in a reasonable sample time with a slow-running VFC. In such a case, it may be more practical to measure the period of the VFC output (this does not work for an SVFC), but of course the resolution of this system deteriorates as the input (and the frequency) increases. However, if the counter/timer arrangement is made smart, it is possible to measure the approximate VFC frequency and the

exact period of not one, but  $N$  cycles (where the value of  $N$  is determined by the approximate frequency), and maintain high resolution over a wide range of inputs. The AD1170 is an example of this architecture.

VFCs have more applications than as a component in ADCs. Since their output is a pulse stream, it may easily be sent over a wide range of transmission media (PSN, radio, optical, IR, ultra-sonic, etc.). It need not be received by a counter, but by another VFC configured as a frequency-voltage converter (FVC). This gives an analog output, and a VFC-FVC combination is a very useful way of sending a precision analog signal across an isolation barrier. There are a number of issues to be considered in building FVCs from VFCs, and these are considered in Reference 5.

## VFCs

- It is possible to use the PERIOD of a VFC, rather than its frequency, to measure the input signal.
- VFCs have other applications than as ADC elements. These include isolation and use as Frequency-to-Voltage Converters (FVCs).

Figure 5.64

## Tracking ADCs

Having considered two types of fast ADCs and two types of slow ADCs, it is interesting to consider a type which is both fast and slow. The *tracking* ADC

consists of a comparator, a DAC, and an up/down counter as shown in Figure 5.65.

## TRACKING ADC

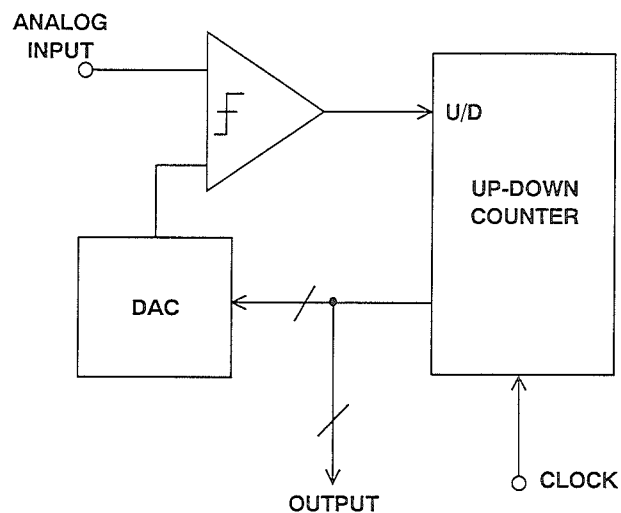


Figure 5.65

The analog input is applied to one input of the comparator, and the DAC output to the other. The DAC input is driven by the counter. If the analog input exceeds the DAC output, the counter counts up until they are equal. If the DAC output exceeds the analog input, the counter counts down until they are equal. It is evident that if the analog input changes slowly, the counter will follow, and the digital output will remain close to its correct value, whereas if the analog input suddenly undergoes a large step change, it will be many hundreds or thousands of clock cycles before the output is again valid - hence the statement that such an ADC is both fast and slow: it responds quickly to a slowly changing signal, but slowly to a quickly changing one.

The simple analysis above ignores the behavior of the ADC when the analog input and DAC output are nearly equal. This will depend on the exact nature of the comparator and counter. If the comparator is a simple one, the DAC output will cycle by 1 LSB from just above the analog input to just below it, and the digital output will, of course, do the same - there will be 1 LSB of flicker. Note that the output in such a case steps every clock cycle, irrespective of the exact value of analog input, and hence always has unity Mark/Space ratio. In other words, there is no possibility of taking a mean value of the

digital output and increasing resolution by oversampling.

A more satisfactory, but more complex arrangement would be to use a window comparator with a window 1-2 LSB wide. When the DAC output is high or low the system behaves as in the previous description, but if the DAC output is within the window, the counter stops. This arrangement eliminates the flicker, provided that the DAC DNL never allows the DAC output to step across the window for 1 LSB change in code.

Tracking ADCs are not very common. Their slow step response makes them unsuitable for many applications, and they have few compensating advantages. But they do have one asset: their output is *continuously* available. Most ADCs perform conversions: i.e., on receipt of a "start convert" command (which may be internally generated), they perform a conversion and, after a delay, a result becomes available. Providing that the analog input changes slowly, the output of a tracking ADC is always available. This is valuable in synchro-to-digital and resolver to digital converters (SDCs and RDCs), and this is the application where tracking ADCs are most often used. A very small change in their architecture, however, produces one of the most widespread ADC designs, the successive approximation ADC.

## Successive Approximation ADCs

In a successive approximation ADC (see Figure 5.66), the counter of the tracking ADC is replaced by a successive approximation register (SAR). The successive approximation ADC performs conversions on command. On the START CONVERT command, all the bits of the SAR are reset to "0" except the MSB which is set to "1". If the DAC output is greater than the analog input, this bit is reset, otherwise it is left set. The next most significant bit is then set to "1". If the DAC output is greater than the analog input, this bit is reset, otherwise it is left set. The process is repeated with each bit in turn. When all the bits have been set, tested, and reset or not as appropriate, the contents of

the SAR correspond to the value of the analog input, and the conversion is complete.

An N-bit conversion takes N steps. It would seem on superficial examination that a 16-bit converter would have one-half the conversion rate of an 8-bit one, but this is not the case. In an 8-bit converter, the DAC must settle to 8-bit accuracy before the bit decision is made, whereas in a 16-bit converter, it must settle to 16-bit accuracy, which takes a lot longer. In practice, 8-bit successive approximation ADCs can convert in a few hundred nanoseconds, while 16-bit ones will generally take several microseconds.

### SUCCESSIVE APPROXIMATION ADC

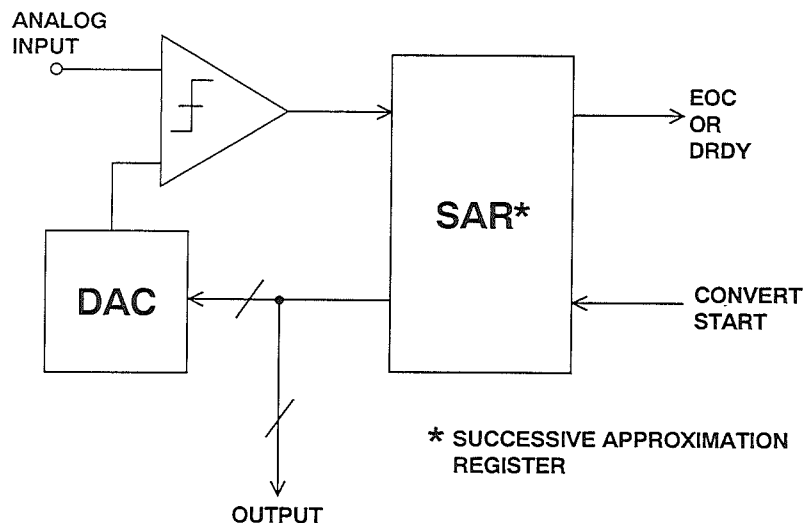


Figure 5.66

The successive approximation ADC has a very simple structure, is low power, and has reasonably fast conversion times. It is probably the most widely used ADC architecture, and will continue to be used for medium speed and medium resolution applications. As levels of analog integration increase, however, the subranging ADC will be

increasingly used for high-speed, medium resolution applications, and the rise of cheap digital signal processing (DSP) makes the sigma-delta architecture increasingly attractive for low bandwidths and very high resolutions. However, its theory is complex, and its mode of operation often misunderstood.

## Sigma-Delta ( $\Sigma$ - $\Delta$ ) ADCs

Sigma-Delta Analog-Digital Converters ( $\Sigma$ - $\Delta$  ADCs) have been known for nearly thirty years, but only recently has the technology (high-density digital VLSI) existed to manufacture them as inexpensive monolithic integrated circuits. They are now used in many applications where a low-cost, low-bandwidth, high-resolution ADC is required.

There have been innumerable descriptions of the architecture and theory of  $\Sigma$ - $\Delta$  ADCs, but most commence with a maze of integrals and deteriorate from there. In the Applications Department at Analog Devices, we frequently encounter engineers who do not understand the theory of operation of  $\Sigma$ - $\Delta$  ADCs and are convinced, from study of a typical published article, that it is too complex to comprehend easily.

There is nothing particularly difficult to understand about  $\Sigma$ - $\Delta$  ADCs, as long as you avoid the detailed mathematics, and this section has been written in an attempt to clarify the subject. A  $\Sigma$ - $\Delta$  ADC contains very simple analog electronics (a comparator, a switch, and one or more integrators and analog summing circuits), and quite complex digital computational circuitry. This circuitry consists of a digital signal processor (DSP) which acts as a filter (generally, but not invariably, a low pass filter). It is not necessary to know how the filter works to appreciate what it does. To understand how a  $\Sigma$ - $\Delta$  ADC works one should be familiar with the concepts of *over-sampling*, *noise shaping*, *digital filtering*, and *decimation*.



## SIGMA-DELTA ( $\Sigma$ - $\Delta$ ) ADCs

- Sigma-Delta ADCs are low-cost and have high resolution, excellent DNL, although limited input bandwidth
- A  $\Sigma$ - $\Delta$  ADC is Simple
- The Mathematics, however, is Complex
- This section concentrates on What Actually Happens!

Figure 5.67

## SIGMA-DELTA ADC KEY CONCEPTS

- Oversampling
- Noise Shaping
- Digital Filtering
- Decimation

Figure 5.68

As we have said earlier in this section, an ADC is a circuit whose digital output is proportional to the ratio of its analog input to its analog reference. Often, but by no means always, the scaling factor between the analog reference and the analog signal is unity, so the digital signal represents the normalized ratio of the two.

Figure 5.69 (which we have seen before) shows the transfer characteristic of such a 3-bit unipolar ADC. The input to an ADC is analog and is not quantized, but its output is quantized. The transfer characteristic therefore consists of eight horizontal steps (when considering the offset, gain and linearity of an ADC we consider the line joining the midpoints of these steps).

Digital full scale (all "1"s) corresponds to 1 LSB below the analog full scale (the

reference or some multiple thereof). This is because, as mentioned above, the digital code represents the *normalized* ratio of the analog signal to the reference, and if this were unity, the digital code would be all "0"s and "1" in the bit *above* the MSB.

The (ideal) ADC transitions take place at  $\frac{1}{2}$  LSB above zero and thereafter every LSB, until  $1\frac{1}{2}$  LSB below analog full scale. Since the analog input to an ADC can take any value, but the digital output is quantized, there may be a difference of up to  $\frac{1}{2}$  LSB between the actual analog input and the exact value of the digital output. This is known as the *quantization error* or *quantization uncertainty*. In AC (sampling) applications, this quantization error gives rise to *quantization noise*.

## TRANSFER CHARACTERISTIC OF A 3-BIT UNIPOLAR ADC

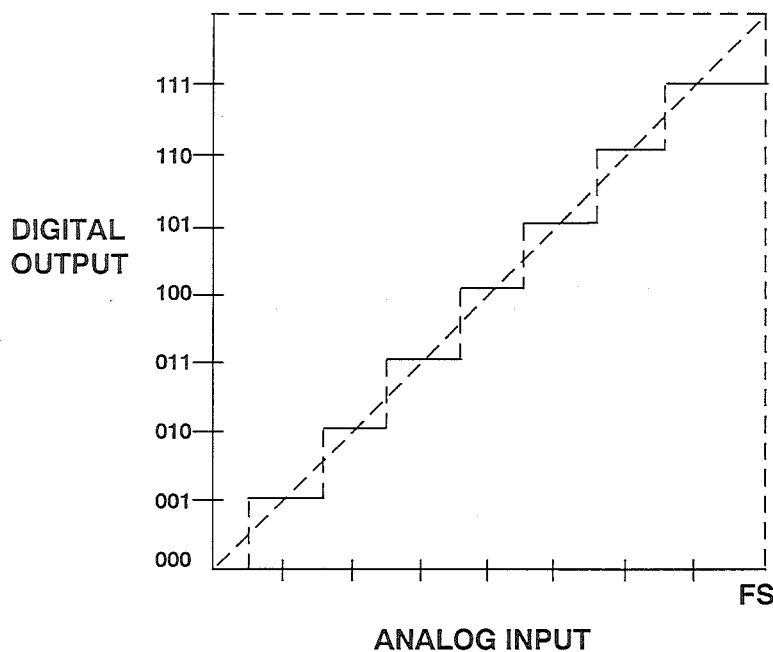


Figure 5.69

If we apply a fixed input to an ideal ADC, we will always obtain the same output, and the resolution will be limited by the quantization error.

Suppose, however, that we add some AC (dither) to the fixed signal, take a large number of samples, and prepare a

histogram of the results. We will obtain something like the result in Figure 5.70. If we calculate the mean value of a large number of samples, we will find that we can measure the fixed signal with greater resolution than that of the ADC we are using. This procedure is known as *over-sampling*.

## OVERSAMPLING

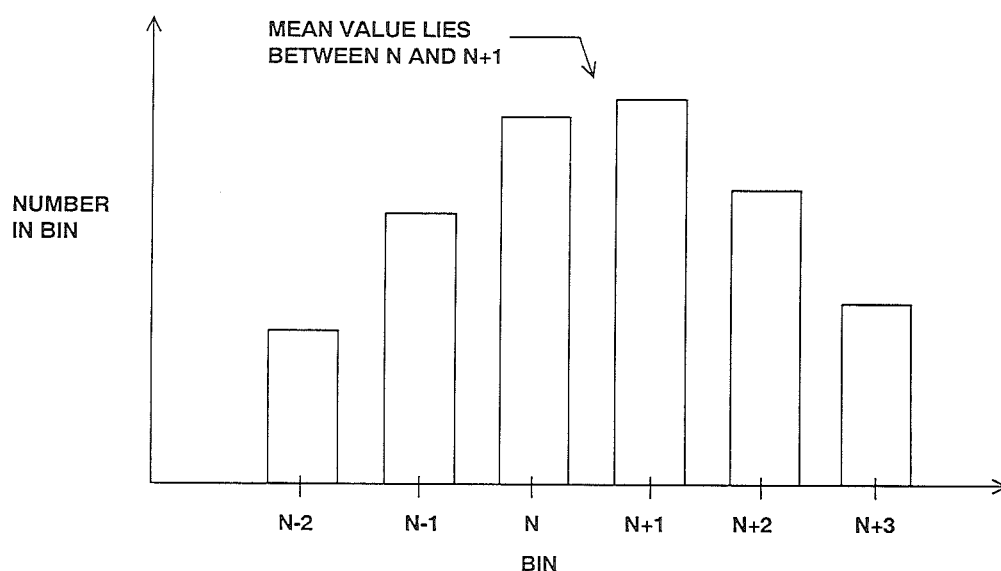


Figure 5.70

The AC (dither) that we add may be a sine-wave, a tri-wave, or gaussian noise (but *not* a square wave) and, with some types of sampling ADCs (including  $\Sigma$ - $\Delta$  ADCs), an external dither signal is unnecessary, since the ADC generates its own. Analysis of the effects of differing dither waveforms and amplitudes is complex and, for the purposes of this section, unnecessary. What we do need to know is that with the simple over-sampling described here, the number of samples must be doubled for each bit of increase in resolution.

If, instead of a fixed DC signal, the signal that we are over-sampling is an AC signal, then it is not necessary to add a dither signal to it in order to over-sample, since the signal is moving anyway. (If the AC signal is a single tone harmonically related to the sampling frequency, dither may be necessary, but this is a special case.)

Let us consider the technique of over-sampling with an analysis in the frequency domain. Where a DC conversion has a *quantization error* of up to  $\frac{1}{2}$  LSB,

a sampled data system has *quantization noise*. As we have already seen, a perfect classical N-bit sampling ADC has an rms quantization noise of  $q/\sqrt{12}$  uniformly distributed within the Nyquist band of DC -  $f_s/2$  (where  $q$  is the value of an LSB and  $f_s$  is the sampling rate). Therefore, its SNR with a full-scale sinewave input will be  $(6.02N + 1.76)$  dB. If the ADC is less than perfect, and its noise is greater than its theoretical minimum quantiza-

tion noise, then its *effective* resolution will be less than N-bits. Its actual resolution (often known as its Effective Number of Bits or ENOB) will be defined by

$$\text{ENOB} = \frac{\text{SNR} - 1.76\text{dB}}{6.02\text{dB}}.$$

5

## SAMPLING ADC QUANTIZATION NOISE

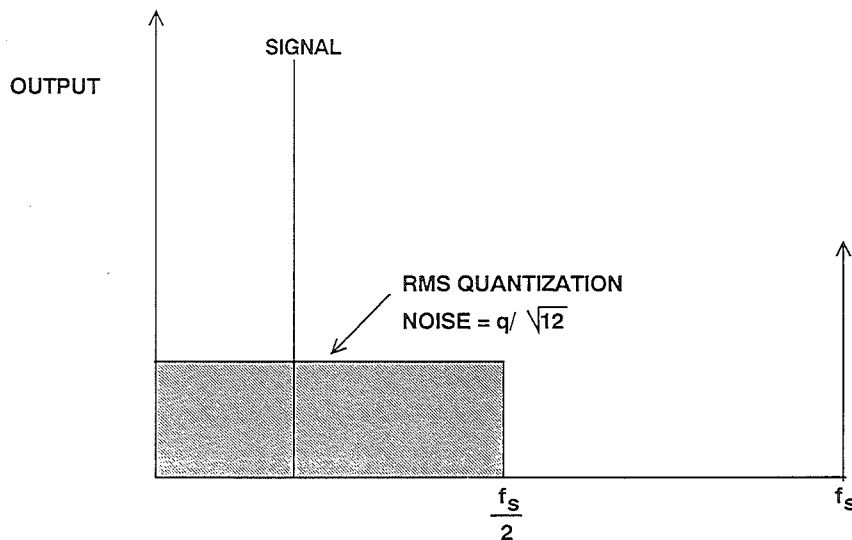


Figure 5.71

If we choose a much higher sampling rate, the quantization noise is distributed over a wider bandwidth as shown in Figure 5.72. If we then apply a digital low pass filter (LPF) to the output, we remove much of the quanti-

zation noise, but do not affect the wanted signal - so the ENOB is improved. We have accomplished a high resolution A/D conversion with a low resolution ADC.

## OVERSAMPLING FOLLOWED BY DIGITAL FILTERING AND DECIMATION IMPROVES SNR AND ENOB

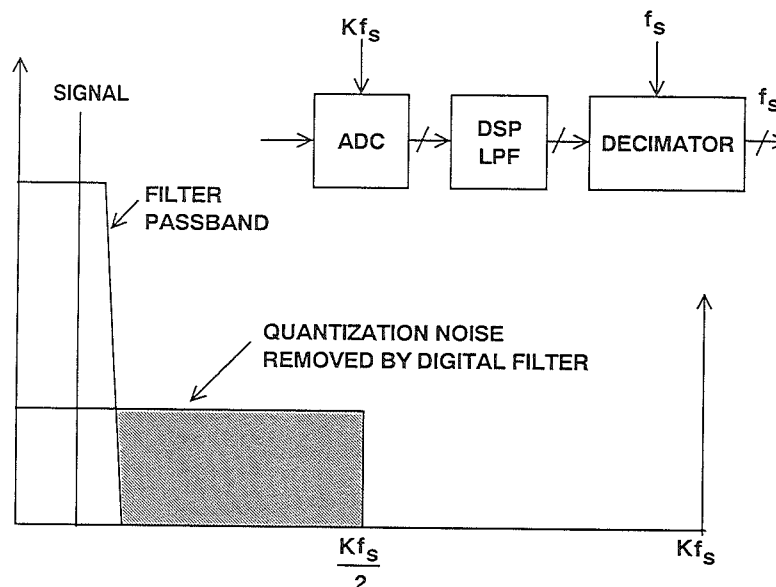


Figure 5.72

Since the bandwidth is reduced by the digital output filter, the output data rate may be lower than the original sampling rate and still satisfy the Nyquist criterion. This may be achieved by passing every Mth result to the output and discarding the remainder. The process is known as "decimation" by a factor of M. Despite the origins of the term (*decem* is Latin for ten), M can have any integer value, provided that the output data rate is more than twice the signal bandwidth. Decimation does not cause any loss of information (see Figure 5.73).

If we simply use over-sampling to improve resolution, we must over-sample by a factor of  $2^N$  to obtain an N-bit increase in resolution. The  $\Sigma$ - $\Delta$  converter does not need such a high over-sampling ratio because it not only limits the signal passband, but also shapes the quantization noise so that it falls outside this passband.

If we take a 1-bit ADC (generally known as a comparator), drive it with the output of an integrator, and feed the integrator with an input signal summed with the output of a 1-bit DAC fed from

## DECIMATION

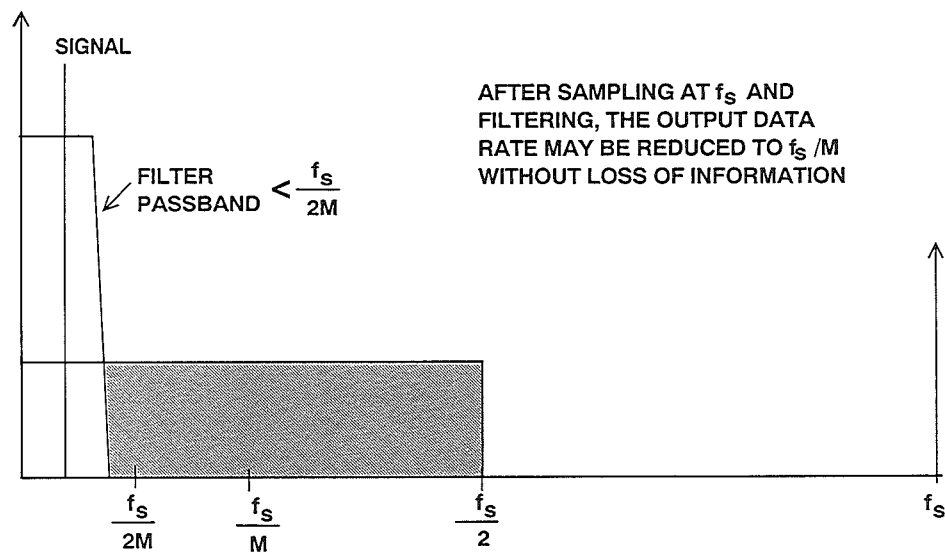


Figure 5.73

## FIRST-ORDER SIGMA-DELTA ADC

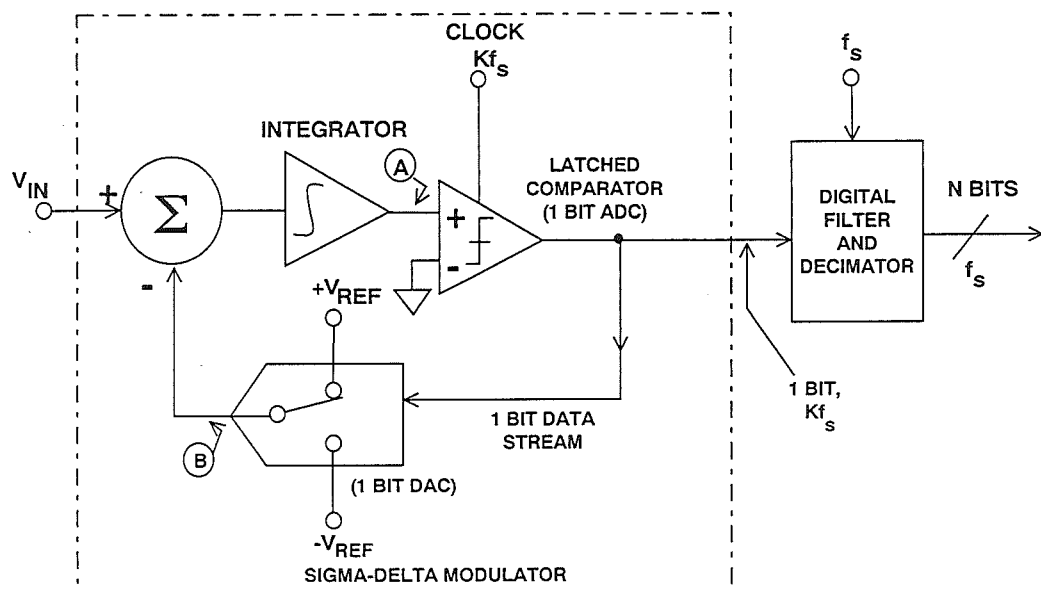


Figure 5.74

the ADC output, we have a first-order  $\Sigma$ - $\Delta$  modulator as shown in Figure 5.74. Add a digital low pass filter (LPF) and decimator at the digital output, and we have a  $\Sigma$ - $\Delta$  ADC: the  $\Sigma$ - $\Delta$  modulator shapes the quantization noise so that it lies above the passband of the output filter, and the ENOB is therefore much larger than would otherwise be expected from the over-sampling ratio.

By using more than one integration and summing stage in the  $\Sigma$ - $\Delta$  modulator, we can achieve higher orders of quantization noise shaping and even better ENOB for a given over-sampling ratio

as is shown in Figure 5.75 for a second-order  $\Sigma$ - $\Delta$  modulator. The block diagram for the second-order  $\Sigma$ - $\Delta$  modulator is shown in Figure 5.76. Third, and higher, order  $\Sigma$ - $\Delta$  ADCs were once thought to be potentially unstable at some values of input — recent analyses using *finite* rather than infinite gains in the comparator have shown that this is not necessarily so, but even if instability does start to occur, it is not important, since the DSP in the digital filter and decimator can very easily recognize incipient instability and react to prevent it.

## SIGMA-DELTA MODULATORS SHAPE QUANTIZATION NOISE

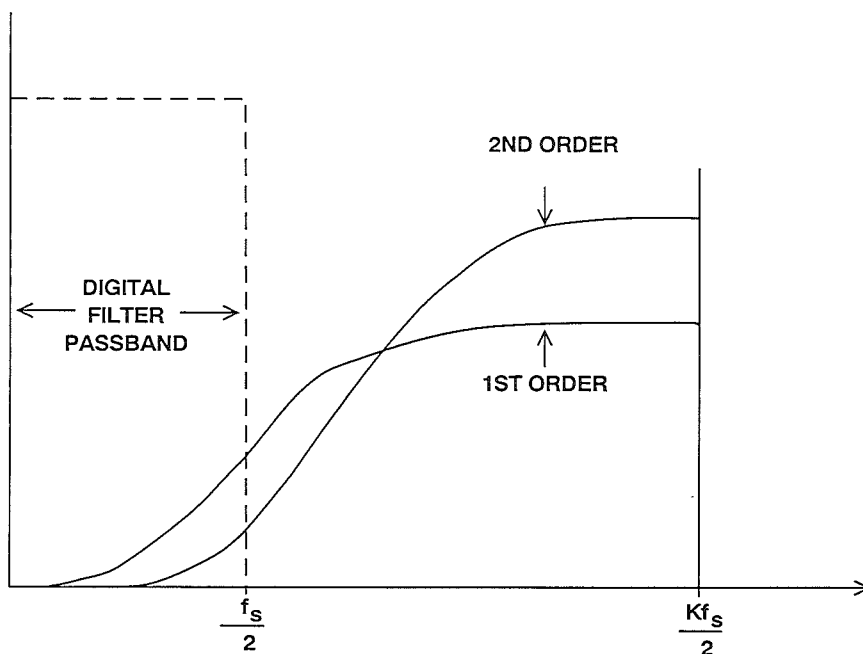


Figure 5.75

## SECOND-ORDER SIGMA-DELTA ADC

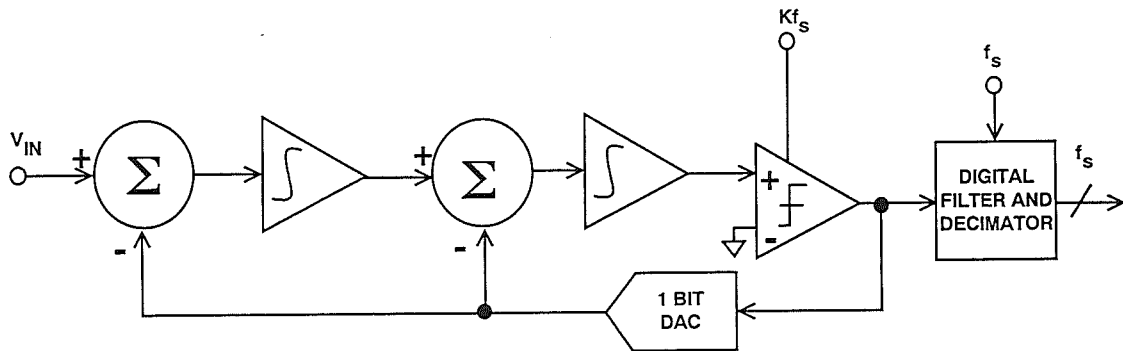


Figure 5.76

Figure 5.77 shows the relationship between the order of the  $\Sigma$ - $\Delta$  modulator

and the amount of over-sampling necessary to achieve a particular SNR.

## SNR VERSUS OVERSAMPLING RATIO FOR FIRST, SECOND, AND THIRD-ORDER LOOPS

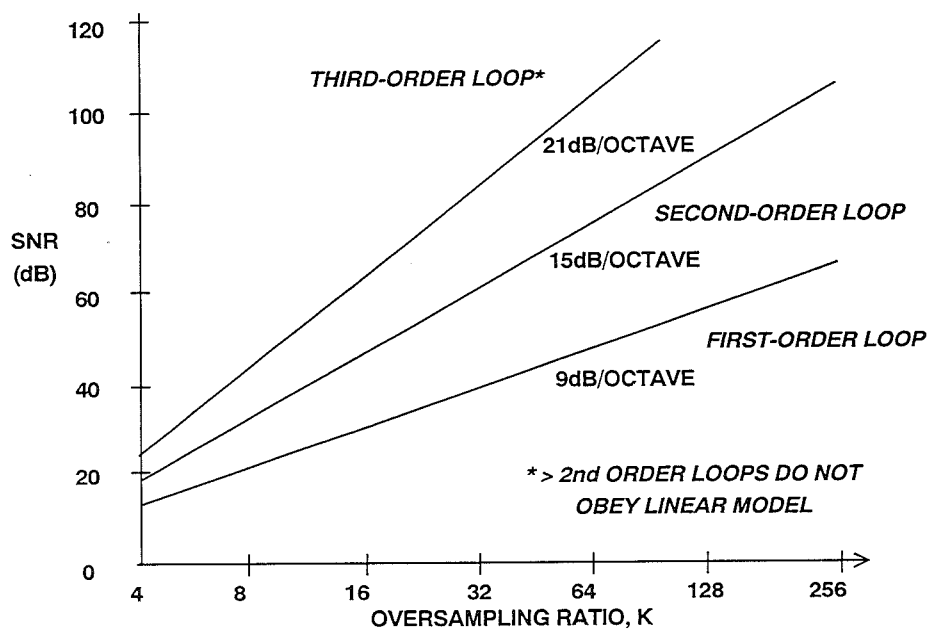


Figure 5.77



The  $\Sigma$ - $\Delta$  ADCs that we have described so far contain integrators, which are low pass filters, whose passband extends from DC. Thus, their quantization noise is pushed up in frequency. At present, all commercially available  $\Sigma$ - $\Delta$  ADCs are of this type (although some which are intended for use in audio or telecommunications applications contain bandpass rather than lowpass digital filters to eliminate any system DC offsets).  $\Sigma$ - $\Delta$  ADCs are available with resolutions up to 24-bits for DC measurement applications (AD7710), and with resolutions of 18-bits for high quality digital audio applications (AD1879).

But there is no particular reason why the filters of the  $\Sigma$ - $\Delta$  modulator should

be LPFs, except that traditionally ADCs have been thought of as being baseband devices, and that integrators are somewhat easier to construct than bandpass filters. If we replace the integrators in a  $\Sigma$ - $\Delta$  ADC with bandpass filters (BPFs), the quantization noise is moved up and down in frequency to leave a virtually noise-free region in the pass-band (see Reference 6). If the digital filter is then programmed to have its pass-band in this region, we have a  $\Sigma$ - $\Delta$  ADC with a bandpass, rather than a low pass characteristic (see Figure 5.78). Although studies of this architecture are in their infancy, such ADCs would seem to be ideally suited for use in digital radio receivers, medical ultrasound, and a number of other applications.

## REPLACING INTEGRATORS WITH RESONATORS GIVES A BANDPASS SIGMA-DELTA ADC

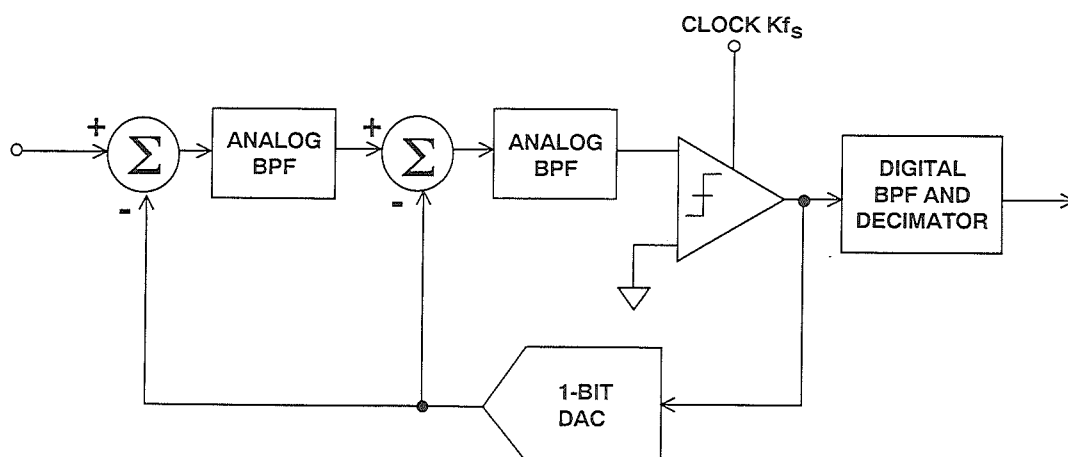


Figure 5.78

A  $\Sigma$ - $\Delta$  ADC works by over-sampling, where simple analog filters in the  $\Sigma$ - $\Delta$  modulator shape the quantization noise so that the SNR *in the bandwidth of interest* is much lower than would otherwise be the case, and by using high performance digital filters and decimation to eliminate noise outside the required passband. Because the analog circuitry is so simple and undemanding, it may be built with the same digital VLSI process that is used to

fabricate the DSP circuitry of the digital filter. Because the basic ADC is 1-bit (a comparator), the technique is inherently linear.

Although the detailed analysis of  $\Sigma$ - $\Delta$  ADCs involves quite complex mathematics, their basic design can be understood without the necessity of any mathematics at all. For further discussion on  $\Sigma$ - $\Delta$  ADCs, refer to References 7 and 8.

## SIGMA-DELTA SUMMARY

- Inherently Excellent Linearity
- Ideal for Mixed-Signal IC Processes, no Trimming
- No SHA Required
- Upper Sampling Rate Currently Limits Applications to Measurement, Voiceband, and Audio, but Bandpass Sigma-Delta Techniques Will Change This
- Analog Multiplexing Applications are Limited by Internal Filter Settling Time. Consider One Sigma-Delta ADC per Channel.

Figure 5.79

## Sample and Hold Amplifiers (SHAs)

If successive approximation and subranging ADCs are to work correctly, the analog input must remain constant to within  $\pm\frac{1}{2}$  LSB during conversion. If we calculate the constraints that this imposes on the maximum input fre-

quency, it is alarming: the maximum full-scale sinusoidal input frequency to a  $10\mu\text{s}$ , 16-bit ADC is 0.24 Hz - less than one cycle every four seconds. The Nyquist frequency of such a converter, however, is 50kHz.

### THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF THE ADC TO HIGHER FREQUENCIES

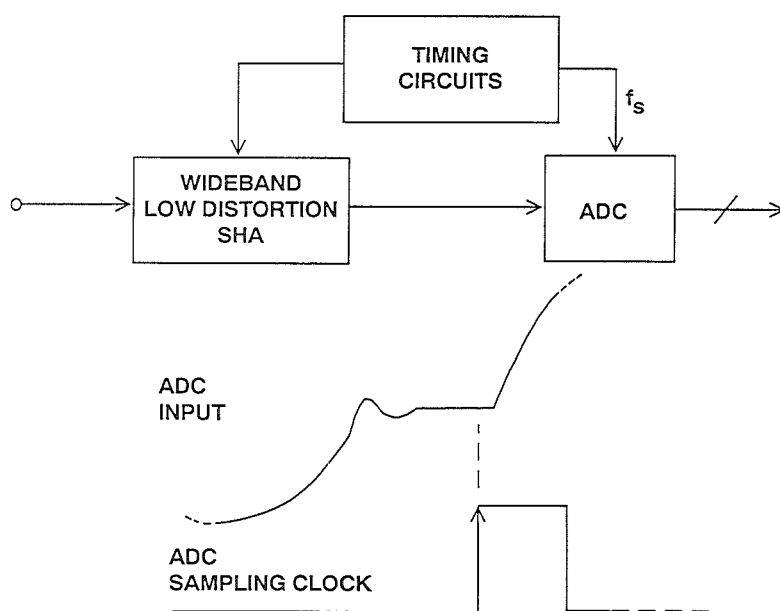


Figure 5.80

To overcome the problem (and also to improve the ENOB of some flash ADCs), all that is necessary is to incorporate a sample-and-hold (SHA) in the system as we have already mentioned. A SHA is a circuit which latches an analog signal in the state that it was at the moment a "sample" command was received. Sample-and-hold circuits are

often referred to as "track-and-hold" circuits (THAs, or T/Hs). For most purposes the two terms are interchangeable, though there is a difference: the output of a SHA does not need to track the analog input at any time, whereas a THA must track as well as hold. For ADC input applications, the track function is not necessary, but

there are other places where it is. SHAs are discussed in detail in Section 8 of this book and Reference 9, and it is not necessary to analyze them here.

Most modern ADCs incorporate the SHA function on chip. This is usually far better than using a separate SHA, since the parameters of the SHA will be tailored to the needs of the ADC, and the whole system will be specified, rather than having separate SHA and ADC specifications which must be married together.

In general, *sampling* ADCs with integrated SHAs should be used wherever the system design requires the use of a SHA. One exception is with flash ADCs, since most flash ADCs are built with processes that are incapable of making a good SHA. Another is where the ENOB of an ADC working at a low sampling rate and a high input frequency (“undersampling”) can be improved by a better external SHA.

## REFERENCES

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7. **System Applications Guide**, Analog Devices, Inc., 1994, Section 14.
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## SECTION 6

### INTERFACING TO ADCs AND DACs

- Driving ADC Inputs
- ADC Input Clamping and Protection Circuits
- Effective Input Noise of ADCs
- Drive Amplifier Noise Considerations
- ADC Reference Voltage Considerations
- Capturing ADC Output Data
- Interfacing ADC Outputs to DSPs in Realtime Signal Processing Applications
- Interfacing to DACs
- Interfacing DSPs to DACs
- Buffering DAC Outputs
- Deglitching DACs Using SHAs
- $\text{SIN}(x)/X$  Frequency Rolloff Effect
- Supplying the Reference Voltage for DACs
- Sampling Clock Generation for ADCs and DACs
- Power Supplies, Ground Planes, Decoupling, and Layout:  
Power Supplies, Grounding, Decoupling, Sockets,  
Prototyping High Performance Analog Circuitry



## SECTION 6

# INTERFACING TO ADCs AND DACs

*Walt Kester*

This section examines the fundamentals of interfacing to ADCs and DACs. ADC inputs require an appropriate drive amplifier to buffer the signal and provide gain and offset capability. DAC outputs may also require buffering. Both ADCs and DACs require low-jitter

sampling clocks to control the conversion rate, some require external voltage references, and all require proper attention to layout, signal routing, power supply generation and decoupling, and grounding.

### ADC AND DAC INTERFACING

- ADC Input / DAC Output Amplifier
- External Reference Voltage Generation
- Capturing ADC Output Data / Buffering DAC Input Data
- Sampling Clock Generation
- Proper Layout and Signal Routing
- Power Supply Generation, Filtering, Decoupling
- Proper use of Ground Planes and Grounding Techniques

Figure 6.1



## DRIVING ADC INPUTS

Selecting the appropriate drive amplifier for an ADC involves many considerations. Because the ADC drive amplifier is in the signal path, its error sources (both dc and ac) must be considered in calculating the total error budget. Ideally, the ac and dc performance of

the amplifier should be such that there is no degradation of the ADC performance. It is rarely possible to achieve this, however; and therefore the effects of each amplifier error source on system performance should be evaluated individually.

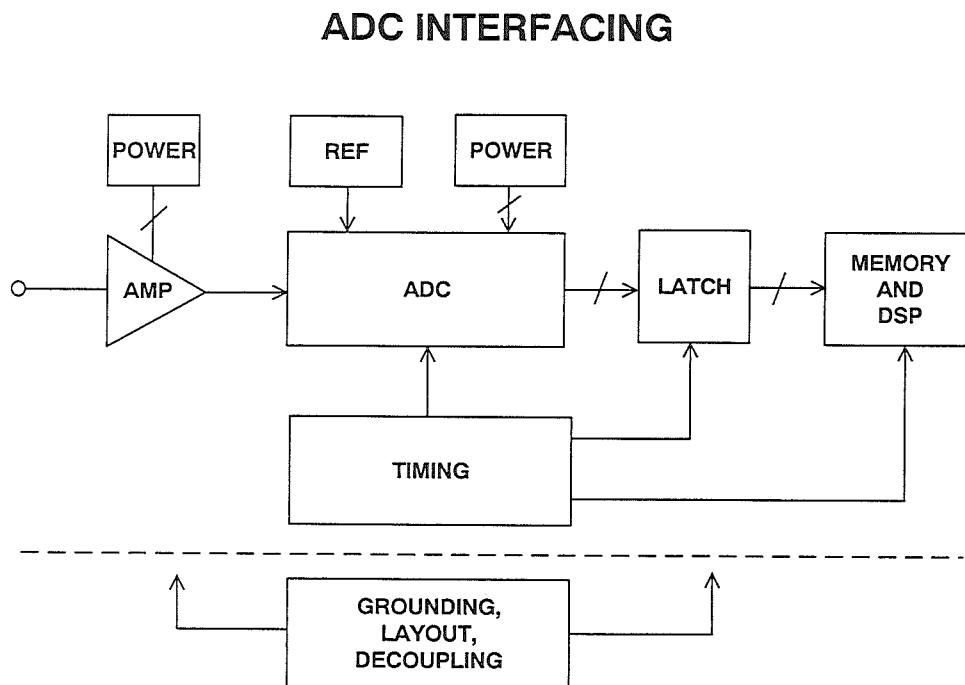


Figure 6.2

Evaluating and selecting op-amps based on the dc requirements of the system is a relatively straightforward matter. For many applications, however, it is more desirable first to select an amplifier on the basis of ac performance (bandwidth, THD, Noise, etc.) The ac characteristics of ADCs are specified in terms of SNR,

ENOBs, and distortion. The drive amplifier should have performance which is better than that of the ADC so that maximum dynamic performance is obtained (see Figure 6.4.). If the amplifier ac performance is adequate, the dc specifications should then be examined in terms of system performance.

## ADC DRIVE AMPLIFIER CONSIDERATIONS

- AC Performance -
  - ◆ Bandwidth, Settling Time
  - ◆ Harmonic Distortion, Total Harmonic Distortion
  - ◆ Noise, THD + Noise
- DC Performance -
  - ◆ Gain, Offset, Drift
  - ◆ Gain Non-Linearity
- As a general principle, select first for AC performance, then evaluate DC performance.
- Always consult the data sheet for recommendations!!

6

Figure 6.3

THE DISTORTION AND NOISE PERFORMANCE OF THE DRIVE AMPLIFIER SHOULD BE BETTER THAN THE ADC

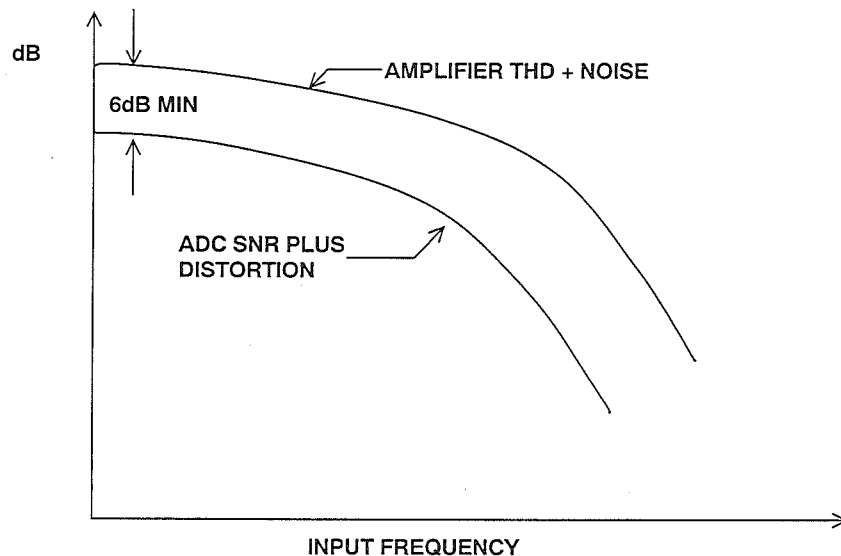


Figure 6.4

One must also understand the analog input circuit of the ADC and its effect on the amplifier. Flash converters generally present a varying capacitive load to the amplifier which may cause instability and distortion. Sampling ADCs often present rather benign loads to the drive amplifier because of their internal track-and-hold. However, some sampling ADC architectures, such as switched-capacitor or sigma-delta, may generate current spikes from which the drive amplifier must quickly settle. A simple model for estimating transient settling time is shown in Figure 6.5. The closed-loop output impedance of an

op-amp increases with frequency and may be as great as several hundred ohms at high frequencies due to the equivalent output inductance of the complementary emitter follower output stage. The transient load current will develop a transient voltage across this impedance at the op amp output. This small perturbation will decay exponentially with a time constant equal to  $1/2\pi f_{cl}$  ( $f_{cl}$  = closed loop bandwidth) if the op-amp exhibits single pole response. The simple exponential decay formula can be used to determine the settling to any desired accuracy.

## SMALL SIGNAL MODEL ALLOWS ESTIMATION OF OP AMP SETTLING TIME DUE TO TRANSIENT LOAD CURRENT

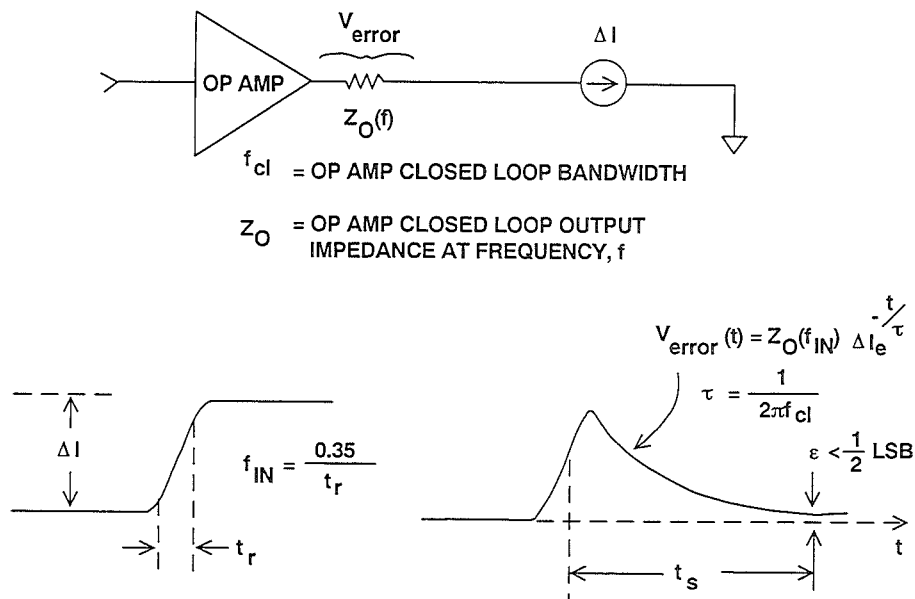


Figure 6.5

Settling from transient load currents is not generally a problem in an op-amp which has been properly selected to drive sampling converters. The op-amp small-signal bandwidth will generally

be high (with respect to the sampling rate) in order to achieve low levels of distortion. The wide bandwidth will automatically yield fast settling to transient currents if they are present.

While it is important to understand the concepts presented above regarding op-amp selection, ADC manufacturers such as Analog Devices generally recommend

appropriate drive amplifiers in their data sheets, so the selection process is relatively straightforward in most cases.

## ADC INPUT CLAMPING AND PROTECTION CIRCUITS

Most ADCs will tolerate out-of-range signals in the order of 50% or so without damage to the input circuit, provided the overvoltage does not go outside the supplies. An exception to this are certain flash converters which have unipolar negative input ranges. This will be discussed shortly.

For example, an ADC with an input range of  $\pm 5\text{V}$  should tolerate an input signal up to  $\pm 7.5\text{V}$ . The overvoltage recovery time of an ADC (Figure 6.6) usually increases as the input signal moves further out of range.

### ADC OVERVOLTAGE RECOVERY TIME

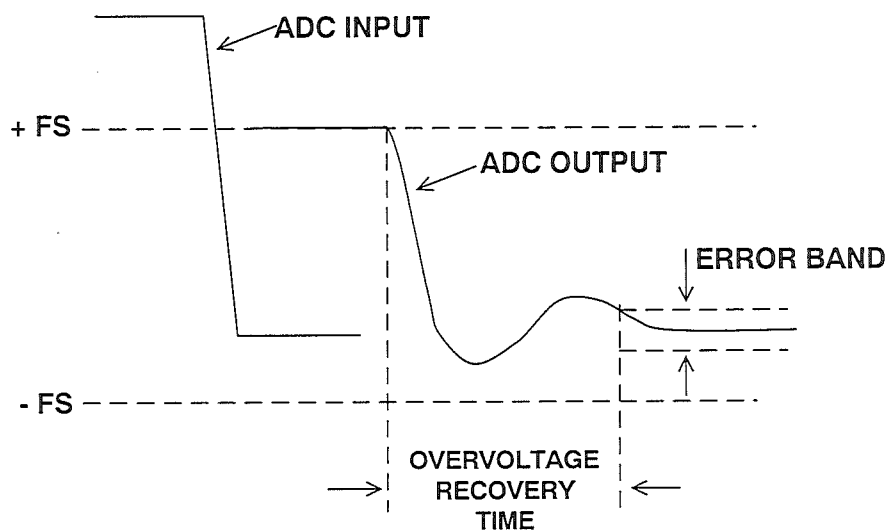


Figure 6.6

It may therefore be desirable to clamp the ADC input so that the input signal is limited to small overrange values, especially if large out-of-range signals are frequent. Clamping not only protects the internal ADC input circuits from damage, but also reduces the overvoltage recovery time. Because the clamping circuit is in the signal path, care must be taken to insure that it does not degrade the system performance for normal signals. Specially designed low distortion amplifiers, such as the AD8036 and AD8037, contain internal clamping circuits and are ideal for this purpose. Recovery time from overdrive is less than 5ns.

Other conditions of temporary overvoltage may occur because of power supply

sequencing. Several possibilities will be discussed briefly.

Figure 6.7 shows an op amp powered by  $\pm 15\text{V}$  supplies driving an ADC which is powered by  $\pm 5\text{V}$  supplies (typical of many CMOS ADCs). If the op amp supplies are brought up before the ADC supplies, an overvoltage condition on the ADC input may cause latch up and destroy the device. In addition, the analog input voltage to a CMOS ADC should never exceed the supply voltages, or a latch-up condition may occur. The diodes shown in the figure will protect against this condition. In fact, many CMOS ADCs have the protection diodes on-chip.

### PROTECTION AGAINST LATCH-UP AND DAMAGE DUE TO POWER SUPPLY SEQUENCING

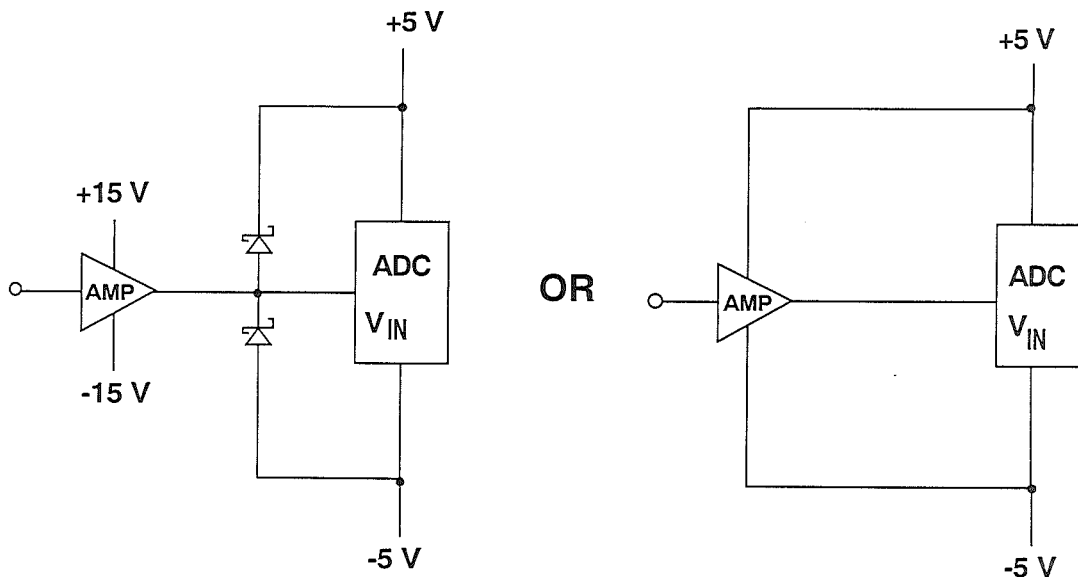


Figure 6.7

An alternative is also shown in Figure 6.7. If a  $\pm 5\text{V}$  supply op amp is chosen, then both the ADC and the op amp may be powered from the same supplies, thereby eliminating the potential latch-up problem. It should be noted that many op amps have specifications for both  $\pm 15\text{V}$  and  $\pm 5\text{V}$  supply operation. If

a  $\pm 15\text{V}$  op amp must be used, the  $\pm 5\text{V}$  for the CMOS ADC may be derived from a three-terminal voltage regulator as shown in Figure 6.8. This is relatively efficient because most CMOS ADCs are low power devices, and is preferable to powering a  $\pm 5\text{V}$  CMOS converter from noisy  $\pm 5\text{V}$  logic supplies.

## USING 3-TERMINAL REGULATORS AS ADC SUPPLIES

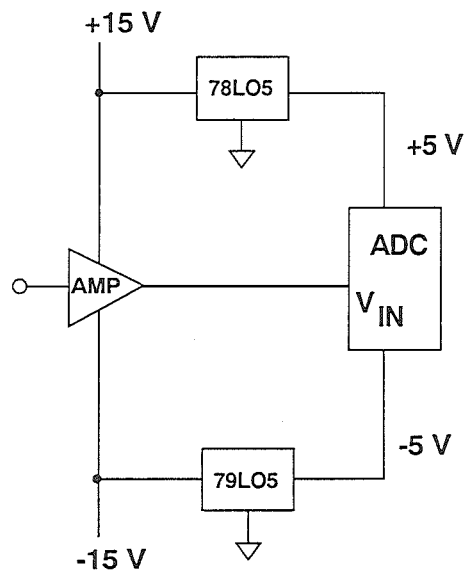


Figure 6.8

Many flash converters are designed to operate on a single  $-5.2\text{V}$  power supply and have a negative input voltage range of 0 to  $-2\text{V}$ . If the input goes positive, the substrate silicon diode begins to conduct. Forward current above a few mA may permanently degrade the performance of the flash converter. Input Schottky diodes should be installed as shown in Figure 6.9 to

prevent this happening. Most amplifiers suitable for driving flash converters operate on dual  $5\text{V}$  supplies and can deliver 50 to  $100\text{mA}$  of output current. The series resistor should be chosen to limit this current to an acceptable level. Two diodes should be paralleled if more than  $50\text{mA}$  current is expected from the drive amplifier.

## PROTECTING FLASH CONVERTER INPUTS WITH SCHOTTKY DIODES

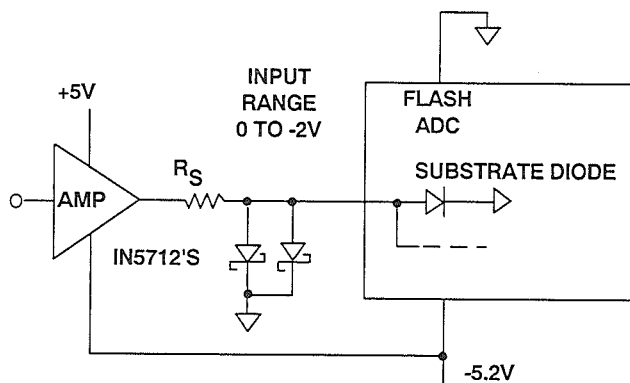


Figure 6.9

## EFFECTIVE INPUT NOISE OF ADCs

Wide bandwidth 12 to 16-bit sampling ADCs behave differently from non-sampling 12-bit SAR ADCs such as the AD574. Ideally, a fixed dc input to an ADC should result in the same output code for each conversion (of course, the dc input should be centered between the transition regions of the two adjacent codes). In the past, ADCs were analyzed for code transition noise using a DAC to reconstruct the analog signal. A very slow ramp voltage was applied to the

ADC, so that each code transition could be observed. In a high-resolution sampling converter, for a given input voltage, a range of output codes may occur. This is because of unavoidable circuit noise within the wideband circuits in the ADC. If a dc signal is applied to a precision sampling ADC (such as the 16-bit, 166kSPS AD7884/AD7885) and several thousand outputs are recorded, a distribution of codes such as that shown in Figure 6.10 will result.

### AD7884/AD7885 HISTOGRAM OF 5000 CONVERSIONS FOR A DC INPUT SHOWS 5 LSB p-p OR 0.8 LSB RMS EQUIVALENT INPUT NOISE

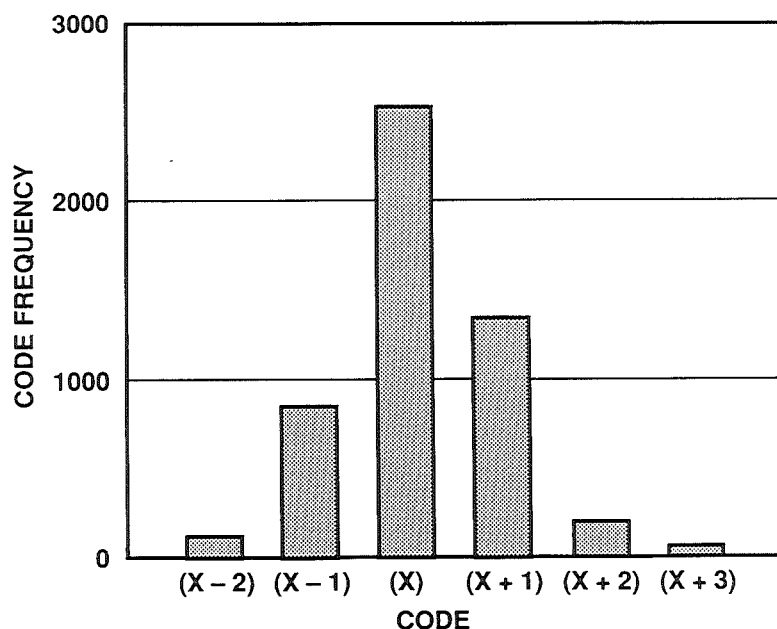


Figure 6.10

The correct code appears most of the time, but adjacent codes appear as well with reduced probability. If a Gaussian probability distribution is fitted to the histogram, the standard deviation is approximately equivalent to the equivalent input rms noise of the ADC. The actual specification on the ADC data sheet may be given in terms of a histogram or may be converted into an equivalent input rms noise voltage. In Figure 6.10, the peak-to-peak noise is about 5 LSBs, corresponding to  $5/6 = 0.8$  LSBs rms (Peak-to-peak values may be converted into rms values by dividing by 6). For a 6V input span, this corresponds to  $74\mu\text{V}$  rms equivalent input noise.

This noise may come from several sources. For example, a  $1\text{M}\Omega$  resistor generates  $158\mu\text{V}$  rms noise over a 1MHz single-pole bandwidth (the equivalent noise bandwidth is 1.57MHz). One LSB for the AD7884 operating with a 6V peak-to-peak input

range is  $92\mu\text{V}$ . This illustrates the importance of keeping the source impedances low. Some of the internal ADC noise is generated in the wideband SHA. Sampling ADCs generally have input bandwidths which exceed the Nyquist frequency of one-half the sampling rate. (The AD7884/AD7885 has an input bandwidth which exceeds 1MHz, even though the maximum sampling rate is 166kSPS). These wide bandwidth front ends are required in order to minimize gain and phase distortion at the signal frequencies and to optimize performance in undersampling applications. A certain amount of unavoidable noise is generated in the SHA and the other wideband circuits within the ADC which cause the sample-to-sample variation in output codes for dc inputs. Good layout, grounding, and decoupling techniques are essential to prevent additional external noise from coupling into the ADC and adding to the inherent equivalent input noise.



# DRIVE AMPLIFIER NOISE CONSIDERATIONS

Most sampling ADCs have input bandwidths much greater than their maximum sampling rate  $f_s$ . The ADC drive amplifier must also have wide bandwidth, generally greater than the ADC. Any output noise generated by the op-amp must therefore be integrated over the full input bandwidth of the ADC as shown in Figure 6.11. This rms noise should be calculated and compared with the ADC input noise specification. Details of how to perform this calculation are given in Section 1. The op-amp output noise should be 2 to 3 times less than the ADC input noise. If this is not the case, a lower-noise op-amp should be selected.

If the input-referred noise of the ADC is not specified, then the op-amp output noise should be compared to the theoretical quantization noise,  $q/\sqrt{12}$ . Again, it should be 2 to 3 times less.

The effects of op-amp noise are reduced by placing the anti-aliasing filter between the amplifier and the ADC input. The op-amp noise is then only integrated over the bandwidth of the anti-aliasing filter. In undersampling applications, the anti-aliasing filter will be a *bandpass* rather than an *lowpass* filter.

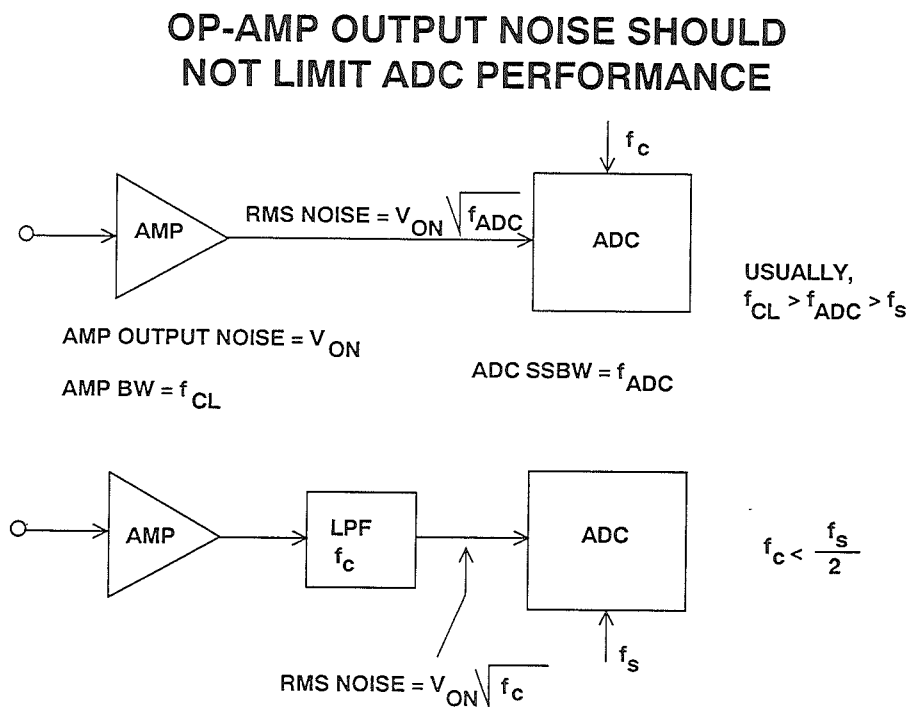


Figure 6.11

## ADC REFERENCE VOLTAGE CONSIDERATIONS

Many ADCs have internal voltage references, others do not. If the ADC has an internal reference, it is often pinned-out so that an external reference can be used to provide better stability and lower noise. External references generally perform better than internal ones because the IC processes used for data converters are less than ideal for

precision low-noise references. Sometimes, however, the internal reference is not very accurate, but the ADC is trimmed to high accuracy using whatever reference voltage the internal reference supplies. In such cases, an accurate external reference voltage may actually reduce the converter's dc accuracy.

### INTERNAL VERSUS EXTERNAL DATA CONVERTER REFERENCES

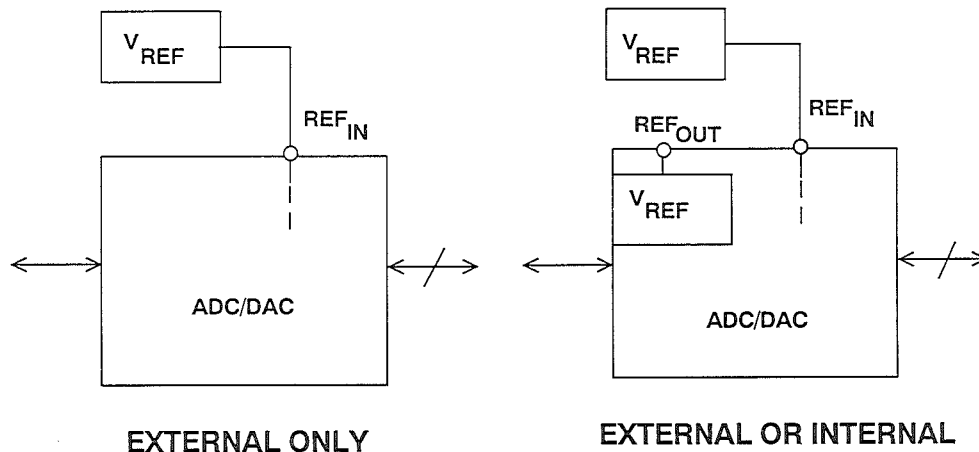


Figure 6.12

The reference voltage is important because it establishes the fullscale range of the ADC, and the overall dc accuracy and stability of the ADC can be no better than that of the reference. Standard monolithic reference voltages are 2.5V, 3V, 5V, and 10V. Noise on the ADC reference generally translates directly into increased internal noise levels and degraded SNR performance.

The entire voltage reference function is available in ICs which utilize laser trimmed thin film resistors for excellent accuracy and low drift. Standard dc specifications for such a voltage reference are output current capability, line regulation, load regulation, output voltage tolerance, and output voltage change with temperature. AC specifications include turn-on settling time,

transient load current settling time, and noise. Selecting voltage references based on dc requirements is relatively straightforward. Evaluating its noise performance deserves further discussion.

Most voltage references specify peak-to-peak noise in a 0.1Hz to 10Hz bandwidth. For instance, the AD586 (a 5V buried zener reference with on-chip output buffer) specification in this bandwidth is  $4\mu\text{V}$  peak-to-peak. In most sampling ADC applications, however, the wideband noise is usually of more concern. For the AD586, the unfiltered noise in a 1MHz bandwidth is approximately  $200\mu\text{V}$  peak-to-peak, corresponding to  $200/6 = 33\mu\text{V}$  rms. This value is usually larger for bandgap voltage references such as the REF-02 ( $800\mu\text{V}$  peak-to-peak). Regardless of the type of reference chosen, proper exter-

nal filtering can virtually eliminate the wideband noise.

Some voltage references, such as the AD586, have a pin brought out designated as the noise reduction pin (see Figure 6.13). Connecting an external capacitor between ground and this pin forms a single-pole lowpass filter with an internal  $4000\Omega$  resistor. For instance, an external  $1\mu\text{F}$  capacitor produces a single-pole corner frequency of approximately 40Hz. This filter virtually eliminates the broadband buried-zener noise, but the output buffer amplifier (approximate bandwidth is 1MHz) still produces approximately  $160\mu\text{V}$  peak-to-peak noise in the 1MHz bandwidth, so the capacitor is not as useful as might be expected. It also greatly increases the reference startup time.

## PRECISION LOW NOISE ADC VOLTAGE REFERENCE

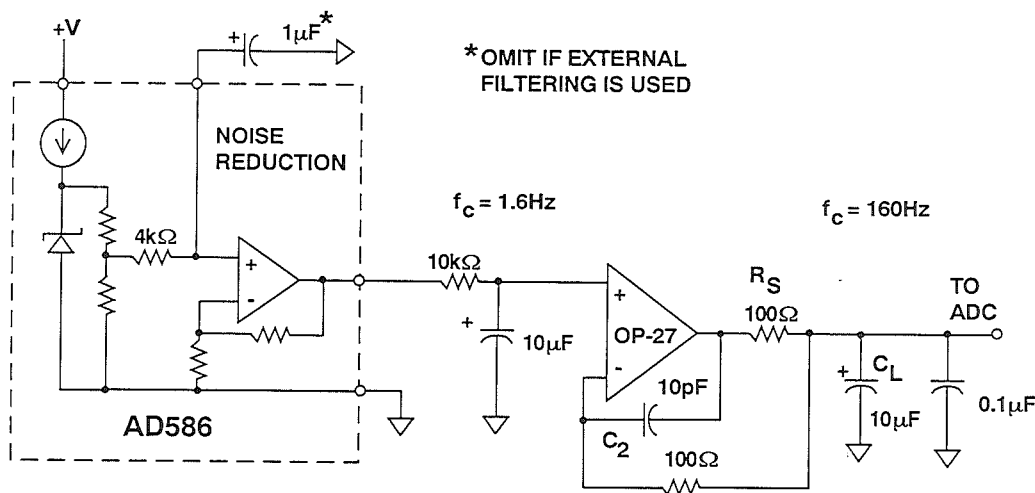


Figure 6.13

If low noise is required, adding a large capacitor on the reference output ( $10\mu\text{F}$ ) will reduce the noise somewhat. This, however, may not produce the expected results for two reasons. First, the voltage reference output buffer amplifier has a low closed-loop output impedance, on the order of a few ohms at low frequencies. The additional large capacitor does little to reduce this impedance further. Second, loading the output of the internal op amp with a large capacitor may cause the op amp to become unstable and to oscillate or ring under transient load conditions. (This is not the case with the AD780 2.5V/3V reference which is designed to be stable regardless of its capacitive load).

The ideal solution in precision applications is to use an external filter such as the one shown in Figure 6.14. The  $10\text{k}\Omega$  resistor and the  $10\mu\text{F}$  capacitor form a single-pole passive filter which has a corner frequency of  $1.6\text{Hz}$ , and reduces the noise to approximately the value specified in the  $0.1$  to  $10\text{Hz}$  frequency band ( $4\mu\text{V}$  peak-to-peak for the AD586 and the AD780). This passive filter is followed by a precision low noise buffer amp such as the OP-27 ( $V_n = 3\text{nV}/\sqrt{\text{Hz}}$ ). The large load capacitor  $C_L = 10\mu\text{F}$  serves two purposes. First, it forms a lowpass filter with  $R_S$  having a corner frequency of approximately  $160\text{Hz}$ . This reduces the output voltage noise of the op amp to a negligible value. Second, it provides additional reference voltage

stability by acting as a charge reservoir to any transient load current. This amount of capacitance is a heavy load on any op amp; therefore,  $R_S$  and  $C_2$  compensate for the pole introduced by  $C_L$  and the op amp's output resistance. This compensation scheme ensures that the buffer circuit recovers and settles from the output transients quickly without the long settling tails that might produce conversion errors. The  $0.1\mu\text{F}$  capacitor in parallel with  $C_L$  is to keep the output impedance low at high frequencies, where the large  $10\mu\text{F}$  electrolytic capacitor becomes less effective.

When using external filtering, do not decouple the noise reduction pin of the reference (if it has one) with a capacitor as it will increase the reference startup time.

In applications where filtering the voltage reference noise is not required, the decoupling capacitors on the ADC reference voltage input terminal may be eliminated completely. Simply buffer the voltage reference output with a precision low noise high bandwidth amplifier which has sufficient transient load settling time, such as the AD845 (see Figure 6.14). This approach will minimize the need for additional components, but dc precision and noise performance will be sacrificed.

## WIDEBAND LOW-NOISE BUFFER AMPLIFIER ELIMINATES THE NEED FOR LARGE DECOUPLING CAPACITORS

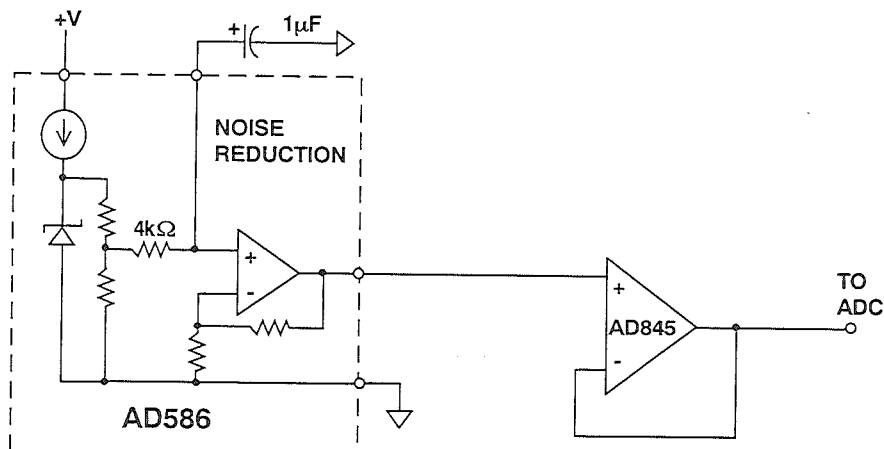


Figure 6.14

## CAPTURING ADC OUTPUT DATA

There are basically two output formats for ADC data: parallel and serial. We will deal first with the parallel case. Flash converters are parallel output devices. A typical timing diagram for a flash converter (AD9048 8-bit, 35MSPS ADC) is shown in Figure 6.15. The conversion process is initiated by the rising edge of the CONVERT pulse. The output data begins to change  $t_{oh}$  ns later and settles  $t_{pd}$  ns after the rising edge. The data is then valid and may be clocked into an external register. Notice, however, that the data corresponds to the sample taken by the previous convert pulse, i.e., there is a one-clock-cycle *pipeline* delay. This is typical in

flash converters because of an internal latch as shown in the AD9048 block diagram (Figure 6.16). The clock to the external latch should be positioned somewhere within the interval in which the output data is stable. In many cases the leading or trailing edge of the CONVERT signal can be used for this purpose. The data sheet for the particular device should be consulted for specific timing details. It is highly recommended that a buffer latch be used between the ADC and the memory or data bus. The reasons will be discussed in more detail later in this section.

## AD9048 8-BIT, 35MSPS FLASH CONVERTER TIMING DIAGRAM SHOWS PIPELINE (LATENCY) DELAY IN THE OUTPUT DATA

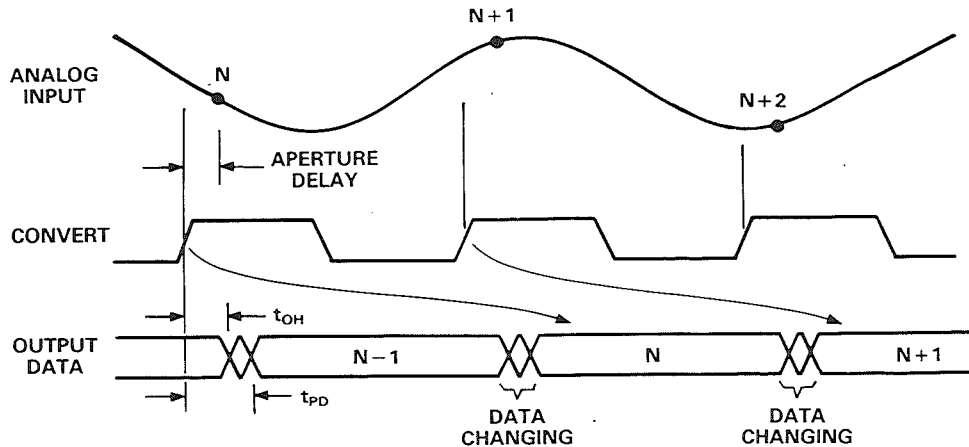


Figure 6.15

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## BLOCK DIAGRAM OF THE AD9048 FLASH CONVERTER

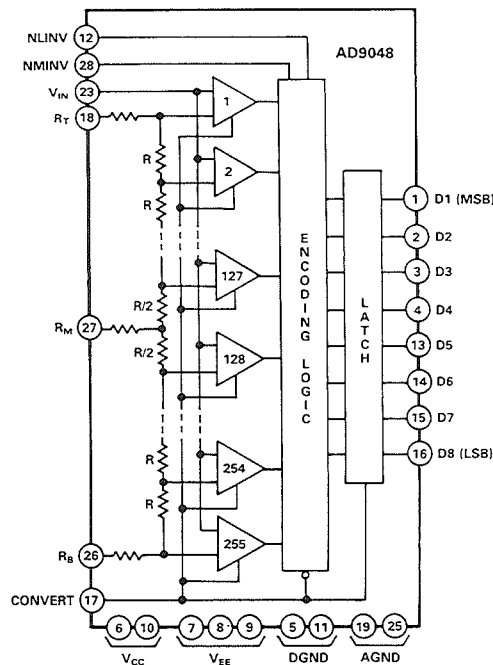


Figure 6.16

Subranging ADCs may have several clock cycles of pipeline delay, or latency. A block diagram of the AD872 12-bit, 10MSPS ADC is shown in Figure 6.17. The conversion is implemented using a 4-stage pipelined multiple flash archi-

tecture with error correction. The timing diagram for the device is shown in Figure 6.18. Note that there are three clock-cycle delays in the output data.

## AD872 12-BIT, 10MSPS PIPELINED ADC ARCHITECTURE

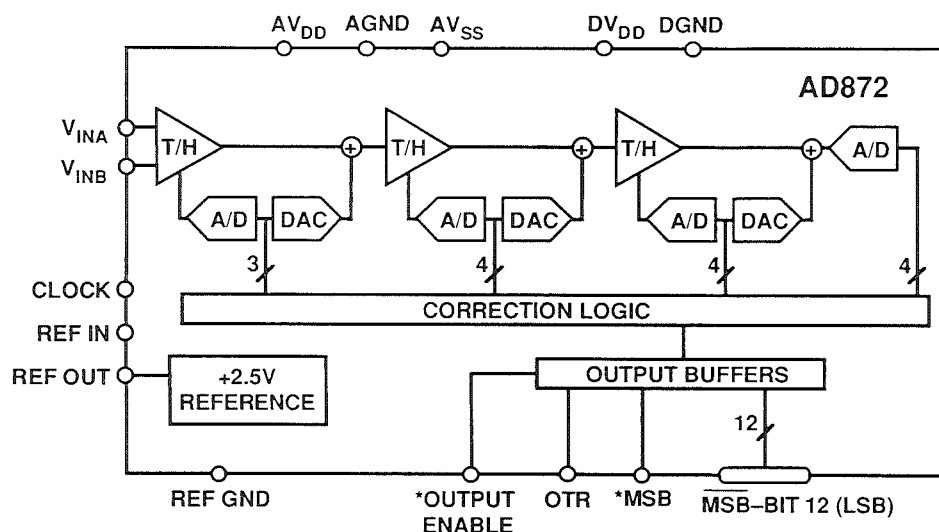
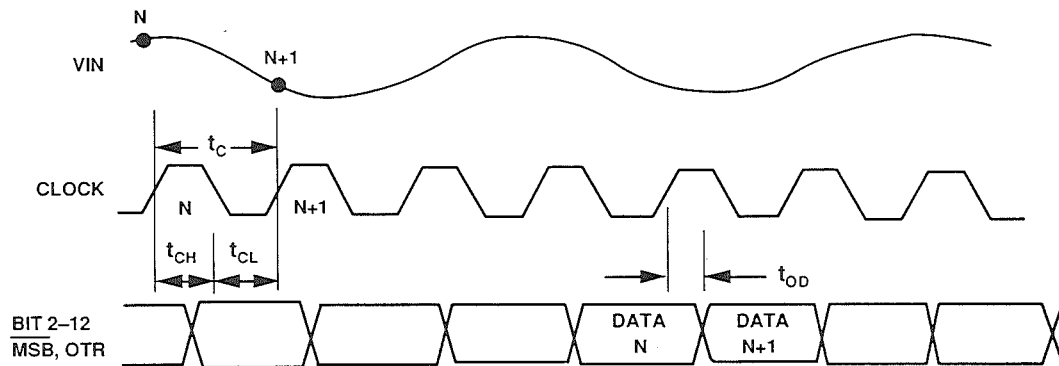


Figure 6.17

In most high speed applications, the output data from the ADC must be downloaded into a buffer memory for further processing. In order to avoid costly high speed, high power memory, the demultiplexing scheme shown in Figure 6.19 may be used to reduce the

data output rate. This will allow low cost CMOS memory to be used for storage of the bulk of the data. High speed flash converters may provide on-chip demultiplexing to ease the demands on the buffer memory interface.

## AD872 TIMING DIAGRAM SHOWS 3 CLOCK-CYCLE LATENCY



**Figure 6.18**

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# DEMULTIPLEXING HIGH SPEED ADC OUTPUTS FOR STORAGE IN SLOWER MEMORIES

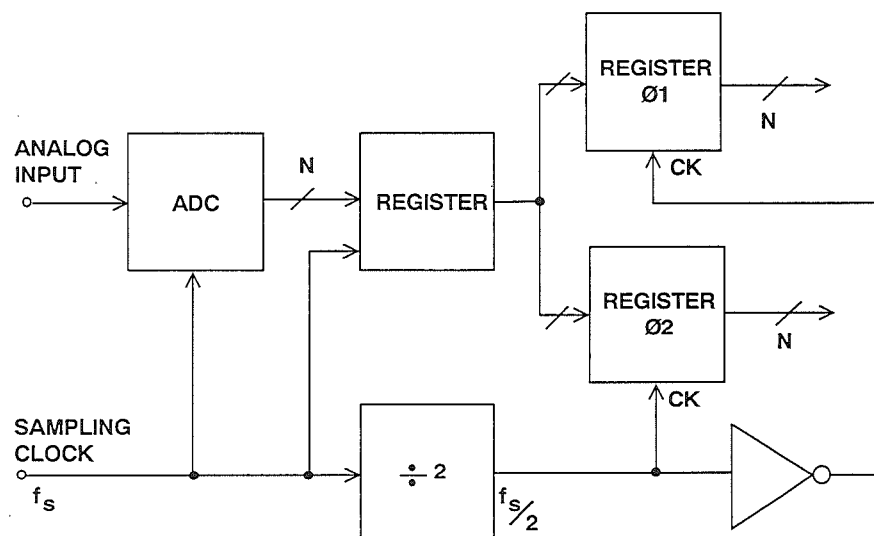


Figure 6.19



## INTERFACING ADC OUTPUTS TO DSPs IN REALTIME SIGNAL PROCESSING APPLICATIONS

Realtime DSP processing of ADC data has become widespread because of faster ADCs and DSPs. The precision sampling ADCs used in these applications will have either parallel data outputs (one pin per bit), or a single serial output data line. The parallel case will be considered first.

Many parallel output sampling ADCs offer three-state outputs which can be enabled or disabled using an *output enable* pin on the IC. While it may be tempting to connect these three-state outputs directly to a backplane data bus, severe performance-degrading noise problems will result. All ADCs have a small amount of internal stray capacitance between the digital outputs and the analog input (typically 0.1 to 0.5pF). Every attempt is made during the design and layout of the ADC to keep this capacitance to a minimum. However, if there is excessive overshoot and ringing and possibly other high frequency noise on the digital output lines (as would probably be the case if the digital outputs were connected directly to a backplane bus) this digital noise will couple back into the analog input through the stray capacitance. The effect of this noise is to decrease the overall ADC SNR and ENOB. Any code-dependent noise will also tend to increase the ADC harmonic distortion.

The best approach to eliminating this potential problem is to provide an intermediate three-state output buffer latch which is located close to the ADC data outputs. This latch serves to isolate the noisy signals on the data bus from the ADC data outputs, thereby

minimizing any coupling back into the ADC analog input.

The ADC data sheet should be consulted regarding exactly how the ADC data should be clocked into the buffer latch. Usually, a signal called *conversion complete*, or *busy* is provided from the ADC for this purpose.

It is also a good idea not to access the data in the intermediate latch during the actual conversion time of the ADC. This practice will further reduce the possibility of corrupting the ADC analog input with noise. The manufacturer's data sheet timing information should indicate the most desirable time to access the output data.

Figure 6.20 shows a simplified parallel interface between the AD676 16 bit, 100kSPS ADC (or the AD7884) and the ADSP-2101 microcomputer. (Note: the actual device pins shown have been relabeled to simplify the following general discussion). In a realtime DSP application (such as in digital filtering) the processor must complete its series of instructions within the ADC sampling interval. Note that the entire cycle is initiated by the sampling clock edge from the sampling clock generator. Even though some DSP chips offer the capability to generate lower frequency clocks from the DSP master clock, the use of these signals as precision sampling clock sources is not recommended due to the probability of timing jitter. It is preferable to generate the ADC sampling clock from a well-designed low noise crystal oscillator circuit as has been previously described.

## GENERALIZED DSP TO ADC PARALLEL INTERFACE

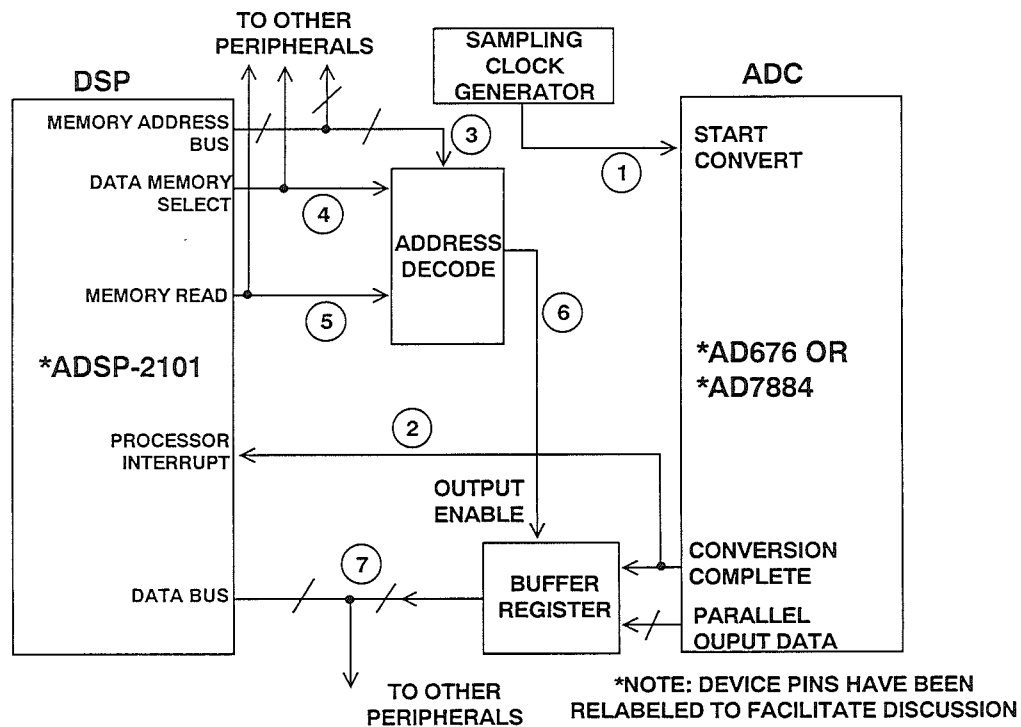


Figure 6.20

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The sampling clock edge initiates the ADC conversion cycle. After the conversion is completed, the ADC *conversion complete* line is asserted which in turn interrupts the DSP. The DSP then places the address of the ADC which generated the interrupt on the *data memory address bus* and asserts the *data memory select* line. The *read* line of the DSP is then asserted. This enables the external three-state ADC buffer register outputs and places the ADC data on the *data bus*. The trailing edge of the *read* pulse latches the ADC data on the *data bus* into the DSP internal registers. At this time, the DSP is free to address other peripherals which may share the common data bus.

Because of the high-speed internal DSP clock (50MHz for the ADSP-2101), the width of the *read* pulse may be too narrow to access properly the data in

the buffer latch. If this is the case, adding the appropriate number of programmable software wait states in the DSP will both increase the width of the *read* pulse and also cause the *data memory address* and the *data memory select* lines to remain asserted for a correspondingly longer period of time. In the case of the ADSP-2101, one wait state is one instruction cycle, or 80ns.

ADCs which have a serial output (such as the AD677, AD776, and AD1879) are interfaced to the serial port of many DSP chips as shown in Figure 6.21. The sampling clock is generated from the low-noise oscillator. The ADC output data is presented on the *serial data* line one bit at a time. The *serial clock* signal from the ADC is used to latch the individual bits into the serial input shift register of the DSP serial port. After all the serial data is transferred into the

serial input register, the serial port logic generates the required processor interrupt signal. The advantages of using serial output ADCs are the reduction in the number of interface connections as well as reduced noise because there are fewer noisy digital PC

tracks close to the converter. In addition, SAR and Sigma-Delta ADCs are inherently serial-output devices. The number of peripheral serial devices permitted is limited by the number of serial ports available on the DSP chip.

## GENERALIZED SERIAL DSP TO ADC INTERFACE

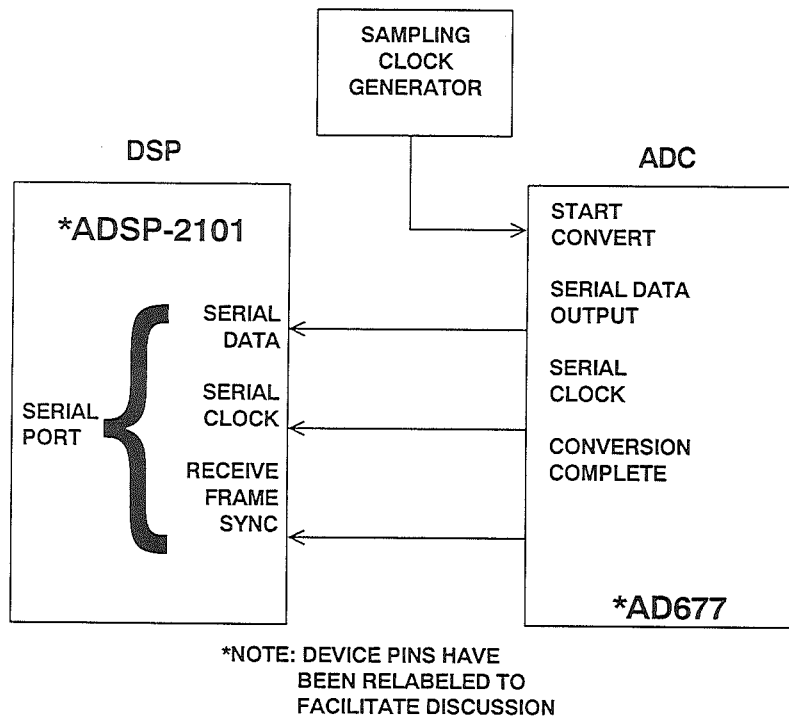


Figure 6.21

## INTERFACING TO DACs

Most of the principles previously discussed regarding interfacing to ADCs also apply to DACs. A generalized block diagram of a parallel input DAC is shown in Figure 6.22. Most high performance DACs have an internal parallel DAC Latch which drives the actual switches. This latch deskews the data so that the output glitch is minimized. Some DACs designed for realtime

sampled-data DSP applications have an additional input latch so that the input data can be loaded asynchronously with respect to the DAC Latch Strobe. Some DACs have an internal reference voltage which can either be used or bypassed with a better external reference. Other DACs require an external reference.

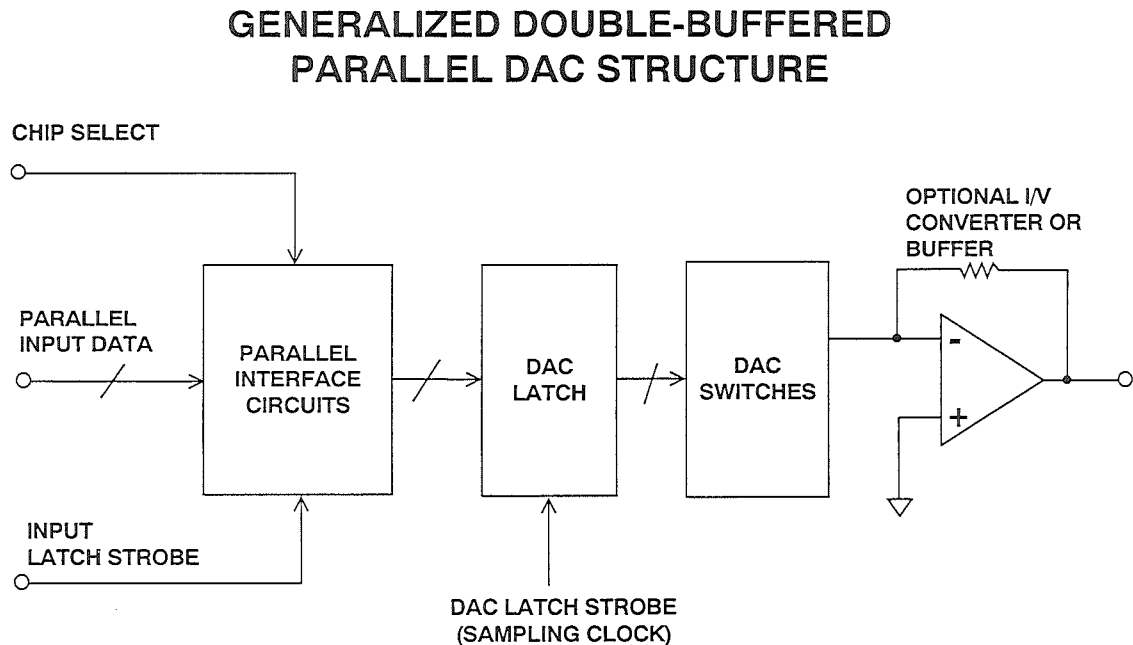


Figure 6.22

The output of a DAC may be a current or a voltage. Fast video DACs are generally designed to supply sufficient output current to develop the required signal levels across resistive loads (generally  $150\Omega$ , corresponding to a  $75\Omega$  source and load-terminated cable). Other DACs are designed to drive a

current into a virtual ground and require a current-to-voltage converter (which may be internal or external). There are some high-impedance voltage-output DACs which require an external buffer in order to drive reasonable values of load impedance.

# INTERFACING DSPs TO DACs

A generalized parallel DSP to DAC interface is shown in Figure 6.23. The operation is similar to the parallel DSP to ADC interface described above. In most DSP applications the DAC is operated continuously from a stable sampling clock generator which is external to the DSP. The DAC requires double-buffering because of the asynchronous interface to the DSP. The sequence of events is as follows. Asserting the *Sampling Clock Generator* line

clocks the word contained in the DAC Input Latch into the DAC Latch (the latch which drives the DAC switches). This causes the DAC output change to the new value. The *Sampling Clock edge* also interrupts the DSP which then *addresses* the DAC, *enables* the DAC *Chip Select*, and *writes* the next data word into the DAC Input Latch using the *Memory Write* and *Data Bus* lines. The DAC is now ready to accept the next Sampling Clock edge.

## GENERALIZED DSP TO DAC PARALLEL INTERFACE

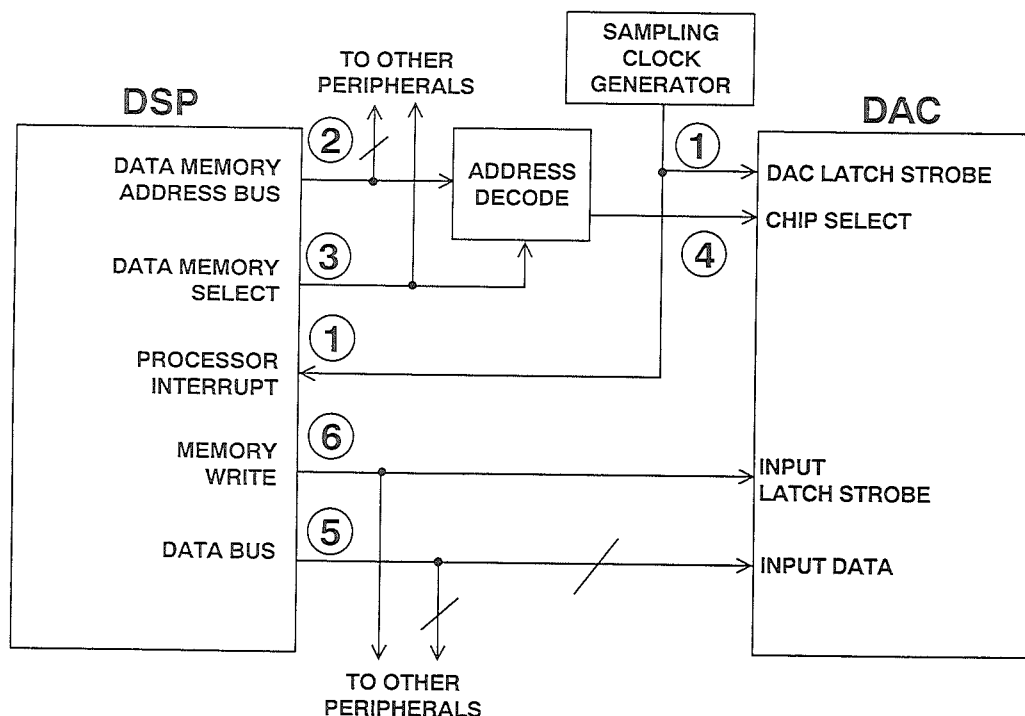


Figure 6.23

A block diagram of a typical serial input DAC is shown in Figure 6.24. The digital input circuitry consists of a serial-to-parallel converter which is driven by a Serial Data line and a Serial Clock. After the serial data is loaded, the DAC Latch Strobe clocks the parallel DAC latch and updates the DAC switches with a new word. Inter-

facing DSPs to serial DACs is quite easy using the DSP serial port (Figure 6.25). The serial data transfer process is initiated by the assertion of the *Sampling Clock Generator* line. This updates the DAC Latch and causes the Serial Port of the DSP to transmit the next word to the DAC using the *Serial Clock* and the *Serial Data* line.

## GENERALIZED SERIAL-INPUT DAC STRUCTURE

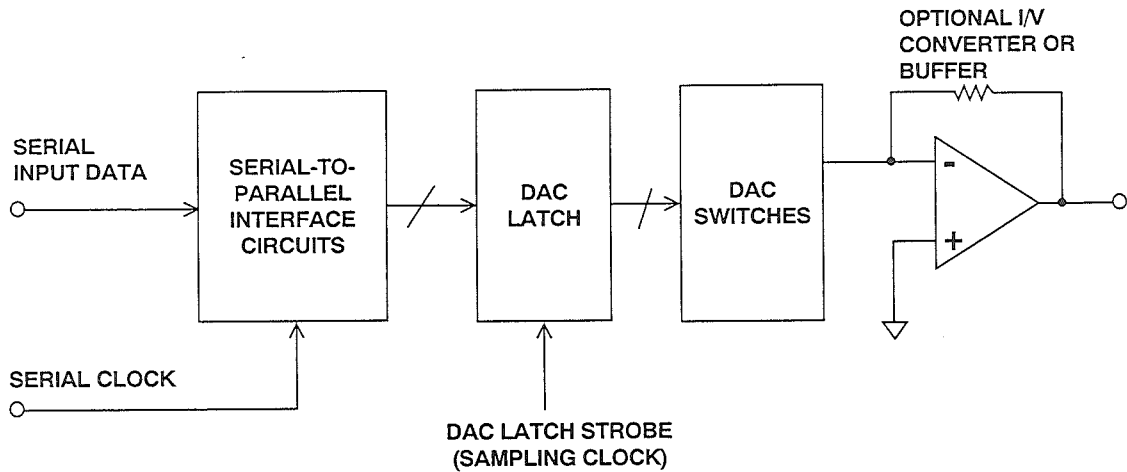


Figure 6.24

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## GENERALIZED DSP TO DAC SERIAL INTERFACE

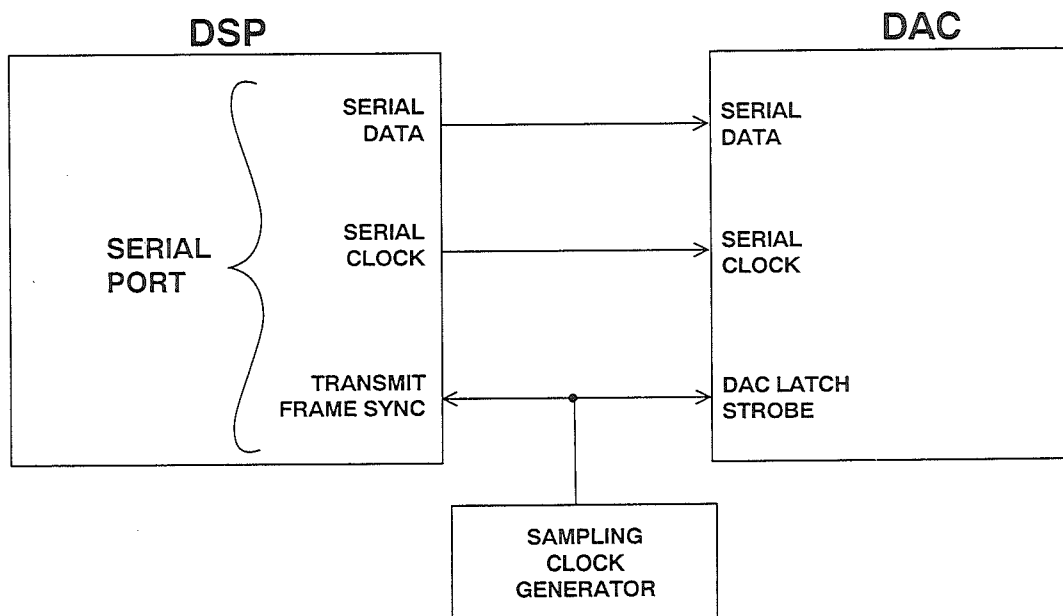


Figure 6.25

## BUFFERING DAC OUTPUTS

Whether or not a DAC output requires additional buffering depends upon its structure. Figure 6.26 shows the case of a voltage-output DAC with an external

buffer for greater drive capability. The op-amp is connected as a simple follower which may provide additional voltage gain if required.

### BUFFERING THE OUTPUT OF A VOLTAGE-OUTPUT DAC

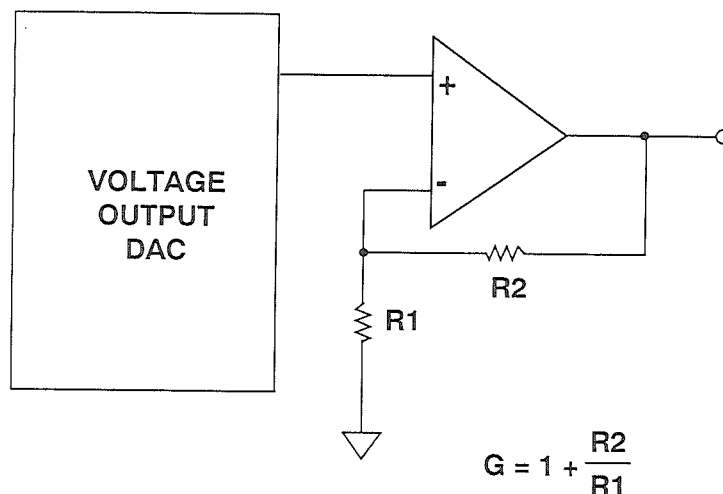


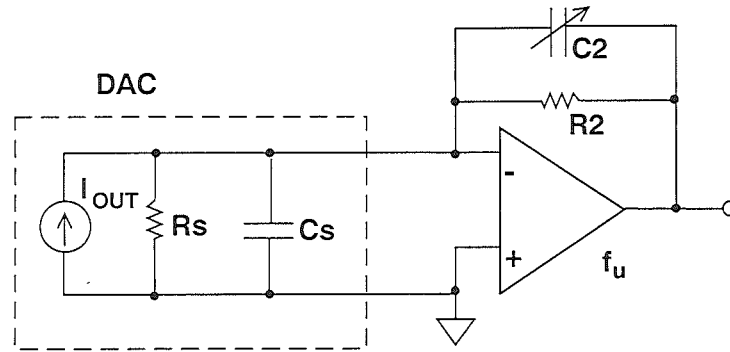
Figure 6.26

A current-output DAC requires a current-to-voltage converter to produce a voltage output. The standard op-amp I/V converter circuit is shown in Figure 6.27. The value of  $R_2$  is chosen to develop the desired voltage for the fullscale DAC output current.  $C_2$  is required to compensate the op-amp because of the additional pole formed by the output capacitance of the DAC,  $C_S$ . The value of  $C_2$  is chosen for best frequency and/or pulse response. If the output resistance of the DAC,  $R_S$ , and

the feedback resistor,  $R_2$ , are of the same order of magnitude, the  $C_2$  should be chosen such that  $R_2 C_2 \approx R_S C_S$ .

If, however,  $R_S \gg R_2$ , then  $C_2$  must be chosen in a different manner. The value of  $C_2$  should be chosen such that the phase margin of the two-pole circuit is between  $45^\circ$  and  $65^\circ$ . The actual value should be chosen in the circuit by adjusting  $C_2$  to provide the best tradeoff between frequency and pulse response.

# BUFFERING THE OUTPUT OF A CURRENT-OUTPUT DAC



- IF  $R_S$  AND  $R_2$  ARE OF THE SAME ORDER OF MAGNITUDE:

$$\text{MAKE } R_2 \cdot C_2 \approx R_S \cdot C_S$$

- IF  $R_S \gg R_2$ , OR LARGE  $C_S$ :

$$\sqrt{\frac{C_S}{2\pi R_2 \cdot f_u}} \leq C_2 \leq 2 \sqrt{\frac{C_S}{2\pi R_2 \cdot f_u}}$$

WHERE  $f_u$  = OP AMP UNITY GAIN BANDWIDTH PRODUCT

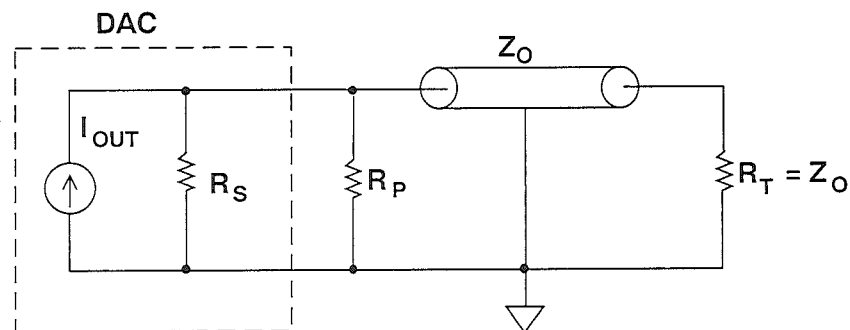
Figure 6.27

Fast, low-glitch DACs such as video-, or DDS DACs often supply a large output current capable of developing sufficient voltage at the output of a source- and load-terminated cable without requiring

additional amplification. A typical configuration is shown in Figure 6.28. In order for the cable to be source-terminated, make  $R_S \parallel R_P = Z_0$ .

6

# TYPICAL VIDEODAC OUTPUTS REQUIRE NO BUFFERING



$$\text{MAKE } \frac{R_S R_P}{R_S + R_P} = Z_0$$

Figure 6.28



## DEGLITCHING DACs USING SHAs

Sample-and-hold circuits can be used to deglitch DACs as shown in Figure 6.29. Just prior to latching new data into the DAC Latch, the SHA is put into the *hold* mode so that the DAC switching glitches are isolated from the output. The transients produced by the SHA

are code-independent, occur at the update frequency, and so are easily filtered. However, modern DACs designed for low glitch and high spectral purity generally achieve the required performance without the requirement for an external SHA.

### DEGLITCHING A DAC OUTPUT USING A SAMPLE-AND-HOLD

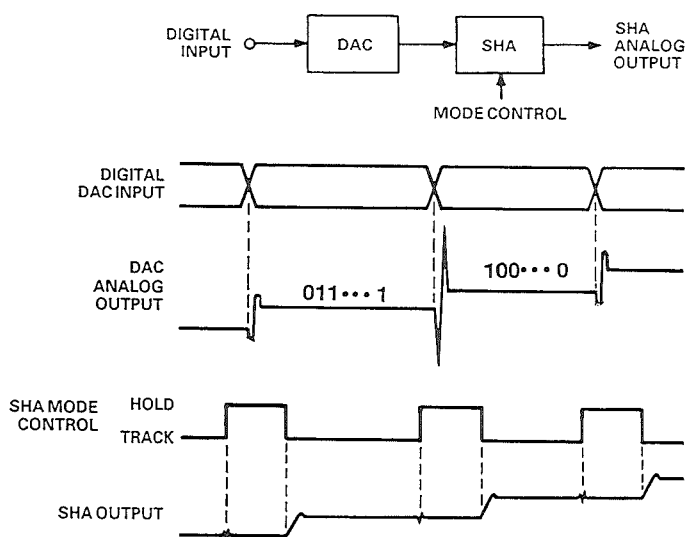


Figure 6.29

Not all sample-and-hold circuits are suitable for this type of application. Some (for example, the AD781) have quite large temperature variable offset

in the sample mode, but are very accurate during the hold mode. Only SHAs with low offset in both sample and hold mode are suitable for deglitching DACs.

## SIN(x)/X FREQUENCY ROLLOFF EFFECT

The output of a reconstruction DAC can be visualized as a series of rectangular pulses whose width is equal to the reciprocal of the update rate (Figure 6.30). The reconstructed signal is down 3.92dB at the Nyquist frequency with

respect to the low frequency amplitude. An inverse  $\sin(x)/x$  filter is sometimes placed after the DAC to correct for this effect and is often incorporated in the anti-aliasing filter.

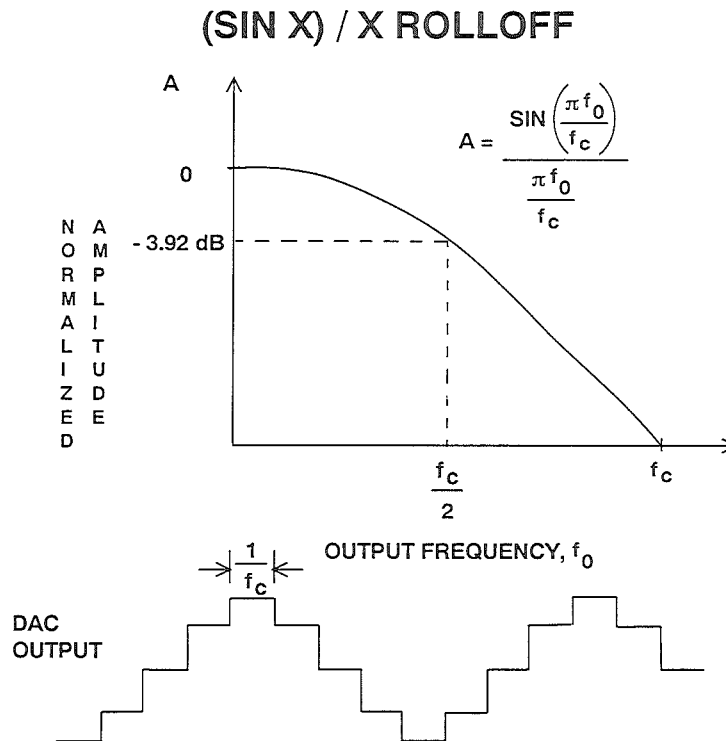


Figure 6.30

## SUPPLYING THE REFERENCE VOLTAGE FOR DACs

Like ADCs, many DACs have an internal reference which may be left unused in favor of a more stable, lower-noise external reference. The same considerations previously discussed for ADCs apply to the selection of a DAC refer-

ence, including the possibility of the DAC being trimmed to its internal reference voltage, so that the use of a high precision external reference actually gives less DAC accuracy.

### REFERENCE VOLTAGES FOR DACs

- DACs may or may not have internal references
- The internal reference (if supplied) is usually not as good as an external one because of process limitations
- An external reference may be substituted for the internal one to achieve higher performance

Figure 6.31

## SAMPLING CLOCK GENERATION FOR ADCs AND DACs

Many users of sampling ADCs and DACs fail to understand the critical nature of the sampling clock signal. The tendency is to focus more on the analog input/output signals and treat the sampling clock as just another digital signal. Unfortunately, noise and jitter on the sampling clock input will cause performance degradation in both ADCs and DACs.

Jitter in an ADC,  $t_a$ , is simply the rms value of the sample-to-sample variation in the precise point in time at which the input signal is sampled. This rms time jitter produces a corresponding rms voltage error which is proportional to the slew rate of the input signal. The effect of broadband time jitter is to degrade the overall SNR of the ADC.

Jitter for an ADC is usually attributed to the SHA. The ADC aperture jitter,

unfortunately, is certainly not the only possible source for this error. In a practical ADC, the sampling clock is often phase and amplitude modulated by some unwanted external sources; the sources can be wideband random noise, oscillator phase noise, power line noise, or digital noise due to poor layout, bypassing, and grounding techniques. Phase jitter on the sampling clock produces the same effect as jitter on the input sinewave.

The effects of even small amounts of timing jitter are shown in Figure 6.32, where SNR and ENOB are plotted as a function of fullscale input sinewave frequency for various amounts of rms timing jitter using the formula shown. For example, in order to achieve 12 bit SNR (74dB) on a 10MHz fullscale input sinewave, the rms jitter can be no more than 3ps rms.

### EFFECTS OF APERTURE JITTER ON SNR AND ENOB

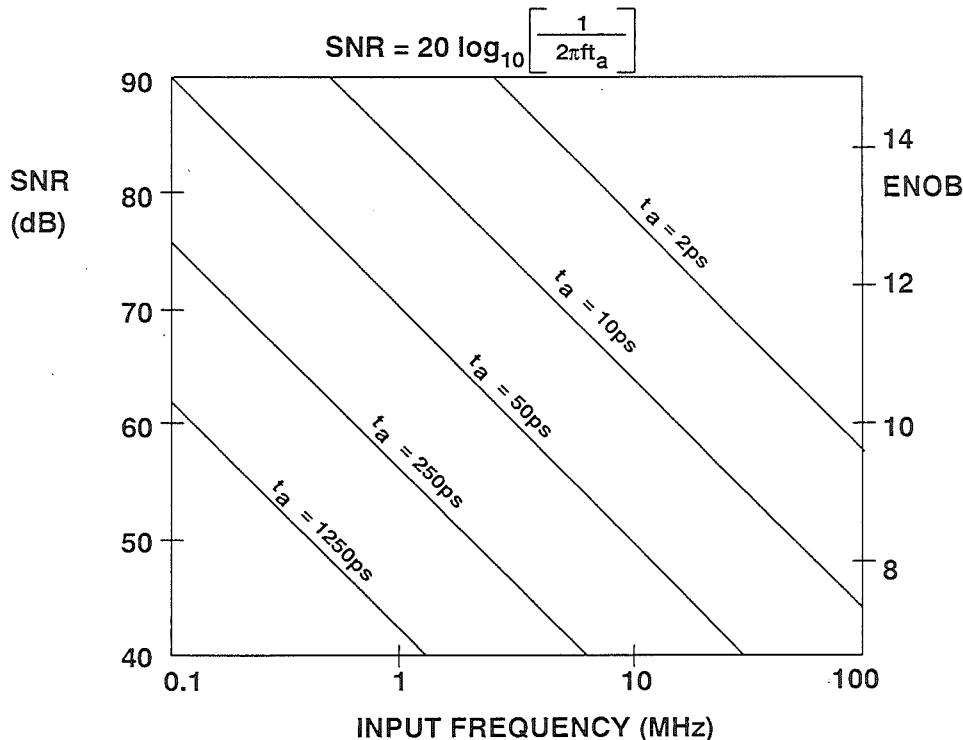


Figure 6.32

The total rms timing jitter will probably consist of two frequency components: narrowband and broadband. The sampling clock oscillator will probably have narrowband phase noise. The effect of narrow-band phase noise centered about the sampling frequency is to produce similar phase noise about the fundamental sinusoid frequency in an FFT of the digitized sinusoid. The high-speed logic circuits in the sampling clock path may introduce broadband noise on the pulse edges which in turn causes broadband jitter due to sample-to-sample variations in the precise times at which the internal logic thresholds are crossed. ECL logic gates have an effective bandwidth greater than 300MHz, and a typical 100K ECL gate has an effective rms timing jitter of approximately 7ps rms.

A detailed mathematical analysis of broadband and narrowband timing jitter is much beyond the scope of this discussion, however their effects may be observed directly in the FFT analysis of a sinusoid. The narrowband phase noise will show up as a widening of the main lobe of the fundamental sinusoid, while the broadband jitter will cause an overall increase in the noise floor.

The sampling clock generator must have low phase noise, therefore RC and relaxation oscillators should be ruled out completely. A crystal oscillator is much preferred. The crystal oscillator should not be constructed out of logic gates, capacitors, and resistors, however, but should be built around discrete bipolar and FET devices in the

circuits recommended by the crystal manufacturer. In exacting applications, additional filtering may be required (Figure 6.33). The bandpass filter following the crystal oscillator serves to remove any frequency skirts around the sampling frequency. The lowpass filter then removes any harmonics of the sampling clock frequency which may not have adequately been attenuated by the bandpass filter. The output then drives a low-jitter wideband comparator which converts the sinewave into a digital signal. Use a TTL comparator such as the AD9696 if the ADC requires TTL inputs, or an ECL comparator such as the AD96685 if ECL inputs are required.

The sampling clock circuits themselves should be isolated as much as possible from the noise present in the digital portions of the system. Separate decoupled power supplies may also be required for optimum results. It is extremely important that the digital outputs of the ADC (and digital inputs to a DAC) not be allowed to couple into the sampling clock signal. Coupling will cause an increase in the harmonic distortion of due to signal-dependent digital transients coupling into the sampling clock. On the other hand, the sampling clock is itself a digital signal. It has the potential for causing noise in the analog portion of the system. It should therefore be isolated from both the analog and digital portions of the system. As we will see in the next section, the sampling clock generator circuits should be referenced and decoupled to the analog ground plane.

## GENERATING PRECISION LOW-JITTER SAMPLING CLOCKS

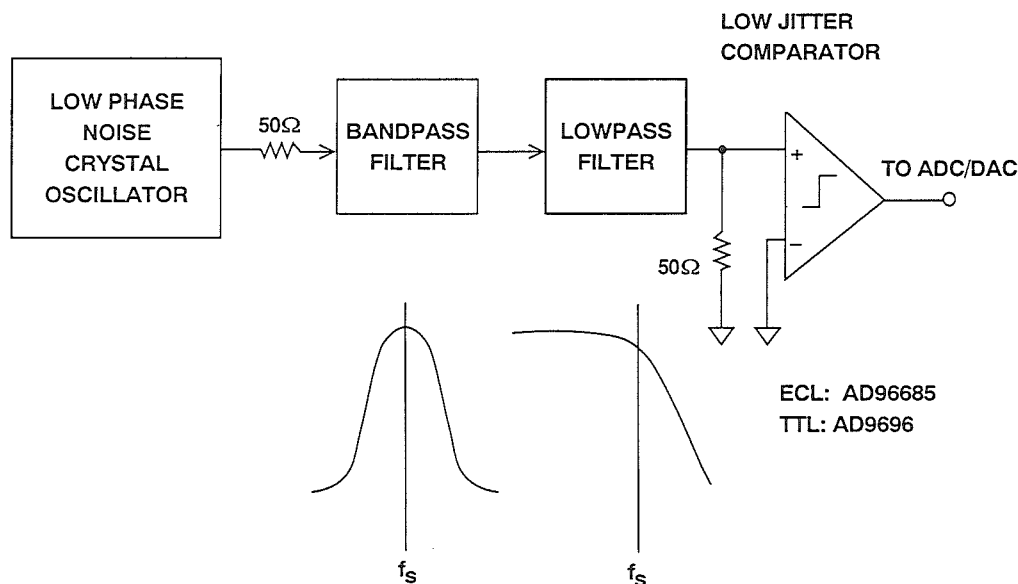


Figure 6.33

## POWER SUPPLIES, GROUND PLANES, DECOUPLING, AND LAYOUT

The switching-mode power supply offers low cost, small size, high efficiency, high reliability and the possibility of operating from a wide range of input voltages without adjustment. Unfortunately, these supplies produce noise over a broad band of frequencies, and this noise occurs as conducted noise, radiated noise, and unwanted electric and magnetic fields. When used to supply logic circuits, even more noise is generated on the power supply bus. The noise transients on the output lines of switching supplies are short-duration voltage spikes. Although the actual switching frequencies may range from 10 to 100kHz, these spikes can contain frequency components that extend into the hundreds of megahertz.

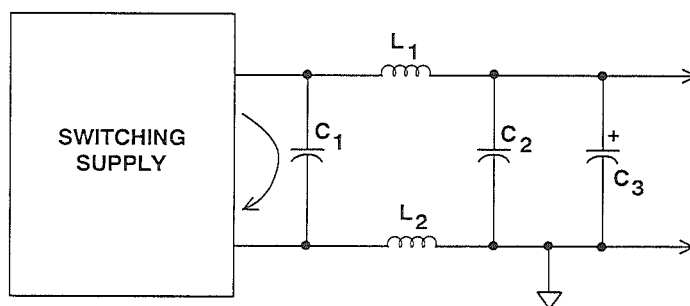
Because of the wide variations in the noise characteristics of commercially available switching supplies, they should always be purchased in accordance with a specification-control drawing. Although specifying switching supplies in terms of rms noise is common practice, you should also specify the peak amplitudes of the switching spikes under the output loading conditions you expect in your system. You should also insist that the switching-supply manufacturer inform you of any internal supply design changes that may alter the spike amplitudes, duration, or switching frequency. These changes may require corresponding changes in the external power-supply filtering networks.

## SWITCHING-MODE POWER SUPPLIES

- Generate Conducted and Radiated Noise as Well as Electric and Magnetic Fields (HF and LF)
- Outputs Must be Adequately Filtered if Powering Sensitive Analog Circuits
- Optimum Filter Design Depends on Power Supply Characteristics. Beware of Power Supply Design Changes.
- Use Faraday Shields to Reduce HF Electric and HF Magnetic Fields
- Physically Isolate Supply from Analog Circuits
- Temporarily Replace Switching Supply with Low-Noise Linear Supply or Battery when Suspicious of Switching Supply Noise

Figure 6.34

## FILTERING A SWITCHING SUPPLY OUTPUT



- $C_1$  MUST HAVE LOW INDUCTANCE AND BE CLOSE TO THE SUPPLY TO MINIMIZE HF CURRENT LOOPS AND RESULTANT HF MAGNETIC FIELDS
- $C_2$  IS ALSO LOW INDUCTANCE,  $C_3$  IS ELECTROLYTIC
- IF THE SWITCHING SUPPLY IS INTERNALLY GROUNDED,  $L_2$  SHOULD BE OMITTED

Figure 6.35

Filtering switching supply outputs that provide several amps and generate voltage spikes having high frequency components is a challenge. For this reason, you should place the initial filtering burden on the switching supply manufacturer. Even so, external filtering such as shown in Figure 6.35 should be added. The series inductors isolate both the output and common lines from the external circuits. Because the load currents may be large, make sure that the inductors selected do not saturate. Split-core inductors or large ferrite beads make a good choice. Because the switching power supplies generate high and low frequency electric and magnetic fields, they should be physically separated as far as possible from critical analog circuitry. This is especially important in preventing the inductive coupling of low frequency magnetic fields.

Proper power supply decoupling techniques must be used on each PC board

in the system. Figure 6.36 shows an arrangement which will ensure minimum problems. The power supply input (usually brought into the PC board on multiple pins) is first decoupled to the large-area low-impedance ground plane with a good quality, low ESL and low ESR tantalum electrolytic capacitor. This capacitor bypasses low frequency noise to the ground plane. The ferrite bead reduces high frequency noise to the rest of the circuit. You should then place one low-inductance ceramic capacitor at each power pin on each IC. Ideally, you should use surface-mount chip capacitors for minimum inductance, but if you use leaded ceramics, be sure to minimize the lead lengths by mounting them flush on the PC board. Some ICs may require an additional small tantalum electrolytic capacitor (usually between 1 and  $5\mu\text{F}$ ). The data sheets for each IC should provide appropriate recommendations, but when in doubt, put them in!

6

### PROPER POWER SUPPLY DECOUPLING AT EACH IC ON THE PC BOARD IS CRITICAL TO ACHIEVING GOOD HIGH SPEED SYSTEM PERFORMANCE

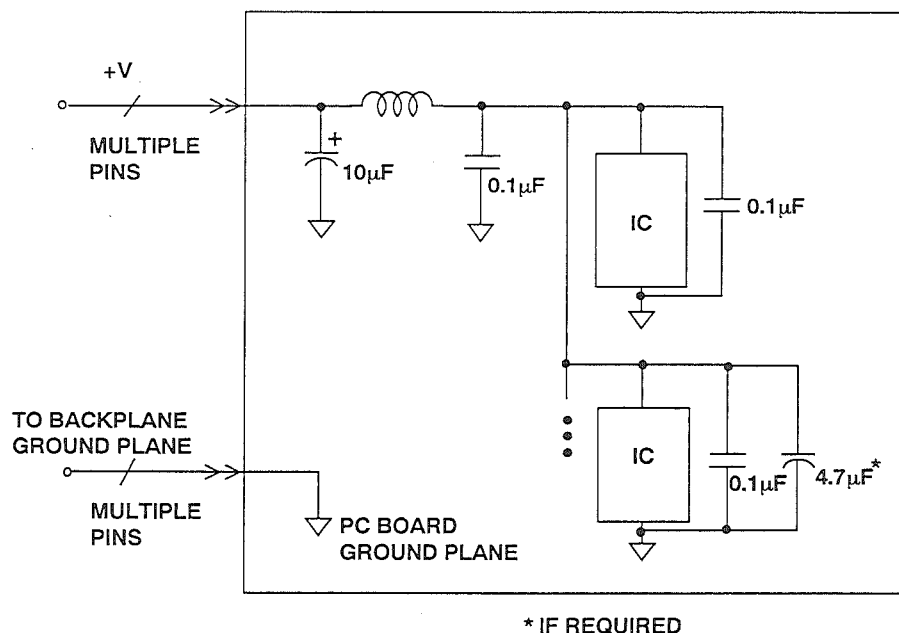


Figure 6.36



If a double-sided PC board is used, one side should be dedicated entirely (at least 75% of the total area) to the ground plane. The ICs are mounted on this side, and connections are made on the opposite side. Because of component interconnections, however, a few breaks in the ground plane are usually unavoidable. As more and more of the ground plane is eaten away for interconnections, its effectiveness diminishes. It is therefore recommended that multilayer PC boards be used where component packing density is high. Dedicate at least one entire layer to the ground plane.

When connecting to the backplane, use a number of pins (30 to 40%) on each PC board connector for ground. This will ensure that the low impedance ground plane is maintained between the various PC boards in a multiscard system.

In practically all high speed systems, it is highly desirable to physically separate sensitive analog components from noisy digital components. It is usually a good idea to also establish separate analog and digital ground planes on each PC board as shown in Figure 6.37. The separate analog and digital ground planes are continued on the backplane using either motherboard ground planes or "ground screens" which are made up of a series of wired interconnections between the connector ground pins. The ground planes are joined together at the system *star ground*, or *single-point ground*, usually located at the common return point for the power supplies. The Schottky diodes are inserted to prevent accidental dc voltages from developing between the two ground systems.

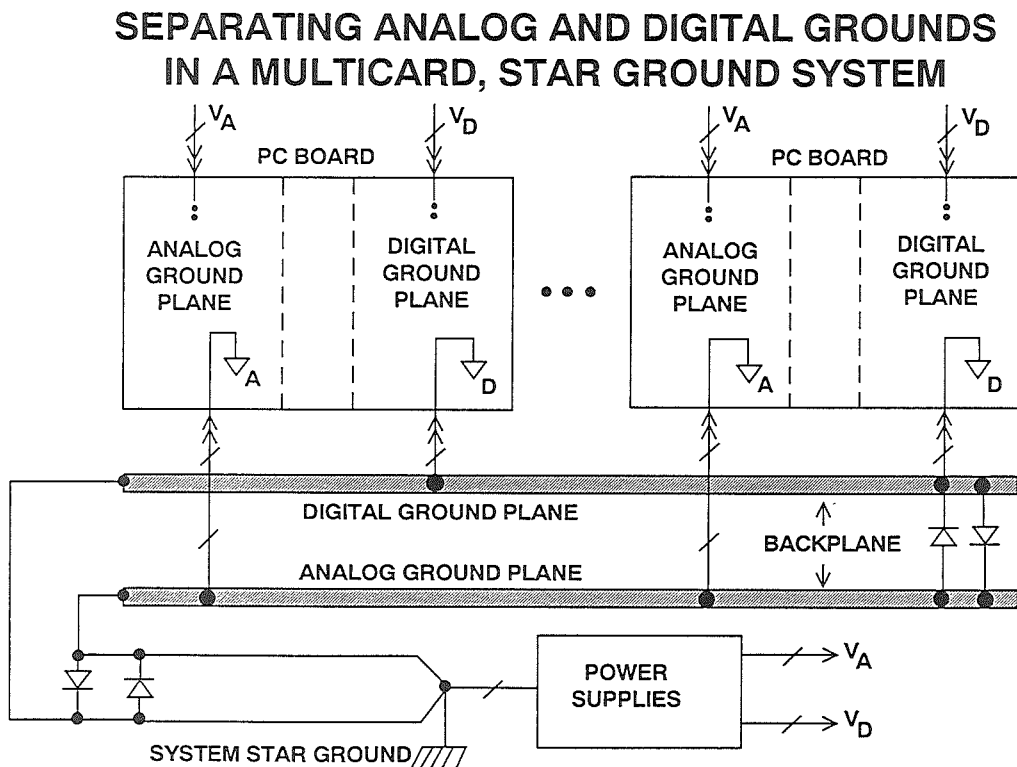


Figure 6.37

Sensitive analog components such as amplifiers and voltage references are referenced and decoupled to the analog ground plane. *The ADCs and DACs (and even some mixed-signal ICs) should be treated as analog circuits and also grounded and decoupled to the analog ground plane.* At first glance,

this may seem somewhat contradictory, since a converter has an analog and digital interface and usually pins designated as analog ground (AGND) and digital ground (DGND). The diagram shown in Figure 6.38 will help to explain this seeming dilemma.

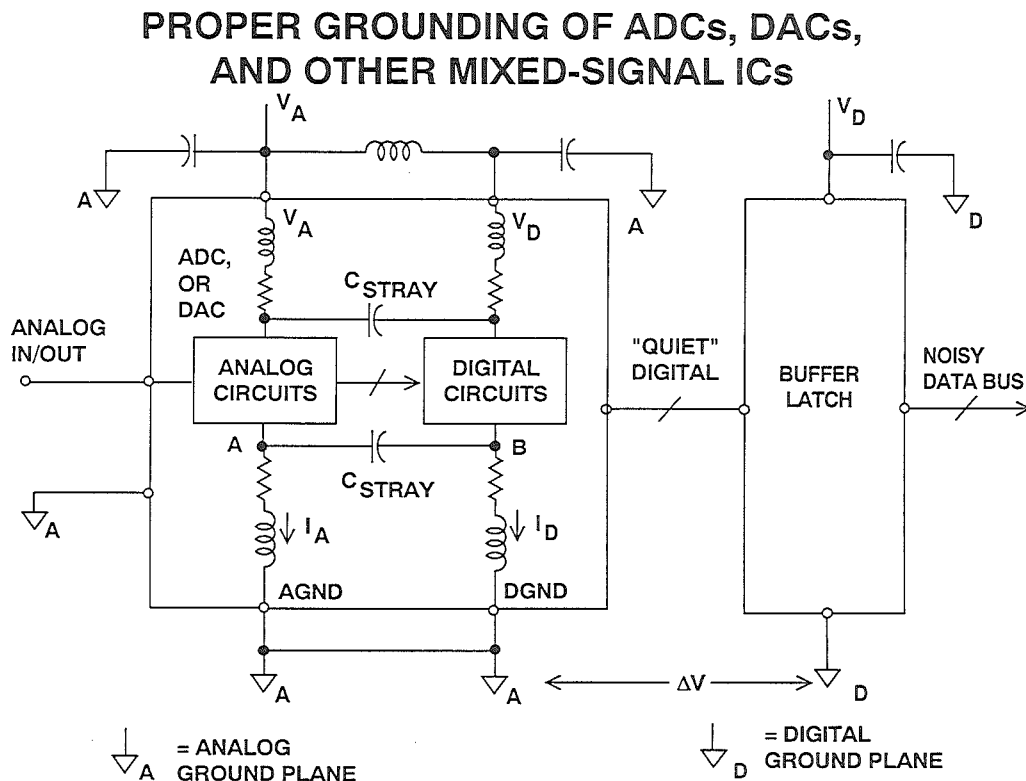


Figure 6.38

Inside an IC that has both analog and digital circuits, such as an ADC or a DAC, the grounds are usually kept separate to avoid coupling digital signals into the analog circuits. Figure 6.38 shows a simple model of a converter. There is nothing the IC designer can do about the wirebond inductance and resistance associated with connect-

ing the pads on the chip to the package pins except to realize it's there. The rapidly changing digital currents produce a voltage at point B which will inevitably couple into point A of the analog circuits through the stray capacitance,  $C_{STRAY}$ . In addition, there is approximately 0.2pF unavoidable stray capacitance between every pin of

the IC package! It's the IC designer's job to make the chip work in spite of this. However, in order to prevent further coupling, the AGND and DGND pins should be joined together externally to the *analog* ground plane with minimum lead lengths. Any extra impedance in the DGND connection will cause more digital noise to be developed at point B; it will, in turn, couple more digital noise into the analog circuit through the stray capacitance.

The name "DGND" on an IC tells us that this pin connects to the digital ground of the IC. It does not say that this pin must be connected to the digital ground of the system.

It is true that this arrangement will inject a small amount of digital noise on the analog ground plane. These currents should be quite small, and can be minimized by ensuring that the converter input/or output does not drive a large fanout. Minimizing the fanout on the converter's digital port will also keep the converter logic transitions relatively free from ringing, and thereby minimize any potential coupling into the analog port of the converter. The logic supply pin ( $V_D$ ) can be further isolated from the analog supply by the insertion of a small ferrite bead as shown in Figure 6.38. The internal digital currents of the converter will return to ground through the  $V_D$  pin decoupling capacitor (mounted as close to the converter as possible) and will not appear in the external ground circuit. It is always a good idea (as shown in Figure 6.38) to place a buffer latch adjacent to the converter to isolate the converter's digital lines from any noise which may be on the data bus. Even though a few high speed converters have three-state outputs/inputs, this isolation latch represents good design practice.

The buffer latch and other digital circuits should be grounded and decoupled to the digital ground plane of the PC board. Notice that any noise between the analog and digital ground plane reduces the noise margin at the converter digital interface. Since digital noise immunity is of the orders of hundreds or thousands of millivolts, this is unlikely to matter.

The sampling clock generation circuitry should also be grounded and heavily-decoupled to the analog ground plane. As previously discussed, phase noise on the sampling clock produces degradation in system SNR.

Separate power supplies for analog and digital circuits are also highly desirable. The analog supply should be used to power the converter. If the converter has a pin designated as a digital supply pin ( $V_D$ ), it should either be powered from a separate analog supply, or filtered as shown in the diagram. All converter power pins should be decoupled to the analog ground plane, and all logic circuit power pins should be decoupled to the digital ground plane. If the digital power supply is relatively quiet, it may be possible to use it to supply analog circuits as well, but be very cautious.

A clean, analog-grade supply can be generated from a 5V logic supply using a differential LC filter with separate power supply and return lines as shown in Figure 6.40. The supply output is virtually free of any glitch noise as evident in the scope photo shown in Figure 6.41, which compares the input and output sides of the filter. All capacitors were selected from commonly available types. Lower noise can be attained using low ESR (Equivalent Series Resistance) type electrolytic and tantalum capacitors. The circuit as

shown can handle 100mA of load current without the risk of saturating the

ferrite core. Higher current capacity can be achieved using larger ferrite cores.

## POWER SUPPLY, GROUNDING, AND DECOUPLING POINTS

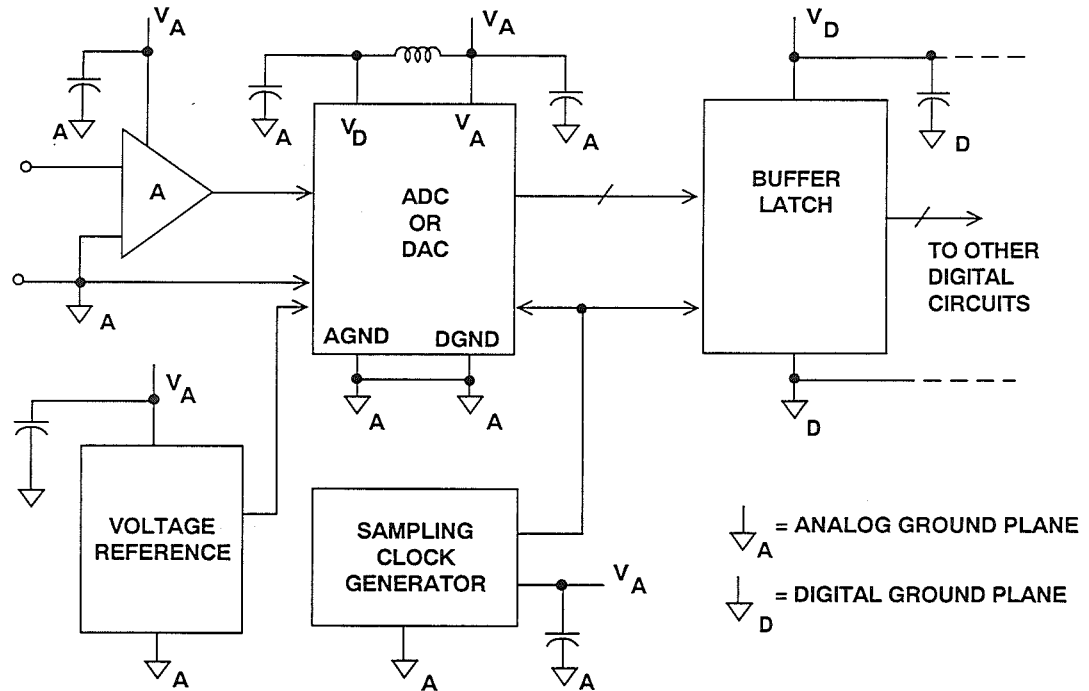


Figure 6.39

## DIFFERENTIAL LC FILTER TURNS NOISY LOGIC SUPPLIES INTO NOISE-FREE ANALOG SUPPLIES

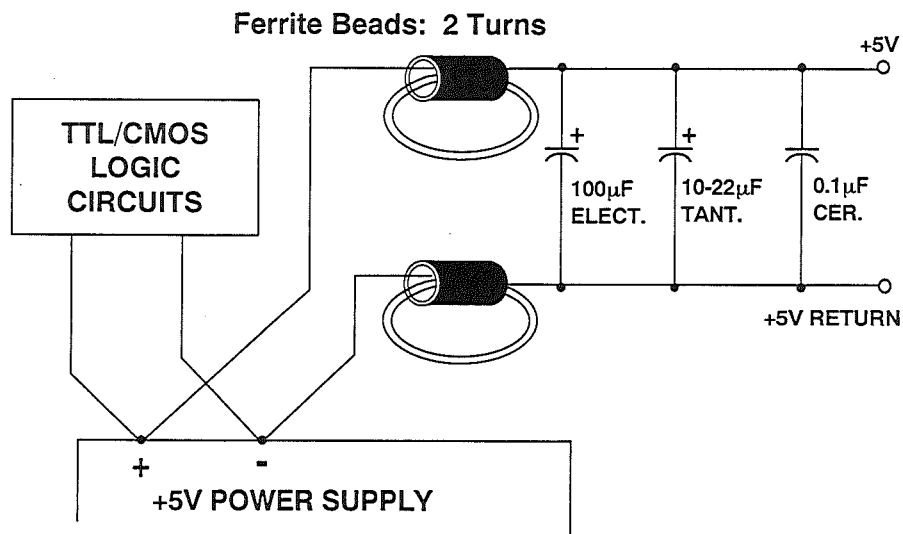


Figure 6.40

## LC FILTER VIRTUALLY ELIMINATES ALL GLITCH NOISE

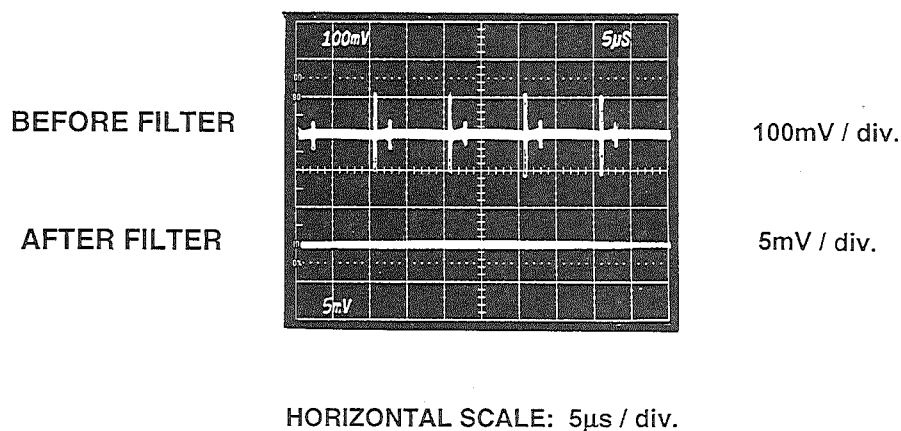


Figure 6.41

## SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC/DAC analog runs.
- Use lots of ground plane.
- Use microstrip techniques at high frequencies for controlled impedances and controlled return current paths.
- Use surface mount components in high frequency systems to minimize parasitic capacitance and inductance.

Figure 6.42

If a ground plane is used, as it should in most cases, it can act as a shield where sensitive signals cross. Figure 6.43 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other and signal paths are kept as short as possible. While real life is rarely as tidy as this the principle remains a valid one.

## EDGE CONNECTIONS

- Separate sensitive signal by ground pins.
- Keep down ground impedances with multiple (30-40% of total) ground pins.
- Have several pins for each power line.
- Critical signals such as analog or sampling clocks may require a separate connector (possibly coax), or microstrip techniques.

Figure 6.44

Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older the contact resistance is likely to rise, and the board's performance may be compro-

mised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 30-40% of all the pins on the PCB connector should be ground pins). For similar reasons there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

## SOCKETS

It is tempting to mount expensive ICs in sockets rather than soldering them in circuit - especially during circuit devel-

opment. Engineers would do well not to succumb to this temptation.

### USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

- DON'T! (If at all possible)
- Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).
- Always test the effect of sockets by comparing system performance with and without the use of sockets.
- Do not change the type of socket or manufacturer used without evaluating the effects of the change on performance.

6

Figure 6.45

Sockets add resistance, inductance and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon to ensure the performance of high performance (high speed or high precision or, worst of all, both) devices. As the socket ages and

the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used the best performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and mixed signal circuits. If their use can be



avoided it should be. However at medium speeds and medium resolutions the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit be-

haves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

## PROTOTYPING HIGH PERFORMANCE ANALOG CIRCUITRY

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits. Prototyping techniques derived from the “node” theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. This approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multichip system.

6

## PROTOTYPING MIXED SIGNAL CIRCUITRY

- NEVER use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).
- Wherever possible avoid the use of sockets for analog ICs.
- Use a prototype of your final PCB layout as early as possible.

Figure 6.46

In this case components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient this is not essential), with ground connections made to the plane

and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5 mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in Reference 1 at the end of this section.

Manufacturer's evaluation boards are also useful in system prototyping since they have already been optimized for best performance. Analog Devices offers many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

## ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 6.47

## REFERENCES

1. Wainwright Instruments, Inc., 7770 Regents Rd., #113, Suite 371, San Diego, CA 92122, Tel. 619-558-1057. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. Tel: +49-8152-3162, Fax: +49-8152-5174.
2. Ralph Morrison, **Grounding and Shielding Techniques in Instrumentation, Third Edition**, John Wiley, Inc., 1986.
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7. Walt Kester, *Basic Characteristics Distinguish Sampling A/D Converters*, **EDN**, September 3, 1992, pp.135-144.
8. Walt Kester, *Peripheral Circuits Can Make or Break Sampling ADC System*, **EDN**, October 1, 1992, pp. 97-105.
9. Walt Kester, *Layout, Grounding, and Filtering Complete Sampling ADC System*, **EDN**, October 15, 1992, pp. 127-134.



## SECTION 7

### DATA ACQUISITION SYSTEM FUNDAMENTALS

- Data Acquisition System Configurations
- Multiplexing
- Filtering Considerations in Data Acquisition Systems
- SHA and ADC Settling Time Requirements in Multiplexed Applications
- Complete Data Acquisition Systems on a Chip
- Multiplexing Inputs to Sigma-Delta ADCs
- Simultaneous Sampling Systems
- Data Distribution Systems using DACs



## SECTION 7

# DATA ACQUISITION SYSTEM FUNDAMENTALS

*Walt Kester*

### DATA ACQUISITION SYSTEM CONFIGURATIONS

There are many applications for data acquisition systems in measurement and process control. All data acquisition applications involve digitizing analog signals for analysis using ADCs. In a measurement application, the ADC is followed by a digital processor which performs the required data analysis. In a process control application, the process controller generates feedback signals which typically must be converted back into analog form using a DAC.

Although a single ADC digitizing a single channel of analog data constitutes a data acquisition system, the term *data acquisition* generally refers to

multi-channel systems. If there is feedback from the digital processor, DACs may be required to convert the digital responses into analog. This process is often referred to as *data distribution*.

Figure 7.1 shows a data acquisition/distribution process control system where each channel has its own dedicated ADC and DAC. An alternative configuration is shown in Figure 7.2, where analog multiplexers and demultiplexers are used with a single ADC and DAC. In most cases, especially where there are many channels, this configuration provides an economical alternative.



## DATA ACQUISITION SYSTEM USING ADC/DAC PER CHANNEL

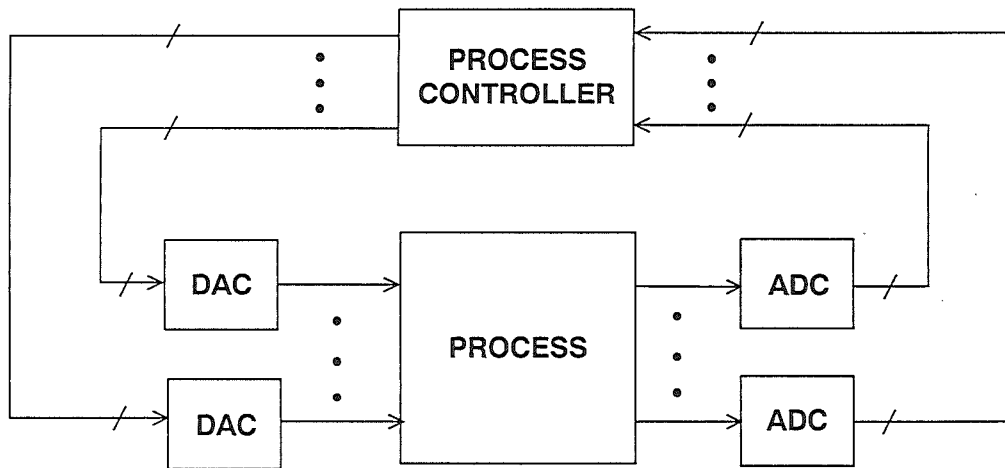


Figure 7.1

## DATA ACQUISITION SYSTEM USING ANALOG MULTIPLEXING/DEMULTIPLEXING AND SINGLE ADC/DAC

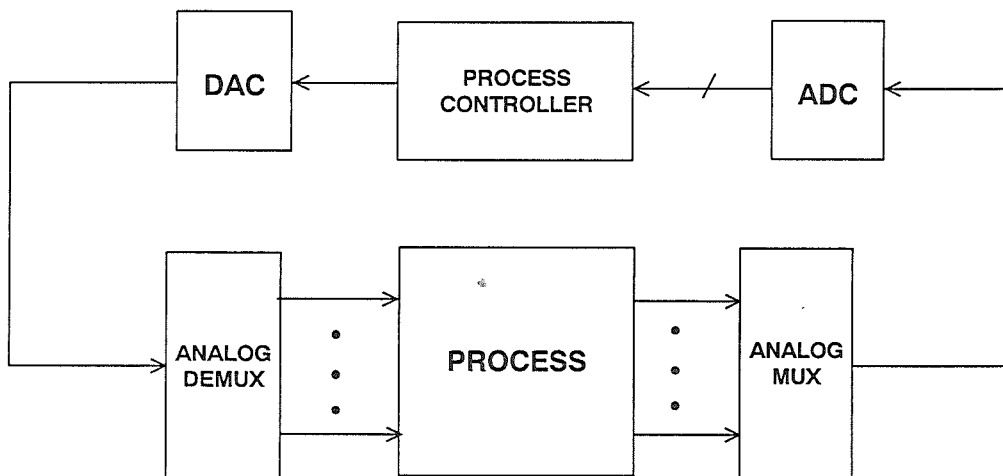


Figure 7.2

There are many tradeoffs involved in designing a data acquisition system. Issues such as filtering, amplification,

multiplexing, demultiplexing, sampling frequency, and partitioning must be resolved.

## MULTIPLEXING

Multiplexing is a fundamental part of a data acquisition system. Multiplexers and switches are examined in more detail in Section 8, but a fundamental understanding is required to design a data acquisition system. A simplified diagram of an analog multiplexer is shown in Figure 7.3. The number of input channels typically ranges from 4 to 16, and the devices are generally fabricated on CMOS processes. The key specifications are *switching time*, *on-resistance*, *on-resistance modulation*,

and *off-channel isolation (crosstalk)*.

Multiplexer switching time ranges from about 50ns to over 1 $\mu$ s, on-resistance from 25 to several hundred ohms, and off-channel isolation from 50 to 90dB. Some multiplexers have internal channel-address decoding logic and registers, while with others, these functions must be performed externally. Unused multiplexer inputs *must* be grounded or severe loss of system accuracy may result.

### SIMPLIFIED DIAGRAM OF A TYPICAL ANALOG MULTIPLEXER

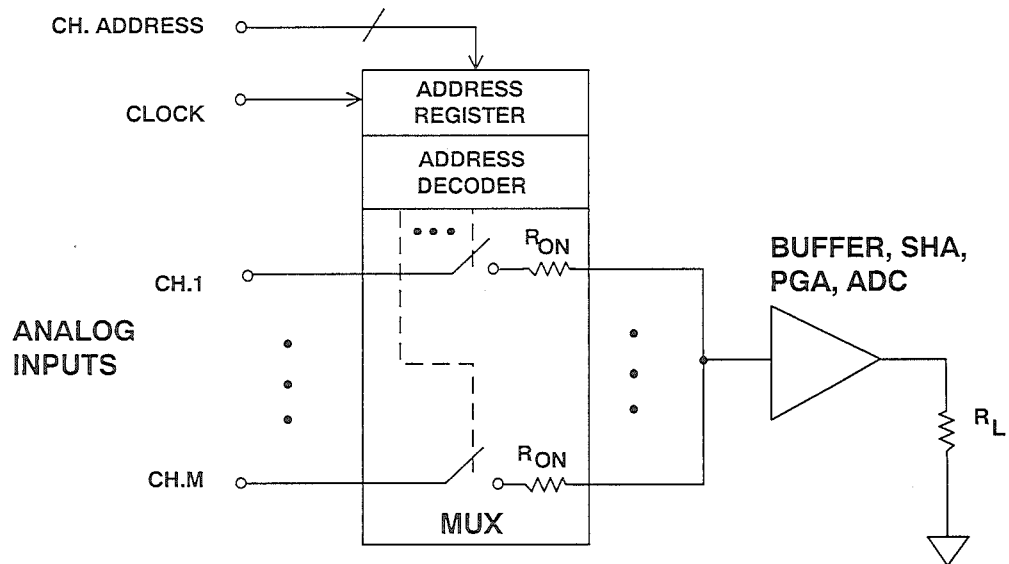


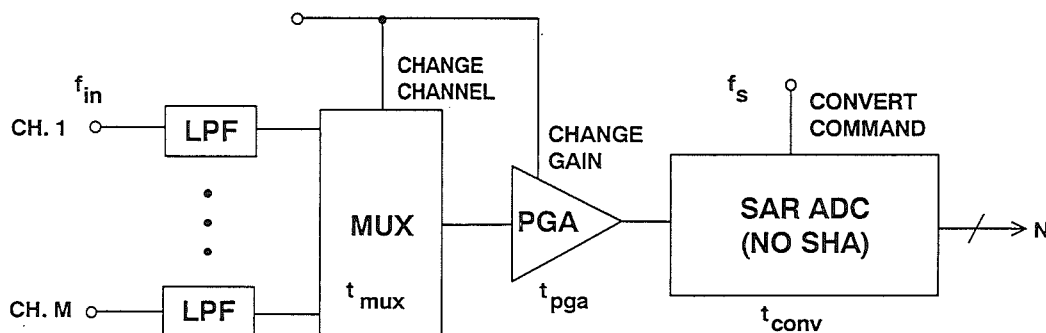
Figure 7.3

Multiplexer on-resistance is generally slightly dependent on the signal level (often called  $R_{on}$  modulation). This will cause signal distortion if the multiplexer must drive a load resistance, therefore the multiplexer output should therefore be isolated from the load with a suitable buffer amplifier. A separate buffer is not required if the multiplexer drives a high input impedance, such as a PGA, SHA or ADC - but beware! Some SHAs and ADCs draw high frequency pulse current at their sampling rate and cannot tolerate being driven by an unbuffered multiplexer.

An M-channel multiplexed data acquisition system is shown in Figure 7.4. The

multiplexer output drives a PGA whose gain can be adjusted on a per-channel basis depending on the channel signal level. This ensures that all channels utilize the full dynamic range of the ADC. The PGA gain is changed at the same time as the multiplexer is switched to a new channel. The ADC *Convert Command* is applied after the multiplexer and the PGA have settled to the required accuracy (1LSB). The maximum sampling frequency (when switching between channels) is limited by the multiplexer switching time  $t_{mux}$ , the PGA settling time  $t_{pga}$ , and the ADC conversion time  $t_{conv}$  as shown in the formula.

### MULTIPLEXED DATA ACQUISITION SYSTEM WITH PGA AND SAR ADC



$$\blacksquare \quad f_s \leq \frac{1}{t_{conv} + \sqrt{t_{mux}^2 + t_{pga}^2}}$$

$$\blacksquare \quad f_{in} \leq \frac{1}{\pi \cdot 2^N \cdot t_{conv}}$$

■ Example: If  $N = 12$  and  $t_{conv} = 20\mu\text{sec}$ ,

Then  $f_{in} \leq 4\text{Hz}!!!!$

Figure 7.4

In a multiplexed system it is possible to have a positive fullscale signal on one channel and a negative fullscale signal on the other. When the multiplexer switches between these channels its output is a fullscale step voltage. All elements in the signal path must settle to the required accuracy (1LSB) before the conversion is made. The effect of inadequate settling is dc crosstalk between channels.

The SAR ADC chosen in this application has no internal SHA (similar to the industry-standard AD574-series), and therefore the input signal must be held constant (within 1LSB) during the conversion time in order to prevent encoding errors. This defines the maximum rate-of-change of the input signal:

$$\left. \frac{dv}{dt} \right|_{\max} \leq \frac{1 \text{ LSB}}{t_{\text{conv}}}$$

The amplitude of a fullscale sine wave input signal is equal to  $2^N/2$ , or  $2^{(N-1)}$ , and its maximum rate-of change is

$$\left. \frac{dv}{dt} \right|_{\max} = 2\pi f_{\max} \cdot 2^{N-1} = \pi f_{\max} \cdot 2^N$$

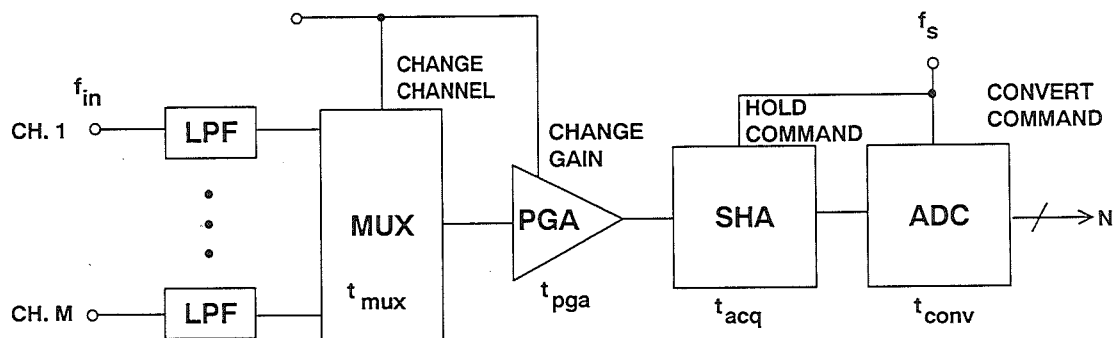
Setting the two equations equal, and solving for  $f_{\max}$ ,

$$f_{\max} \leq \frac{1}{\pi \cdot 2^N t_{\text{conv}}}$$

For example, if the ADC conversion time is  $20\mu\text{sec}$  (corresponding to a maximum sampling rate of slightly less than 50kSPS), and the resolution is 12-bits, then the maximum channel input signal frequency is limited to 4Hz. This may be adequate if the signals are DC, but the lack of a SHA function severely limits the ability to process dynamic signals.

Adding a SHA function to the ADC as shown in Figure 7.5 allows processing of much faster signals with almost no increase in system complexity, since sampling ADCs such as the AD1674 have the SHA function on-chip.

## THE ADDITION OF A SHA FUNCTION TO THE ADC ALLOWS PROCESSING OF DYNAMIC INPUT SIGNALS



■ In General,  $\sqrt{t_{\text{mux}}^2 + t_{\text{pga}}^2} \ll t_{\text{acq}} + t_{\text{conv}}$

■ Therefore,  $f_s \leq \frac{1}{t_{\text{acq}} + t_{\text{conv}}}$

■ Example: If  $t_{\text{acq}} = 1\mu\text{sec}$ ,  $t_{\text{conv}} = 9\mu\text{s}$ , then  $f_s \leq 100\text{kSPS}$

Then  $f_{\text{in}} \leq f_s / 2M$

Figure 7.5

# TYPICAL TIMING DIAGRAM FOR MULTIPLEXED DATA ACQUISITION SYSTEM USING SHA

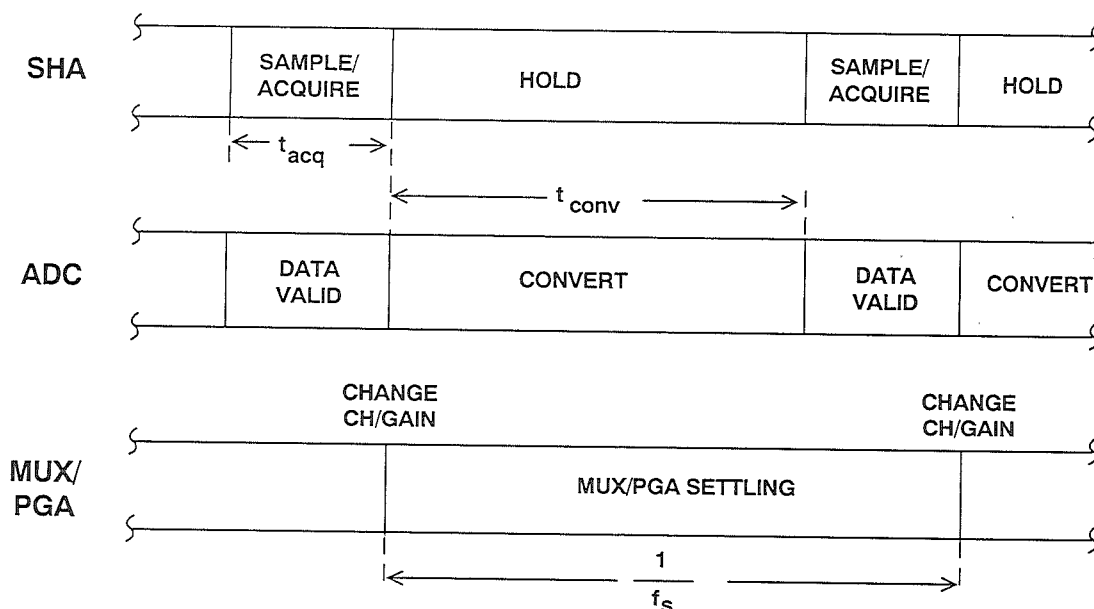


Figure 7.6

The timing is adjusted such that the multiplexer and the PGA are switched immediately following the acquisition time of the SHA. If the combined multiplexer and PGA settling time is less than the ADC conversion time (see Figure 7.6), then the maximum sampling frequency of the system is given by:

$$f_s \leq \frac{1}{t_{acq} + t_{conv}}$$

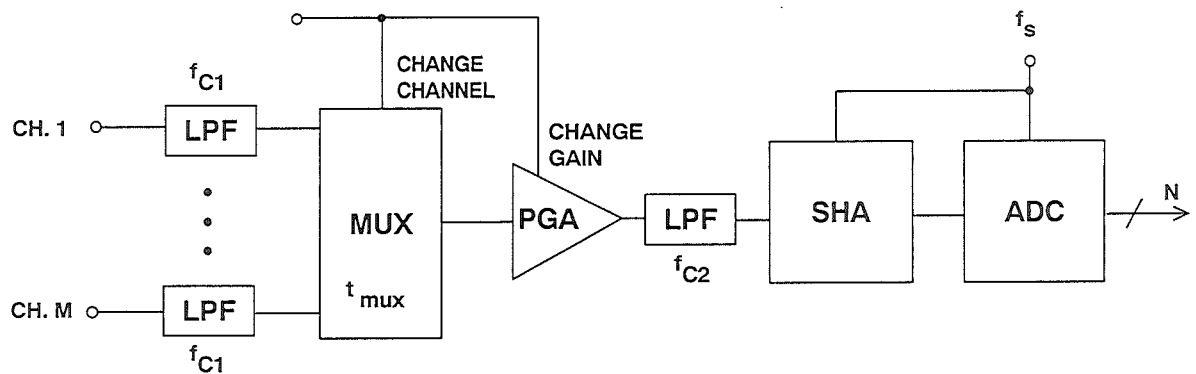
The AD1674 has a conversion time of  $9\mu s$ , an acquisition time of  $1\mu s$  to 12-bits, and a sampling rate of 100kSPS is possible. If all the channels are addressed. The per-channel sampling rate is obtained by dividing the ADC sampling rate by M.

## FILTERING CONSIDERATIONS IN DATA ACQUISITION SYSTEMS

Filtering in data acquisition systems not only prevents aliasing of unwanted signals but also reduces noise by limiting bandwidth. In a multiplexed sys-

tem, there are basically two places to put filters: in each channel, and at the multiplexer output.

### FILTERING IN A DATA ACQUISITION SYSTEM



$$\text{For Sequential Sampling, } f_{C1} < \frac{f_s}{M}$$

Figure 7.7

The filter at the input of each channel is used to prevent aliasing of signals which fall outside the Nyquist bandwidth. The per-channel sampling rate (assuming each channel is sampled at the same rate) is  $f_s/M$ , and the corresponding Nyquist frequency is  $f_s/2M$ . The filter should provide sufficient attenuation at  $f_s/2M$  to prevent dynamic range limitations due to aliasing. Specifying this filter is discussed in detail in Section 4.

A second filter can be placed in the signal path between the multiplexer output and the ADC, usually between the PGA and the SHA. The cutoff frequency of this filter must be carefully chosen because of its impact on settling time. In a multiplexed system such as shown in Figure 7.7, there can be a fullscale step voltage change at the multiplexer output when it is switched between channels. This occurs if the signal on one channel is positive

fullscale, and the signal on the adjacent channel is negative fullscale. From the timing diagram shown in Figure 7.6, the signal from the filter has essentially the entire conversion period ( $1/f_s$ ) to settle from the step voltage. The signal should settle to within 1LSB of the final value in order not to introduce a significant error. The settling time require-

ment therefore places a lower limit on the filter's cutoff frequency. The single-pole filter settling time required to maintain a given accuracy is shown in Figure 7.8. The settling time requirement is expressed in terms of the filter time constant and also the ratio of the filter cutoff frequency,  $f_{c2}$ , to the ADC sampling frequency,  $f_s$ .

### SINGLE-POLE FILTER SETTLING TIME TO REQUIRED ACCURACY

RESOLUTION, # OF BITS	LSB (%FS)	# OF TIME CONSTANTS	$f_{c2}/f_s$
6	1.563	4.16	0.67
8	0.391	5.55	0.89
10	0.0977	6.93	1.11
12	0.0244	8.32	1.32
14	0.0061	9.70	1.55
16	0.00153	11.09	1.77
18	0.00038	12.48	2.00
20	0.000095	13.86	2.22
22	0.000024	15.25	2.44

Figure 7.8

As an example, assume that the ADC is a 12-bit one sampling at 100kSPS. From the table in Figure 7.8, 8.32 time constants are required for the filter to settle to 12-bit accuracy, and

$$\frac{f_{c2}}{f_s} \geq 1.32, \text{ or}$$

$$f_{c2} \geq 132\text{kSPS}.$$

While this filter will help prevent wideband noise from entering the SHA, it does not provide the same function as

the antialiasing filters at the input of each channel.

The above analysis assumes that the multiplexer/PGA combined settling time is significantly less than the filter settling time. If this is not the case, then the filter cutoff frequency must be larger, and in most cases it should be left out entirely in favor of per-channel filters.

## SHA AND ADC SETTling TIME REQUIREMENTS IN MULTIPLEXED APPLICATIONS

We have discussed the importance of the fullscale settling time of the multiplexer/PGA/filter combination, but what is equally important is the ability of the ADC to acquire the final value of the step voltage input signal to the required accuracy. Failure of any link in the signal chain to settle will result in dc crosstalk between adjacent channels and loss of accuracy. If the data acquisition system uses a separate SHA and ADC, then the key specification to examine is the SHA acquisition time, which is usually specified as the amount of time required to acquire a fullscale input signal to 0.1% accuracy (10-bits) or 0.01% accuracy (13-bits). In most cases, both 0.1% and 0.01% times are specified. If the SHA acquisition time is not specified for 0.01% accuracy or better, it should not be used in a 12-bit multiplexed application.

If the ADC is a sampling one (with internal SHA), the SHA acquisition time required to achieve a level of accuracy may still be specified, as in the

case of the AD1674 ( $1\mu\text{s}$  to 12-bit accuracy). SHA acquisition time and accuracy are not directly specified for some sampling ADCs, so the transient response specification should be examined. The transient response of the ADC (settling time to within 1 LSB for a fullscale step input) must be less than  $1/f_s$ , where  $f_s$  is the ADC sampling rate. This often ignored specification may become the weakest link in the signal chain. In some cases neither the SHA acquisition time to specified accuracy nor the transient response specification may appear on the data sheet for the particular ADC, in which case it is probably not acceptable for multiplexed applications. Because of the difficulty in measuring and achieving better than 12-bit settling times using discrete components, the accuracy of most multiplexed data acquisition systems is limited to 12-bits. Designing multiplexed systems with greater accuracy is extremely difficult, and using a single ADC per channel should be strongly considered at higher resolutions.



## SHA AND ADC CONSIDERATIONS IN MULTIPLEXED DATA ACQUISITION SYSTEMS

- Examine SHA Acquisition Time Specification to Required Accuracy :

0.1% = 10-bits

0.01% = 13-bits

- If Sampling ADC, SHA Acquisition Time may not be given, so examine Transient Response Specification
- Inadequate Settling Results in Loss of Accuracy and Causes DC Crosstalk Between Channels
- Multiplexing at greater than 12-bits Accuracy, or at Video Speeds is Extremely Difficult!

Figure 7.9

## COMPLETE DATA ACQUISITION SYSTEMS ON A CHIP

VLSI mixed-signal processing allows the integration of large and complex data acquisition circuits on a single chip. Most signal conditioning circuits including multiplexers, PGAs, and SHAs, may now be manufactured on the same chip as the ADC. This high level of integration permits data acquisition systems to be specified and tested as a single complex function.

Such functionality relieves the designer of most of the burden of testing and calculating error budgets. The DC and AC characteristics of a complete data acquisition system are specified as a complete function, which removes the necessity of calculating performance from a collection of individual worst case device specifications. A complete monolithic system should achieve a higher performance at much lower cost

than would be possible with a system built up from discrete functions. Furthermore, system calibration is easier and in fact many monolithic DASs are self calibrating.

With these high levels of integration, it is both easy and inexpensive to make many of the parameters of the device programmable. Parameters which can be programmed include gain, filter cutoff frequency, and even ADC resolution and conversion time, as well as the obvious digital/MUX functions of input channel selection, output data format, and unipolar/bipolar range.

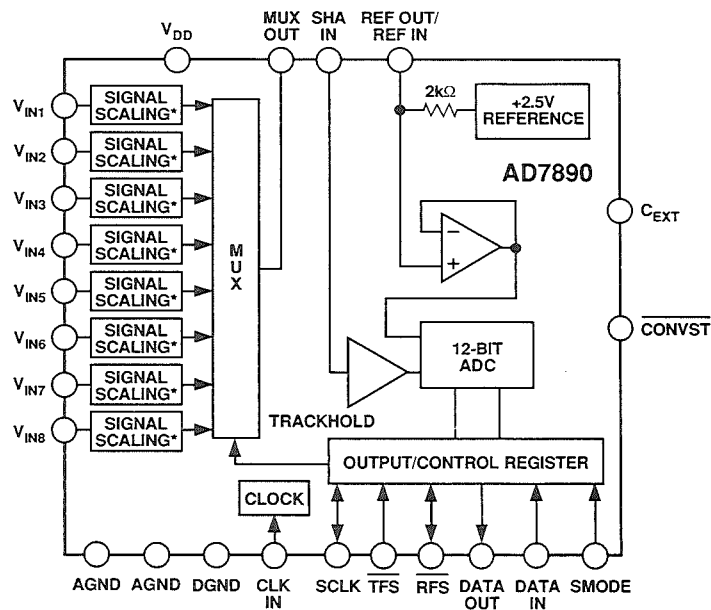
The AD7890 is an example of a highly integrated monolithic data acquisition system. It has 8 multiplexed input channels, a SHA amplifier, an internal voltage reference, and a fast 12-bit

ADC. Input scaling allows up to  $\pm 10V$  inputs when operating on a single +5V supply. Its block diagram is shown in Figure 7.10, and key specifications are summarized in Figure 7.11. Both AC and DC parameters are fully specified, simplifying the preparation of an error

budget, and three types are available with three different standard input ranges:-

AD7890-10	$\pm 10 V$
AD7890-5	0 to 5V
AD7890-2	0 to +2.5V

### AD7890 8-CHANNEL, 12-BIT, 100kSPS COMPLETE DATA ACQUISITION SYSTEM



\*NO SCALING ON AD7890-2

Figure 7.10

## AD7890 SPECIFICATIONS

■	ADC Conversion Time:	5.9 $\mu$ s
■	SHA Acquisition Time:	2 $\mu$ s
■	117kSPS Throughput Rate	(Includes 0.6 $\mu$ s Overhead)
■	AC and DC Specifications	
■	Single +5V Operation	
■	Low Power Drain:	
	Operational:	30mW
	Power Down Mode:	1mW
■	Standard Input Ranges:	
	AD7890 - 10:	$\pm 10$ V
	AD7890 - 5:	0 to +5V
	AD7890 - 2:	0 to +2.5V

Figure 7.11

The input channel selection is via a serial input port. A total of 5 bits of data control the AD7890 via a serial port:- 3 address bits select the input channel, a CONV bit starts the A-D conversion, and 1 in the STBY register places the device in a power-down mode where its power consumption is under 1mW. All timing takes place on the chip and a single external capacitor controls the acquisition time of the internal track-and-hold. A-D conversion may also be initiated externally using the CONVST pin.

With the serial clock rate at its maximum of 10MHz, the achievable throughput rate for the AD7890 is 5.9 $\mu$ s (conversion time) plus 0.6 $\mu$ s (six serial clocks of internal overhead) plus 2 $\mu$ s (acquisition time). This results in a minimum throughput time of 8.5 $\mu$ s (equivalent to a throughput rate of 117kSPS). The AD7890 draws 30mW from a +5V supply.

## MULTIPLEXING INPUTS TO SIGMA-DELTA ADCs

As was discussed in Section 5, the digital filter is an integral part of a sigma-delta ADC. If the inputs to a sigma-delta ADC are switched using a multiplexer, the digital filter must be allowed to settle before valid data is available. As an example, the AD7710-family of ADCs contains an on-chip multiplexer (see Figure 7.12 and Figure

7.13), and the digital filter (frequency response shown in Figure 7.13) requires three conversion cycles (300ms at a 10Hz throughput rate) to settle. It is thus possible to multiplex sigma-delta converters, provided adequate time is allowed for the internal digital filter to settle.

### THE AD771X-SERIES PROVIDES A HIGH LEVEL OF INTEGRATION IN A 24-PIN PACKAGE

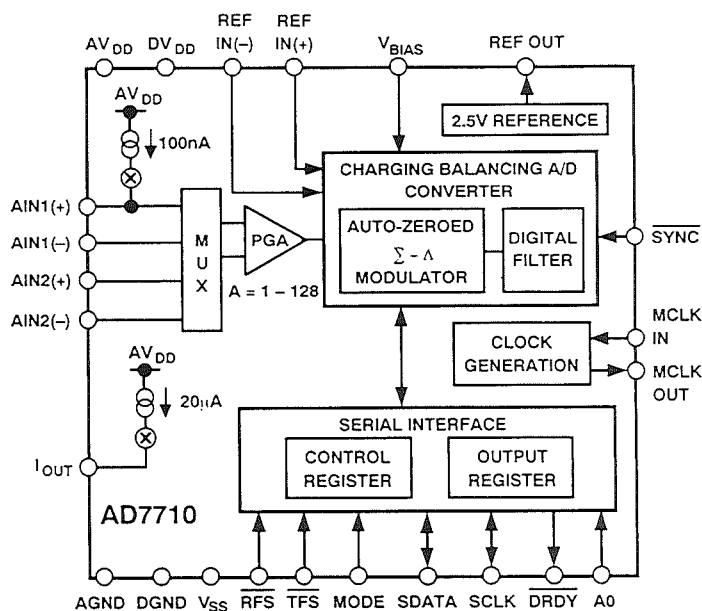


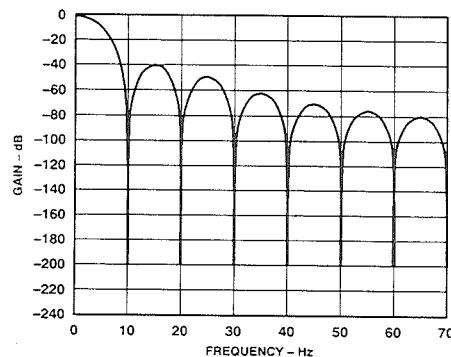
Figure 7.12

## KEY FEATURES OF THE AD7710

- $\pm 0.0015\%$  Nonlinearity
- Two Channels with Differential Inputs
- Programmable Gain Amplifier ( $G = 1$  to  $128$ )
- Programmable Low Pass Filter
- System or Self-Calibration Option
- Single or Dual 5V Supply Operation
- Microcontroller Serial Interface

Figure 7.13

## AD7710 DIGITAL FILTER FREQUENCY RESPONSE



- Response Follows a  $\text{sinc}^3 = \left( \frac{\sin x}{x} \right)^3$
- First Notch Frequency is Programmable and given by:
 
$$f_{\text{notch}} = \left( \frac{f_{\text{clk in}}}{512} \right) \left( \frac{1}{\text{Decimal Value of Digital Code}} \right)$$
- For  $f_{\text{clk in}} = 10\text{MHz}$ ,  $9.76\text{Hz} \leq f_{\text{notch}} \leq 1.028\text{kHz}$

Figure 7.14



## AD7716 QUAD SIGMA-DELTA ADC KEY FEATURES

- Up to 22-Bit Resolution, 4 Input Channels
- $\Sigma\Delta$  Architecture, 570kSPS Oversampling Rate
- On-Chip Lowpass Filter, Programmable from 36.5Hz to 584Hz
- Serial Input / Output Interface
- $\pm 5V$  Power Supply Operation
- Low Power: 50mW

Figure 7.16

## SIMULTANEOUS SAMPLING SYSTEMS

There are certain applications where it is desirable to sample a number of channels simultaneously such as in-phase and quadrature (I and Q) signal processing. A typical configuration is shown in Figure 7.17. Each channel requires its own filter and SHA. Each SHA is simultaneously placed in the hold mode by a common command signal. During the input SHAs' hold time the multiplexer is sequentially switched from channel to channel, and the single non-sampling ADC is used to digitize the signal on each channel. The maximum ADC sampling rate is the reciprocal of the sum of the multiplexer settling time,  $t_{mux}$ , and the ADC conversion time,  $t_{conv}$ .

$$f_{s2} \leq \frac{1}{t_{mux} + t_{conv}}$$

The maximum per-channel sampling frequency is determined by  $M$ ,  $t_{mux}$ ,  $t_{conv}$ , and the acquisition time of the simultaneous SHAs,  $t_{acq1}$ .

$$f_{s1} \leq \frac{1}{t_{acq1} + M(t_{mux} + t_{conv})}$$

## SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING NON-SAMPLING ADC

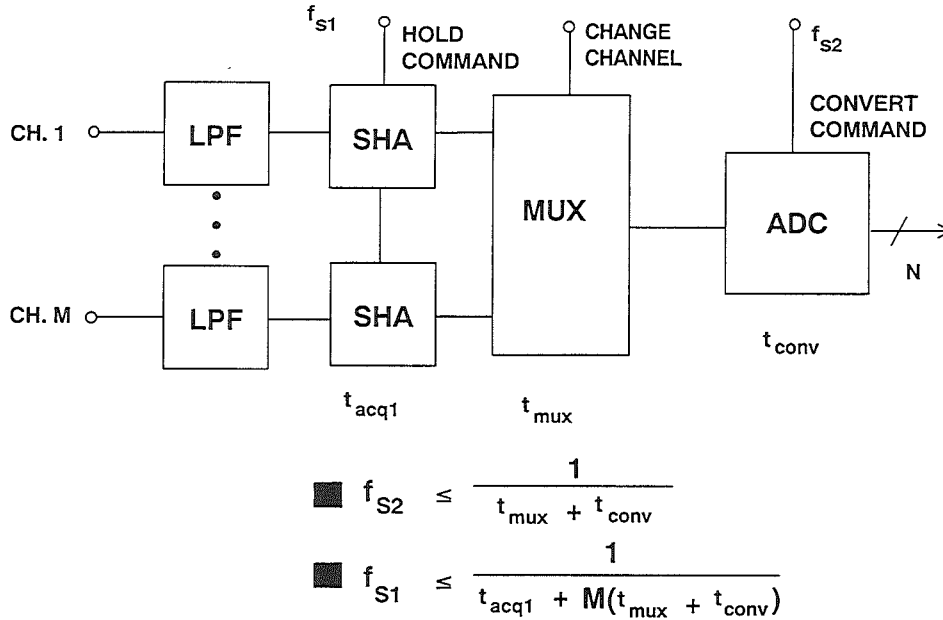


Figure 7.17

If a sampling ADC is used to perform the conversion (see Figure 7.18), the acquisition time of the second SHA,  $t_{\text{acq2}}$ , must be considered in determining the maximum ADC sampling rate,  $f_{s2}$ . The multiplexer should be switched to the next channel after the single SHA goes into the hold mode. If the multiplexer settling time is less than the ADC conversion time, then the maximum ADC sampling rate  $f_{s2}$  is the reciprocal of the sum of the SHA acquisition time and the ADC conversion time.

$$f_{s2} \leq \frac{1}{t_{\text{acq2}} + t_{\text{conv}}}$$

The maximum input sampling frequency is less than this value divided by  $M$ , where  $M$  is the number of channels. Additional timing overhead ( $t_{\text{acq1}}$ ) is required for the simultaneous SHAs to acquire the signals.

$$f_{s1} < \frac{1}{t_{\text{acq1}} + M(t_{\text{conv}} + t_{\text{acq2}})}$$



## SIMULTANEOUSLY SAMPLED DATA ACQUISITION SYSTEM USING SAMPLING ADC

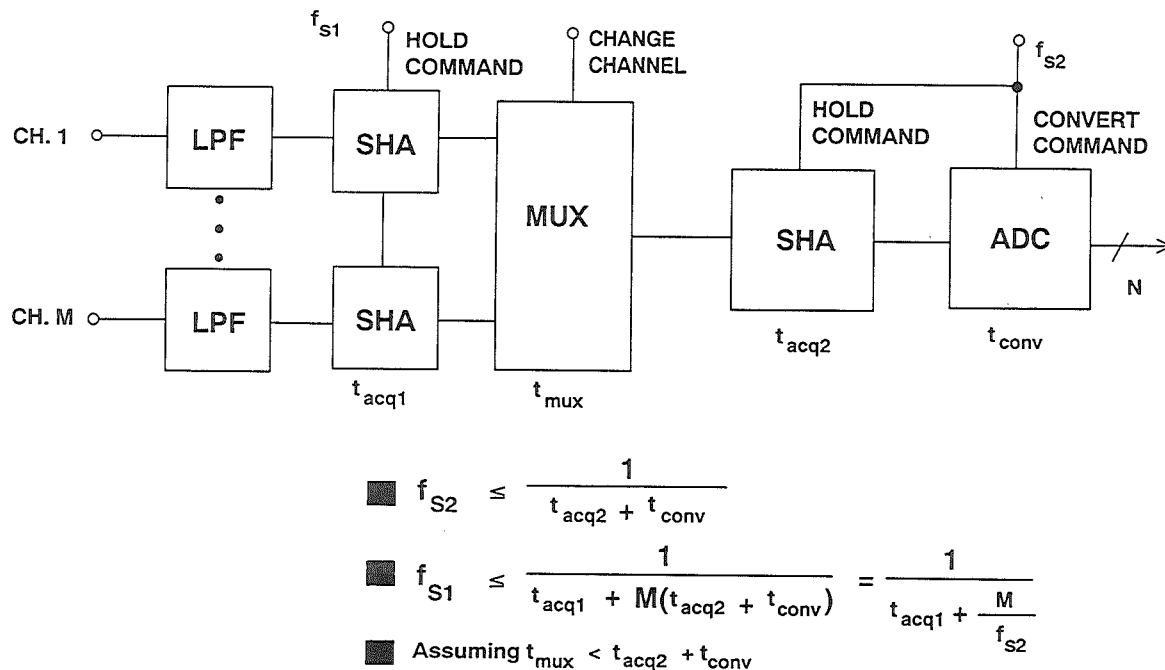


Figure 7.18

## DATA DISTRIBUTION SYSTEMS USING DACs

The simplest method to distribute data in a multi-channel data acquisition system is to use a single DAC per channel as shown in Figure 7.19. The process controller digitally demultiplexes the data for each channel and presents it in parallel format to each DAC. Each DAC is followed by a lowpass antialiasing filter.

An alternate approach is shown in Figure 7.20 where a single DAC output is applied to the input of multiple SHAs.

The timing circuits provide the hold commands sequentially to the individual SHAs as the DAC output is updated. Timing is adjusted so that each SHA enters the hold-mode near just prior to the DAC update.

If this approach is used with a large number of channels, the SHA hold time may become large enough so that SHA droop introduces errors in the outputs. In this case, the multiple DAC approach shown in Figure 7.19 should be used.

## DATA DISTRIBUTION SYSTEM USING MULTIPLE DACs

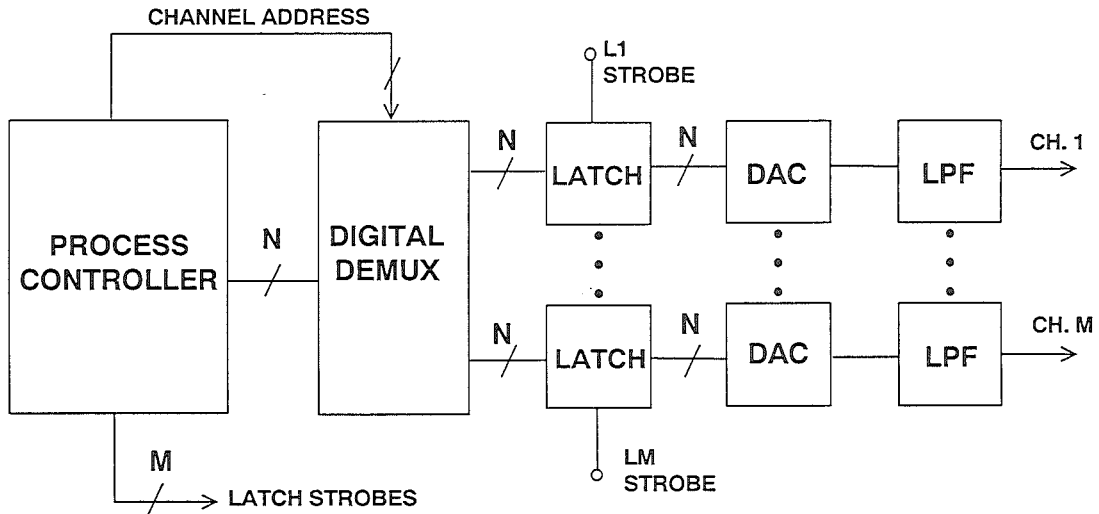


Figure 7.19

## DATA DISTRIBUTION SYSTEM USING SINGLE DAC WITH MULTIPLE SHAs

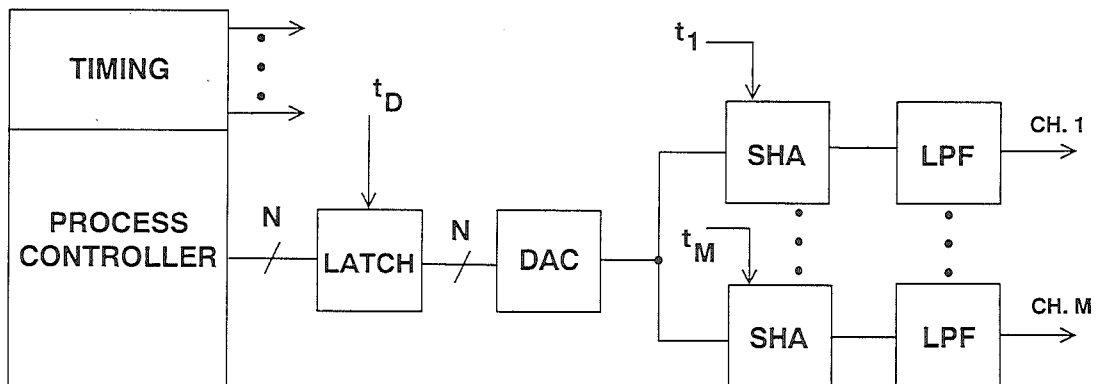


Figure 7.20

## REFERENCE

Dan Sheingold, **Analog-Digital Conversion Handbook, Third Edition**,  
Prentice-Hall, 1986.

## SECTION 8

### SUPPORT CIRCUITRY

- Voltage References:  
Types of Voltage References, Voltage Reference Specifications, Low-Noise References for High Resolution Converters
- Multiplexing Signals with Analog Switches:  
Parasitic Latchup Mechanism and Prevention Techniques, The Anatomy of an Analog Switch, Trench-Isolated LCCMOS Analog Switch Family, Applying the Analog Switch
- Sample-and-Hold Circuits:  
Basic SHA Operation, Track Mode Specifications, Track-to-Hold Mode Specifications, Hold Mode Specifications, Hold to Track Transition Specifications, SHA Architectures, SHA Applications



## SECTION 8

### SUPPORT CIRCUITRY

*Walt Kester, Jerry Whitmore, James Bryant*

#### VOLTAGE REFERENCES

(MATERIAL LARGELY EXTRACTED FROM REFERENCES 4 AND 7)

Voltage references have a major impact on the performance and accuracy of analog systems. A  $\pm 5\text{mV}$  tolerance on a 5V reference corresponds to  $\pm 0.1\%$  absolute accuracy—only 10-bits. For a 12-bit system, choosing a reference that has a  $\pm 1\text{mV}$  tolerance may be far more cost effective than performing manual calibration, while both high initial accuracy and calibration will be necessary in a system making absolute 16-bit measurements. (Many systems make *relative* measurements rather than absolute ones, and in such cases the absolute accuracy of the reference is not important, although noise and short-term stability may be.)

Temperature drift or drift due to aging may be an even greater problem than absolute accuracy. The initial error can always be trimmed, but compensating for drift is difficult. Where possible, references should be chosen to have a temperature coefficient and aging characteristics that preserve adequate accuracy over the operating temperature range and expected lifetime of the system.

Noise in voltage references is often overlooked, but it can be very important in system design. It is generally specified on data sheets, but system designers frequently ignore the specification and assume that voltage references do not contribute to system noise.

There are two dynamic issues that must be considered with voltage references: their behavior at start-up and their behavior with transient loads. Voltage references do not power up instantly (this is true of references inside ADCs and DACs as well as discrete designs). Many early designs took tens, or even hundreds, of milliseconds to deliver any output at all, and as long again before reaching full accuracy - modern designs tend to start up more quickly (but read the data sheet), but still need time to reach thermal equilibrium. It is rarely possible to turn on an ADC and reference, whether internal or external, make a reading, and turn off again within a few microseconds, however attractive such a procedure might be in terms of energy saving. (There are also issues, which we shall not consider here, of anomalous ADC logic states on start-up. Irrespective of reference accuracy, the first, and sometimes even the second, result from an ADC after powering up may be in error because of misbehavior arising from the state of its logic immediately after power is applied.)

Many references have low power, and therefore low bandwidth, buffer amplifiers. This makes for poor behavior under fast transient loads, which may degrade the performance of fast ADCs, especially successive approximation and flash ADCs. Suitable decoupling can

ease the problem (but some references oscillate with capacitive loads), or an additional external broadband buffer

amplifier may be used to drive the node where the transients occur.

## **CHOOSING VOLTAGE REFERENCES FOR HIGH RESOLUTION SYSTEMS**

- Tight Tolerance Improves Accuracy, Reduces Costs
- Temperature Drift Affects Accuracy
- Long-Term Stability Assures Repeatability
- Noise Limits System Resolution
- Dynamic Loading Causes Errors

Figure 8.1

## **TYPES OF VOLTAGE REFERENCES**

Two simple diode-based references are shown in Figure 8.2. In the first, a current-driven forward biased diode (or diode-connected transistor) produces a voltage,  $V_f$ . While the junction drop is somewhat decoupled from the raw power supply, it has numerous deficiencies as a reference including a  $-0.3\%/^{\circ}\text{C}$  temperature coefficient, sensitivity to loading, and an inflexible output volt-

age (only available in 600mV increments). This simple reference (as well as other shunt-type regulators) does have one basic advantage in that the polarity is easily reversible by flipping connections and reversing the drive current polarity. However, a basic limitation of all shunt regulators is that the load current must always be much less than the driving current  $I_D$ .

## SIMPLE DIODE REFERENCE CIRCUITS

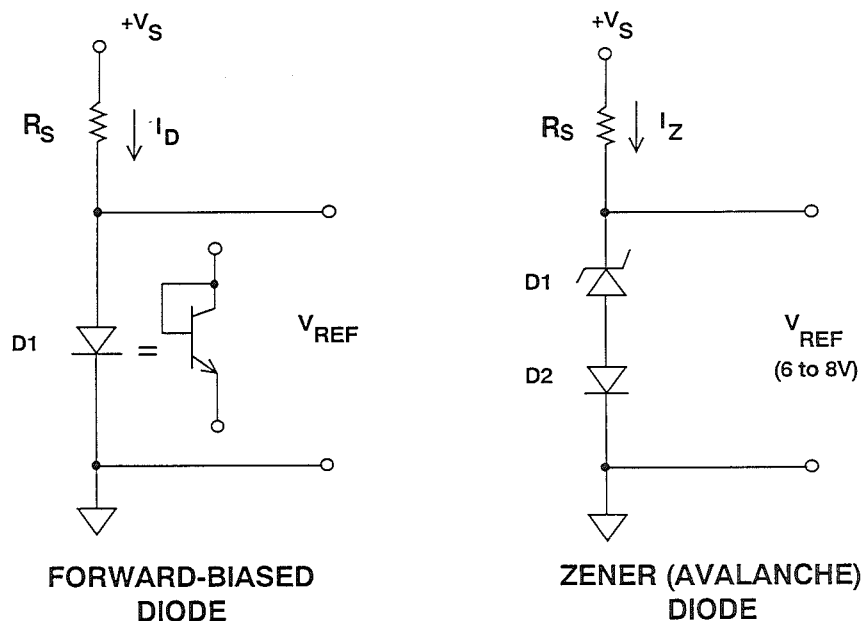


Figure 8.2

In the second circuit of Figure 8.2, a zener or avalanche diode is used, and an appreciably higher output voltage realized. While true *zener* breakdown occurs below 5V, *avalanche* breakdown occurs at higher voltages and has a positive temperature coefficient. (Diode reverse breakdown is referred to almost universally today as *zener*, even though it is usually avalanche breakdown.) With a D1 breakdown voltage in the 5 to 8V range, the net positive TC is such that it equals the negative TC of a forward-biased diode D2, yielding a net TC of 100ppm/°C or less with proper bias current. Combinations of such carefully chosen diodes formed the basis of the early single package “temperature-compensated zener” references, such as the 1N821-1N829 series.

The temperature-compensated zener reference is limited in terms of initial

accuracy, as the best TC combinations fall at odd voltages, such as the 1N829’s 6.2V. In order to obtain the best TC, the diode current must be carefully controlled, making loading somewhat difficult. Zener references must also be driven from voltage sources higher than 6V levels, precluding their operation in 5V systems. References based on low TC avalanche diodes also tend to be noisy due to the noise of the breakdown mechanism. Monolithic zener references described below provide significant improvements.

The development of low voltage (<5V) references based on the bandgap voltage of silicon led to the introductions of various ICs which could be operated on low voltage supplies with good TC performance. The first was the LM109 (Reference 1), and the basic bandgap reference cell is shown in Figure 8.3.



## BASIC BANDGAP REFERENCE

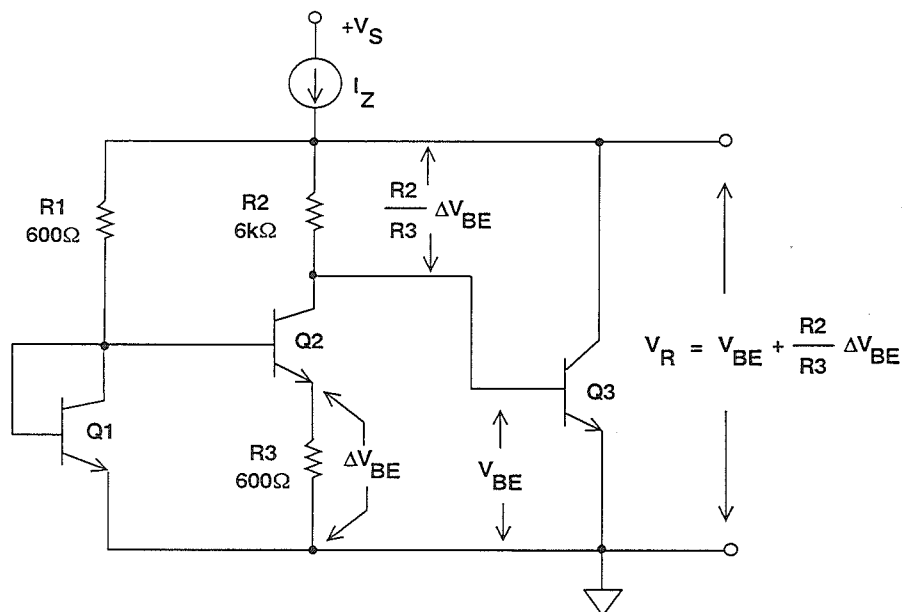


Figure 8.3

This circuit is also called a “ $\Delta V_{BE}$ ” reference because the differing current densities between matched transistors Q1-Q2 produces a  $\Delta V_{BE}$  across R3. It works by summing the  $V_{BE}$  of Q3 with the amplified  $\Delta V_{BE}$  of Q1-Q2, developed across R2. The  $\Delta V_{BE}$  and  $V_{BE}$  components have opposite polarity TCs;  $\Delta V_{BE}$  is proportional-to-absolute-temperature (PTAT), while  $V_{BE}$  is complementary-to-absolute-temperature (CTAT). The summed output is  $V_R$ , and when it is equal to 1.205V (silicon bandgap voltage), the TC is a minimum.

The bandgap reference technique is attractive in IC designs because of its relative simplicity, the avoidance of zeners and their noise, and the fact that

it operates at low voltages. Not only is it used in stand-alone IC references, but it is also used in the design of many other linear ICs such as ADCs, DACs, and op-amps. Buffered forms of 1.2V bandgap references, such as the AD589, remain stable under varying load currents. The AD589 1.235V reference supplies 50μA to 5mA with an output impedance of 0.6Ω, and TCs ranging between 10 and 100ppm/°C.

An improved bandgap reference (popularly called the “Brokaw Cell”, see References 2 and 3) shown in Figure 8.4 provides on-chip buffering which allows good drive capability and voltage scaling. The AD580, which uses this circuit, was the first precision bandgap based IC reference.

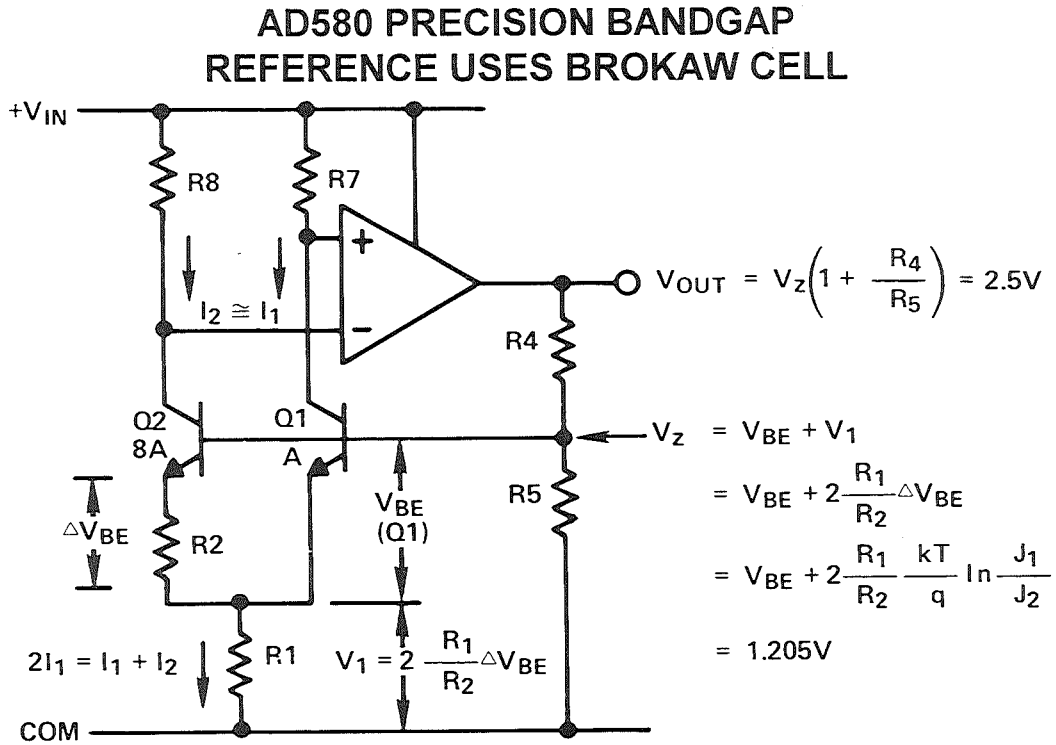


Figure 8.4

The AD580 has two 8:1 emitter-scaled transistors Q1-Q2 operating at identical collector currents (and thus 1/8 current densities), because of equal load resistors and a closed loop around the buffer op-amp. Due to the resultant smaller  $V_{BE}$  of 8× area Q2, R2 in series with Q2 drops the  $\Delta V_{BE}$  voltage, while R1 (due to the current relationships) drops a PTAT voltage V1, which is:

$$V_1 = 2 \times \frac{R_1}{R_2} \times \Delta V_{BE}$$

The bandgap cell reference voltage  $V_Z$  appears at the base of Q1, and is the sum of  $V_{BE}(Q1)$  and V1, or 1.205V, the bandgap voltage.

$$\begin{aligned}
 V_Z &= V_{BE}(Q1) + V_1 \\
 &= V_{BE}(Q1) + 2 \times \frac{R_1}{R_2} \times \Delta V_{BE} \\
 &= V_{BE}(Q1) + 2 \times \frac{R_1}{R_2} \times \frac{kT}{q} \times \ln \frac{J_1}{J_2} \\
 &= V_{BE}(Q1) + 2 \times \frac{R_1}{R_2} \times \frac{kT}{q} \times \ln 8 \\
 &= 1.205V
 \end{aligned}$$

Note that  $J_1$  = current density in Q1,  $J_2$  = current density in Q2, and  $J_1/J_2 = 8$ . However, because of the presence of the R4/R5 (laser trimmed) thin film divider

and the op-amp, the actual voltage appearing at  $V_{OUT}$  can be scaled higher, in this case 2.5V. This voltage can be raised to any practical level, and the AD584 reference provides taps for 2.5, 5, 7.5, and 10V operation. The AD580 provides up to 10mA output current while operating from supplies between 4.5 and 30V. It is available in tolerances as low as 10mV, with TCs as low as 10ppm/°C.

Modern IC references come in a variety of styles, but three-terminal, fixed output positive types dominate. They use either bandgap or zeners at the device core, which has an impact on ultimate specifications and performance.

Figure 8.5 shows the standard footprint for an IC positive reference. There are several details which are important. Many references allow optional trimming by connecting an external trim circuit to drive the references' *trim* input pin. Some bandgap references have a PTAT output ( $V_{TEMP}$ ) for Kelvin temperature sensing. All references should use decoupling capacitors on the input, but the amount of decoupling placed on the output depends upon the stability of the reference's output op-amp with capacitive load (more about this important point shortly).

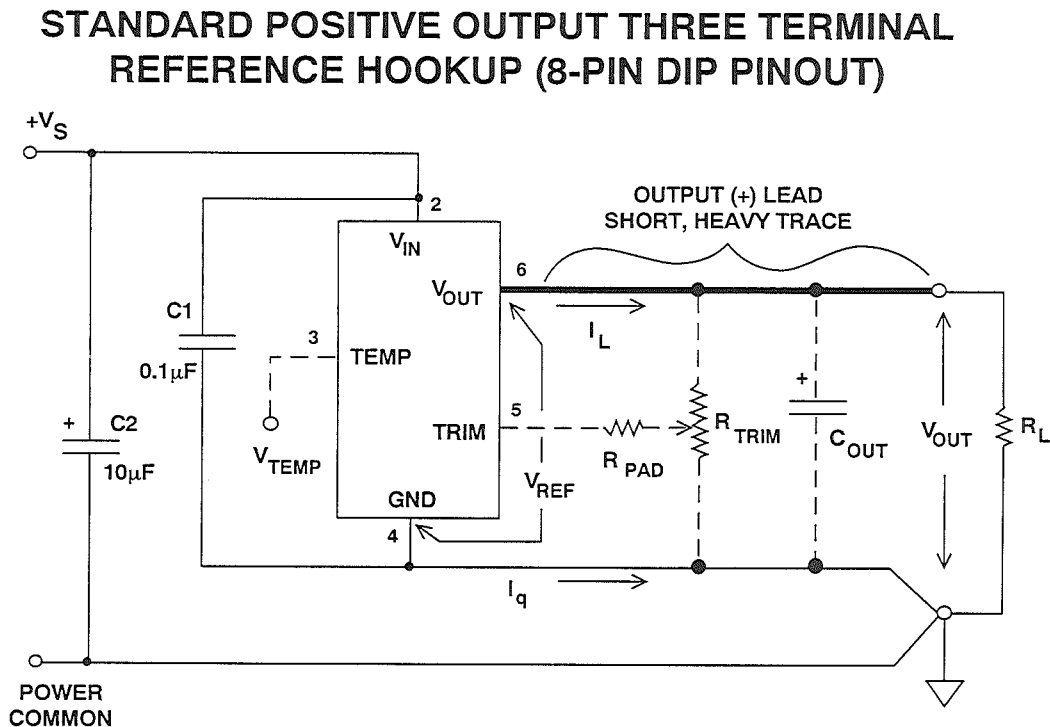


Figure 8.5

There are two basic types of IC references: bandgap and buried zener. Bandgaps have been discussed, but zeners warrant further discussion. The surface of a chip is prone to contamination and lattice dislocations, and zener diodes at the surface are more noisy and less stable than buried ones. All Analog Devices IC references using zeners employ a *buried* (sub-surface) zener technology which improves upon the noise and drift of surface-mode zeners.

Buried zener diodes may be made with a range of voltages, and all have good low noise performance (better than

bandgap references). Ones which have a breakdown voltage just below 7V (in combination with their temperature compensating diodes) have the best temperature performance.

Buried zener references offer the lowest drift, down to the 1-2ppm/°C (AD588 and AD586), and the lowest noise as a percent of fullscale, 100nV/√Hz or less. The best way to compare the noise of references is to compare the ratio of the noise to the output voltage. By this criterion, a 10V reference with 100μV noise is quieter than a 5V reference with 100μV noise.

## ATTRIBUTES OF REFERENCE ARCHITECTURES

8

BANDGAP	BURIED ZENER
■ Low Reference Voltage	■ Low Noise
■ Low Quiescent Power	■ Good Long-Term Stability
	■ Lowest Temperature Drift

Figure 8.6

## **VOLTAGE REFERENCE SPECIFICATIONS**

### **TOLERANCE**

It is better to select a reference with the required value and accuracy and to avoid external trimming and scaling if possible. This allows the best TCs to be realized, as tight tolerances and low TCs usually go hand-in-hand. Tolerances as low as 0.04% can be achieved with the AD586, AD780, REF-195,

while the AD588 is 0.01%. If trimming must be used, be sure to use the recommended trim network with no more range than is absolutely necessary. If additional external scaling is required, a precision op-amp should be used, along with ratio-accurate, low TC tracking thin film resistors.

### **DRIFT**

Buried zener references have the best long term drift and TC performance. TCs as low as 1-2ppm/°C are available with the AD586 and AD588. The AD780 bandgap reference is almost as good at 3ppm/°C. The AD588 offers the lowest long term drift of 25ppm/1000 hours. Where a figure is given for long term drift, it is usually drift expressed in ppm/1000 hours. There are 8766 hours in a year, and many engineers multiply the 1000 hour figure by 8.77 to find the annual drift - this is incorrect. Long term drift in precision analog circuits is a "random walk" phenomenon and increases with the *square root* of the elapsed time (this supposes that drift is due to random micro-effects in the chip and not some over-riding cause such as contamination). The 1 year figure will therefore be about  $\sqrt{8.766} \approx 3$

times the 1000 hour figure, and the ten year value will be roughly 9 times the 1000 hour value. In practice, things are a little better even than this, as devices tend to stabilize with age.

The accuracy of an ADC or DAC can be no better than that of its reference. Reference temperature drift affects fullscale accuracy as shown in Figure 8.7. This table shows system resolution and the TC required to maintain 1/2 LSB error over an operating temperature range of 100°C. For example, a TC of about 1ppm/°C is required to maintain 1/2LSB error at 12-bits. For smaller operating temperature ranges, the drift requirement will be less. The last three columns of the table show the voltage value of 1/2 LSB for popular fullscale ranges.

## REFERENCE TEMPERATURE DRIFT REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB CRITERIA, 100°C SPAN)

BITS	REQUIRED DRIFT, (ppm/°C)	1/2 LSB WEIGHT (mV), VARIOUS FULLSCALE RANGES		
		10V	5V	2.5V
8	19.53	19.53	9.77	4.88
9	9.77	9.77	4.88	2.44
10	4.88	4.88	2.44	1.22
11	2.44	2.44	1.22	0.61
12	1.22	1.22	0.61	0.31
13	0.61	0.61	0.31	0.15
14	0.31	0.31	0.15	0.08
15	0.15	0.15	0.08	0.04
16	0.08	0.08	0.04	0.02

Figure 8.7

### SUPPLY RANGE

IC reference supply voltages range from about 3V (or less) above rated output to 30V (or more) above rated output. Exceptions are devices designed for low

dropout, such as the REF-195 and the AD780. At low currents, the REF-195 can deliver 5V with an input as low as 5.1V (100mV dropout).

### LOAD SENSITIVITY

Load sensitivity (or output impedance) is usually specified in  $\mu\text{V}/\text{mA}$  of load current, or  $\text{m}\Omega$ . While figures of  $100\mu\text{V}/\text{mA}$  ( $100\text{m}\Omega$ ) or less are quite good (AD780, REF-43, REF-195), external wiring drops can produce comparable errors at high currents without care in layout. Load current dependent errors are minimized with short, heavy conductors on the (+) output and on the ground return. For the highest precision, buffer amplifiers and Kelvin sensing circuits (AD588 and AD688) are

used to ensure accurate voltages at the load.

The output of a buffered reference is the output of an op amp, and therefore is a function of frequency. Typical reference output impedance rises at 6dB/octave from the DC value, and are nominally about  $10\Omega$  at a few hundred kHz. This impedance can be lowered with an external capacitor, provided the op-amp in the reference remains stable.

## LINE SENSITIVITY

Line sensitivity (or regulation) is usually specified in  $\mu\text{V}/\text{V}$  of input change, and is lower than  $50\mu\text{V}/\text{V}$  ( $-86\text{dB}$ ) in the REF-43, REF-195, AD680, and AD780. For DC and very low frequencies, such errors are easily masked by noise.

degrades with increasing frequency, typically 30 to 50dB at a few hundred kHz. For this reason, the reference input should be highly decoupled (LF and HF). Line rejection can also be increased with a pre-regulator, such as the 78Lxx-series.

As with op-amps, the line sensitivity (or power supply rejection) of references

## VOLTAGE REFERENCE DC SPECIFICATIONS (TYPICAL VALUES AVAILABLE)

- Tolerance:
  - AD586, AD780, REF-195: 0.04%
  - AD588: 0.01%
- Drift (Temperature Coefficient):
  - AD586, AD588: 1 - 2 ppm/ $^{\circ}\text{C}$
  - AD780: 3 ppm/ $^{\circ}\text{C}$
- Drift (Long Term):
  - 25ppm/1000 hours
- Supply Range: 3V to 30V above rated voltage output  
REF-195 Low Dropout (100mV)
- Load Sensitivity:  $100\mu\text{V}/\text{mA}$  ( $100\text{m}\Omega$ )
- Line Sensitivity:  $50\mu\text{V}/\text{V}$  ( $-86\text{dB}$ )

Figure 8.8

## NOISE

Reference noise is not always specified, and when it is, there is not total uniformity on how. For example, some devices are characterized for peak-to-peak noise in a 0.1 to 10Hz bandwidth, while others are specified in terms of wideband rms or peak-to-peak noise over a specified bandwidth. The most useful way to specify noise (as with op-amps) is a plot of noise voltage spectral density (nV/√Hz) versus frequency.

Low noise references are important in high resolution systems to prevent loss of accuracy. Since white noise is statistical, a given noise density must be related to an equivalent peak-to-peak noise in the relevant bandwidth. Strictly speaking, the peak-to-peak noise in a gaussian system is infinite (but its probability is infinitesimal). Conventionally, the figure of  $6.6 \times \text{rms}$  is used to define a practical peak value - statistically, this occurs less than 0.1% of the time. This peak-to-peak value should be less than 1/2LSB in order to maintain required accuracy. If peak-to-

peak noise is assumed to be 6 times the rms value, then for an N-bit system, reference voltage fullscale  $V_{\text{REF}}$ , reference noise bandwidth (BW), the required noise voltage spectral density  $E_n$  (V/√Hz) is given by:

$$E_n \leq \frac{V_{\text{REF}}}{12 \cdot 2^N \cdot \sqrt{\text{BW}}}$$

For a 10V, 12-bit, 100kHz system, the noise requirement is a modest 643nV/√Hz. Figure 8.9 shows that increasing resolution and/or lower fullscale references make noise requirements more stringent. The 100kHz bandwidth assumption is somewhat arbitrary, but the user may reduce it with external filtering, thereby reducing the noise. Most good IC reference have noise spectral densities around 100nV/√Hz, so additional filtering is obviously required in most high resolution systems, especially those with low values of  $V_{\text{REF}}$ .

### REFERENCE NOISE REQUIREMENTS FOR VARIOUS SYSTEM ACCURACIES (1/2 LSB / 100kHz CRITERIA)

BITS	NOISE DENSITY (nV/√Hz) VARIOUS FULLSCALE RANGES		
	10V	5V	2.5V
12	643	322	161
13	322	161	80
14	161	80	40
15	80	40	20
16	40	20	10

Figure 8.9



Some references like the AD587 (see Figure 8.10) have a pin designated as the *noise reduction pin*. The capacitor  $C_N$  forms a low pass filter with the internal resistor  $R_B$  that limits the noise bandwidth at the *output* of the zener diode. A  $1\mu\text{F}$  capacitor gives a 3dB bandwidth of 40Hz. The photo shows noise measured in a 1MHz

bandwidth with and without the external filter capacitor, indicating that the filtering provides little value. Although  $C_N$  reduces the zener reference noise, it does not affect the wideband noise generated by the output buffer op-amp. This noise can only be reduced with external filtering.

### REFERENCE NOISE REDUCTION USING THE NOISE REDUCTION PIN

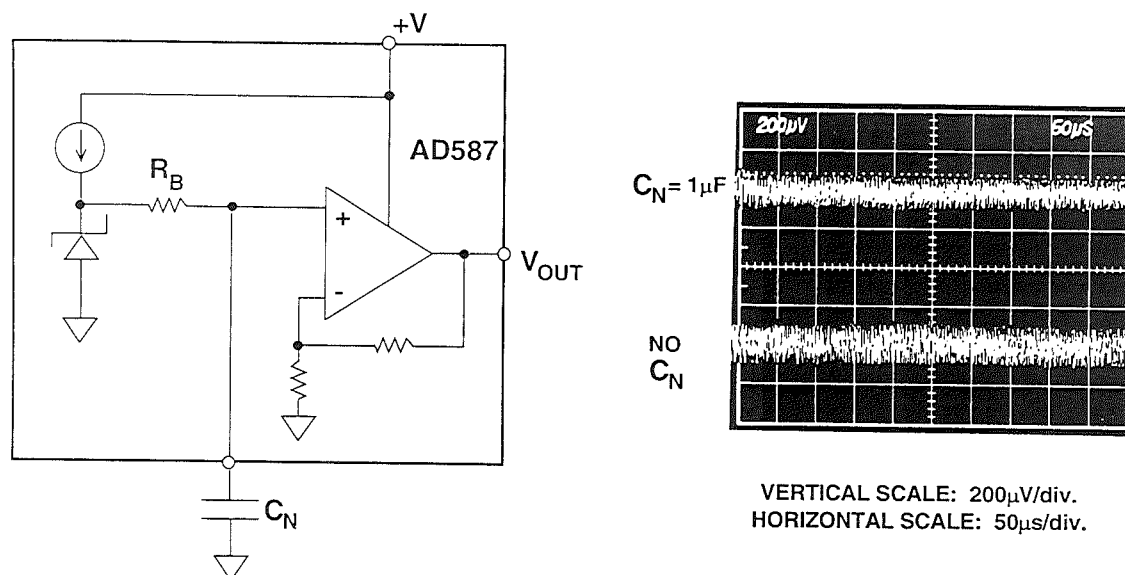


Figure 8.10

The reference circuit in Figure 8.11 (Reference 4) uses external filtering and a precision low-noise op-amp to provide both low noise and dc accuracy. Reference U1 is a 2.5, 3.0, 5, or 10V reference with a low noise buffered output. The output of U1 is applied to the R1-C1/C2 noise filter to produce a corner frequency of about 1.7Hz. Electrolytic

capacitors usually imply dc leakage errors, but bootstrapping C1 causes its bias voltage to be only the small drop across R2. This lowers the leakage current through R1 to acceptable levels. Since attenuation is modest below 10Hz, the reference noise still affects overall performance at low frequencies.

## COMBINING LOW-NOISE AMPLIFIER WITH EXTENSIVE FILTERING YIELDS EXCEPTIONAL NOISE PERFORMANCE (1.5 TO 5nV/ $\sqrt{\text{Hz}}$ @ 1kHz)

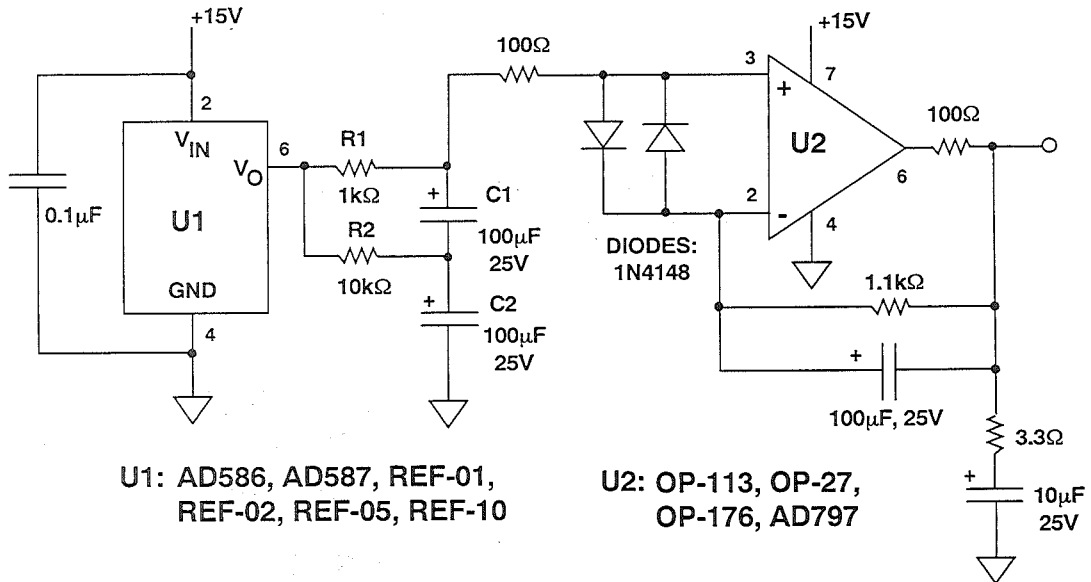


Figure 8.11

The output of the filter is then buffered by a precision low noise unity-gain follower, such as the OP-113EP. With less than  $\pm 150\mu\text{V}$  of offset error and under  $1\mu\text{V}/^\circ\text{C}$  drift, buffer dc performance will not affect the accuracy/drift of most references. The OP-113 has a typical current limit of 40mA, providing output currents higher than a typical IC reference.

While the single-supply OP-113 is useful over the entire 2.5 to 10V range, even lower noise op-amps are available for 5-10V use. The AD797 offers 1kHz noise performance less than  $2\text{nV}/\sqrt{\text{Hz}}$ , compared to about  $5\text{nV}/\sqrt{\text{Hz}}$  for the OP-113. Other op-amps suitable for the 5 to 10V range include the OP-27 and OP-176.

## REFERENCE PULSE CURRENT RESPONSE

The response of references to dynamic loads is often a concern, especially in applications such as driving ADCs and DACs. Fast changes in load current invariably perturb the output, often outside the rated error band. For example, the reference input to a sigma-

delta ADC may be the switched capacitor circuit shown in Figure 8.12. The dynamic load causes current spikes in the reference as the capacitor is charged and discharged. As a result, noise may be induced on the ADC reference circuitry.

### SWITCHED CAPACITOR INPUT OF SIGMA-DELTA ADC PRESENTS A DYNAMIC LOAD TO THE VOLTAGE REFERENCE

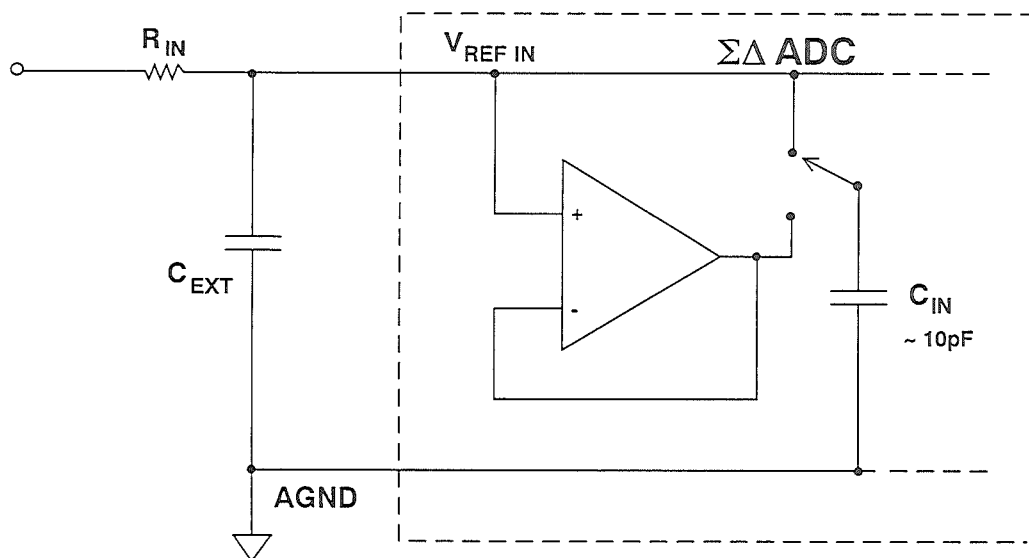


Figure 8.12

Although sigma-delta ADCs have an internal digital filter, transients on the reference input can still cause appreciable conversion errors. An example of sampling noise on a sigma-delta ADC reference is shown in Figure 8.13. The bottom trace shows the noise that is generated if the reference source impedance is too high. The dynamic load causes the reference input to shift by more than 5mV.

A bypass capacitor on the output of a reference may help it to cope with load transients, but many references are unstable with large capacitive loads, and it is important to verify that the one chosen will drive the capacitance required. (The input to references should always be decoupled - with 0.1μF in all cases, and with an additional 5-50μF if there is any LF ripple on its supply.)

## TYPICAL NOISE INDUCED AT THE REFERENCE INPUT OF A SIGMA-DELTA ADC

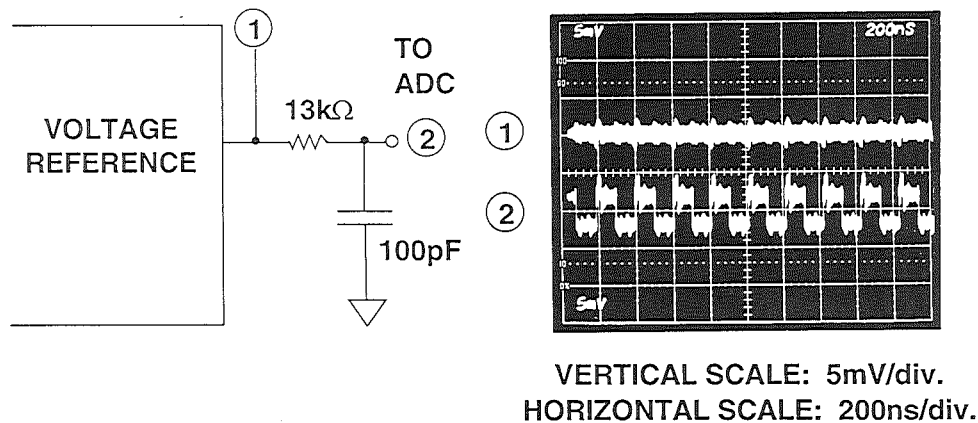


Figure 8.13

## BYPASSING REFERENCE OUTPUT WITH LARGE CAPACITOR HELPS MINIMIZE TRANSIENT LOADS PROVIDED THE REFERENCE REMAINS STABLE

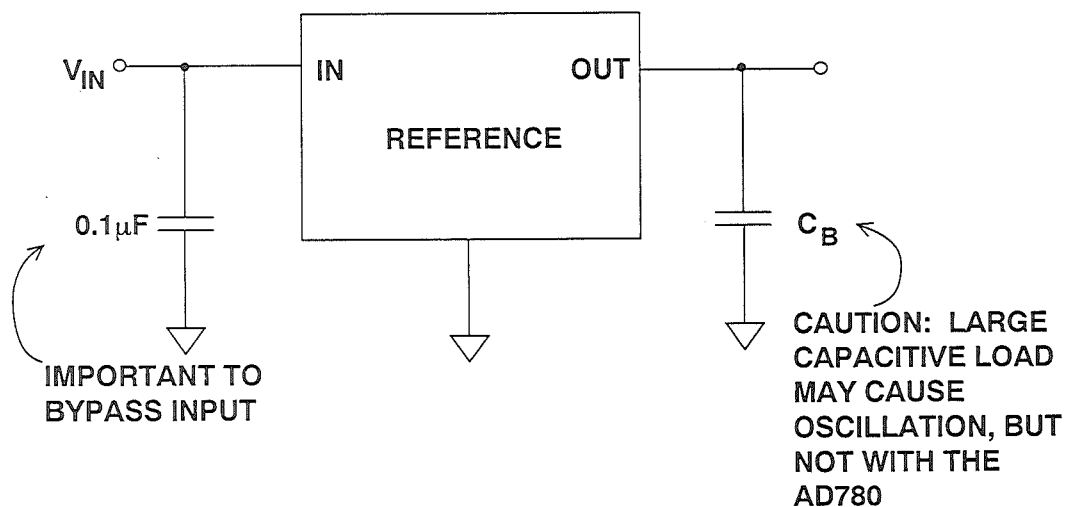


Figure 8.14

Since references do misbehave with transient loads, either by oscillating or by losing accuracy for comparatively long periods, it is advisable to test the pulse response of voltage references which may encounter transient loads. A suitable circuit is shown in Figure 8.15.

In a typical voltage reference, a step change of 1mA produces the transients shown. Both the duration of the transient, and the amplitude of the ringing *increase* when a  $0.01\mu\text{F}$  capacitor is connected to the reference output.

### MAKE SURE REFERENCE IS STABLE WITH LARGE CAPACITIVE LOADS

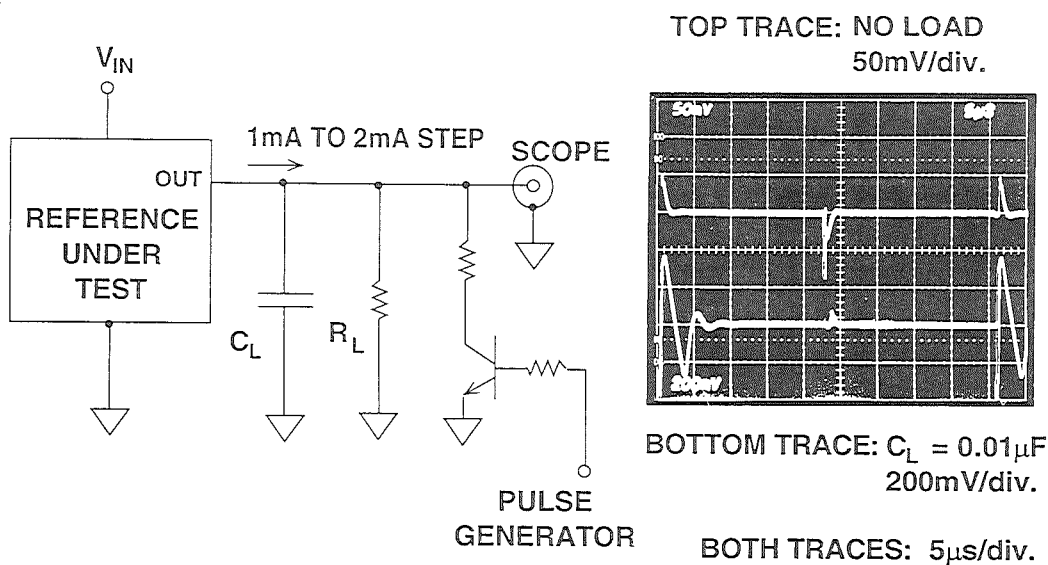


Figure 8.15

Where possible, a reference should be designed to drive large capacitive loads. The AD780 is designed to drive unlimited capacitance without oscillation. It has excellent drift and an accurate output in addition to low power consumption.

Large reference bypass capacitors are useful when driving the reference inputs of successive-approximation

ADCs. Figure 8.16 illustrates reference voltage settling behavior immediately following a "Conversion Start" command. A small capacitor ( $0.01\mu\text{F}$ ) does not provide sufficient charge storage to keep the reference voltage stable during conversion, and errors may result. Decoupling with a  $>1\mu\text{F}$  capacitor maintains the reference stability during conversion.

## SUCCESSIVE APPROXIMATION ADCs CAN PRESENT A DYNAMIC TRANSIENT LOAD TO THE REFERENCE

Solution: Bypass Reference Adequately

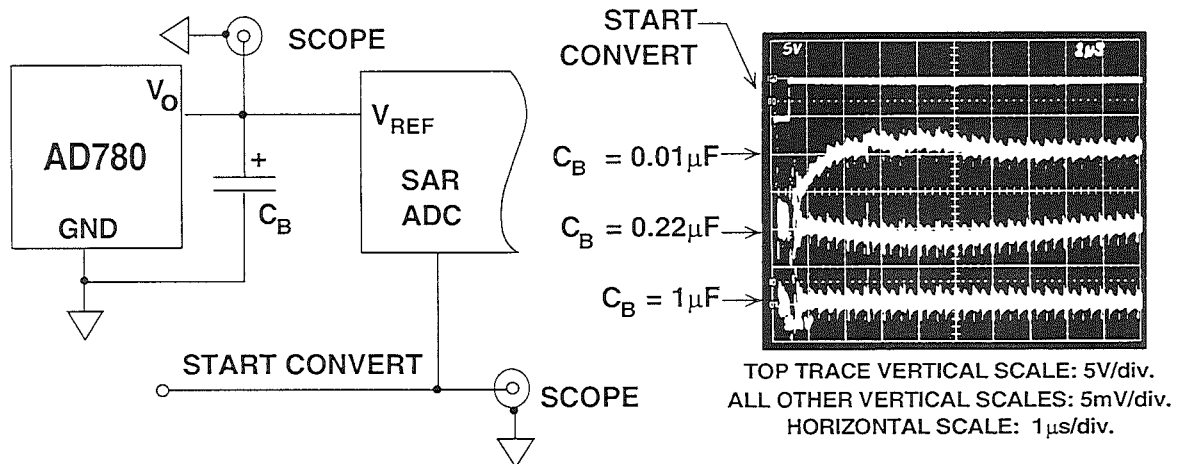


Figure 8.16

Where voltage references drive large capacitances, it is important to realize that their turn-on time will be prolonged. Experiment may be needed to determine the delay before the output of

the reference reaches full accuracy, but it will certainly be much longer than the time specified on the data sheet for the unloaded reference.

## LOW NOISE REFERENCES FOR HIGH RESOLUTION CONVERTERS

High resolution converters (both sigma-delta and high speed ones) can benefit from recent improvements in IC references, such as lower noise and the ability to drive capacitive loads. Even though many data converters have internal references, the performance of these references is often compromised because of the limitations of the converter process. Using an external reference rather than the internal one often yields better overall performance. For example, the AD7710-series of 22-bit ADCs has a 2.5V internal reference with a 0.1 to 10Hz noise of  $8.3\mu\text{V rms}$  ( $2600\text{nV}/\sqrt{\text{Hz}}$ ), while the AD780 refer-

ence only  $0.67\mu\text{V rms}$  ( $200\text{nV}/\sqrt{\text{Hz}}$ ). The internal noise of the AD7710-series in this bandwidth is about  $1.7\mu\text{V rms}$ . The use of the AD780 increases the effective resolution of the AD7710 from about 20.5-bits to 21.5 bits.

Figure 8.17 shows the AD780 used as the reference for the AD7710-series ADCs. The 3V scaling enhances the dynamic range of the ADC, while lowering overall system noise as described above. In addition, the AD780 allows a large decoupling capacitor on its output thereby minimizing conversion errors due to transients.

### THE AD780 IS IDEAL FOR DRIVING PRECISION SIGMA-DELTA ADCs

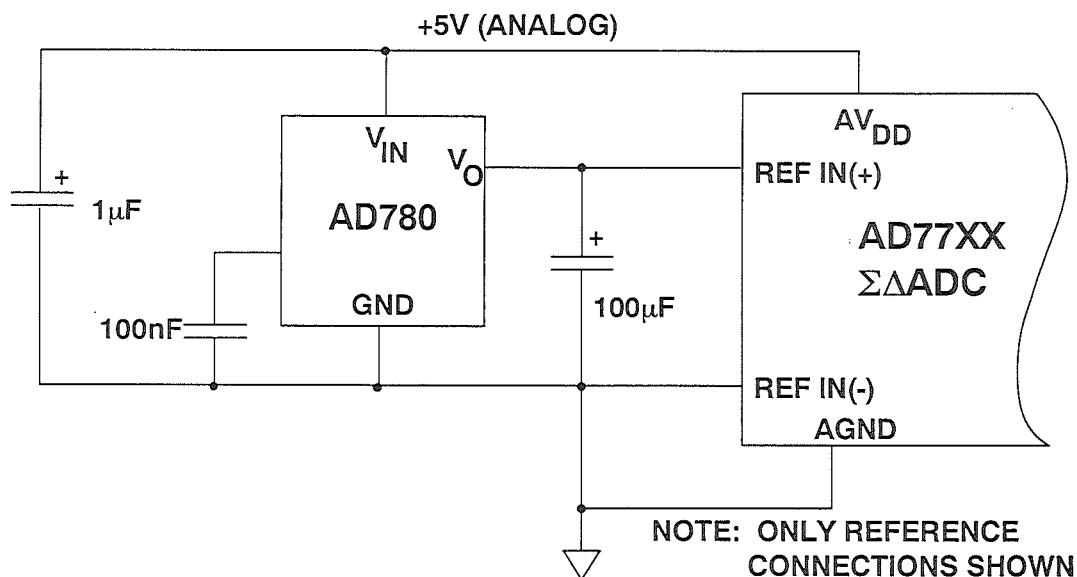


Figure 8.17

There is one possible problem when replacing the internal reference of a converter with a high precision external one. The converter may have been trimmed, during manufacture, to deliver its specified performance with an inaccurate internal reference. In this case, using an accurate reference may introduce additional gain error. For example, the early AD574 had a guar-

anteed uncalibrated gain accuracy of 0.125% when using an internal 10V reference which itself had a specified accuracy of only  $\pm 1\%$ . It is obvious that if such a device, having an internal reference which is at one end of the specified range, is used with an external reference of exactly 10V, then its gain will be about 1% in error.

# MULTIPLEXING SIGNALS WITH ANALOG SWITCHES

*Jerry Whitmore, James Bryant*

Analog signals can be switched, multiplexed, and easily connected using analog switches. With sufficient care, there will be little or no degradation of signal quality. This section is devoted to CMOS technology in analog switch

circuitry, their parasitic latchup mechanisms, and effective protection methods. It also discusses AC switch characteristics and how they affect the performance of a system, and some application circuits.

## MULTIPLEXING CONCEPTS

- Advantages of CMOS Technology in Analog Switch Circuitry
- Parasitic Transistors/Latchup and Protection Methods
- Switch Equivalent Circuit dc and ac Analysis
- Applying the Analog Switch

**8**

Figure 8.18

The ideal analog switch has no ON-resistance, infinite OFF impedance and zero time delay, and can handle large signal and common-mode voltages. Real

CMOS analog switches meet none of these criteria, but if we understand the limitations of analog switches, most of these limitations can be overcome.



## CHARACTERISTICS OF THE IDEAL ANALOG SWITCH

- On Resistance: Zero
- Off Impedance: Infinite at All Frequencies
- Switching Time: Zero
- Switch Leakage: Zero
- Power Dissipation: Zero
- MTBF: Infinite

Figure 8.19

CMOS switches have an excellent combination of attributes. In its most basic form, the MOSFET transistor is a voltage-controlled resistor. In the ON state, its resistance can be less than  $100\Omega$ , while in the OFF-state, the resistance increases to several hundreds of megohms, with nanoamp leakage currents.

CMOS technology is compatible with logic circuitry and can be densely packed in an IC. Its fast switching characteristics are well controlled with minimum circuit parasitics.

MOSFET transistors are bilateral. That is, they can switch positive and negative voltages and conduct positive and negative currents with equal ease.

A MOSFET transistor has a voltage controlled resistance which varies nonlinearly with signal voltage as shown in Figure 8.21. Figure 8.22 shows a basic CMOS switch using complementary P-channel and N-channel MOS devices connected in parallel. This reduces the ON-resistance and also produces a resistance which varies less with signal voltage.

## ADVANTAGES OF MIXED SIGNAL CMOS TECHNOLOGY

- A Great Logic Technology
  - ◆ High Density
  - ◆ Moderate to High Speed
  - ◆ Low Power Dissipation
- An Excellent Switch Technology
  - ◆ MOSFETs are Voltage Controlled Resistors
  - ◆ MOSFETs Lose No Current to the Control Input (Gate)
  - ◆ MOSFETs are Electrically Bilateral -- Can Switch Positive or Negative Voltages or Steer Positive or Negative Current with Equal Ease
  - ◆ No Offset Voltage in Series With ON MOSFET (Unlike Bipolar Transistor)

Figure 8.20

### MOSFET SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

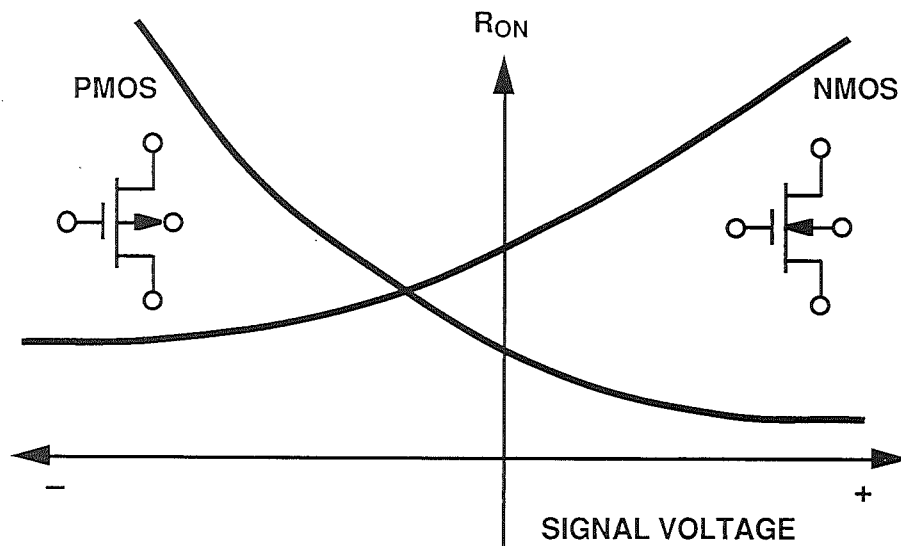


Figure 8.21

## BASIC CMOS SWITCH USES COMPLEMENTARY PAIR TO MINIMIZE $R_{on}$ VARIATION DUE TO INPUT SIGNAL SWING

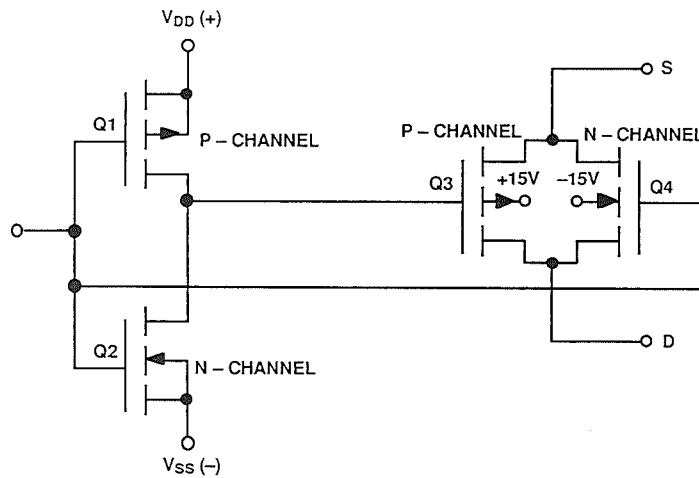


Figure 8.22

Figure 8.23 shows the ON-resistance changing with channel voltage for both N-type and P-type devices. This nonlinear resistance can cause errors in DC accuracy as well as AC distortion. The bilateral CMOS switch solves this

problem. ON-resistance is minimized and its linearity is also improved. The bottom curve of Figure 8.23 shows the improved flatness of the ON-resistance characteristic of the switch.

## CMOS SWITCH ON-RESISTANCE VERSUS SIGNAL VOLTAGE

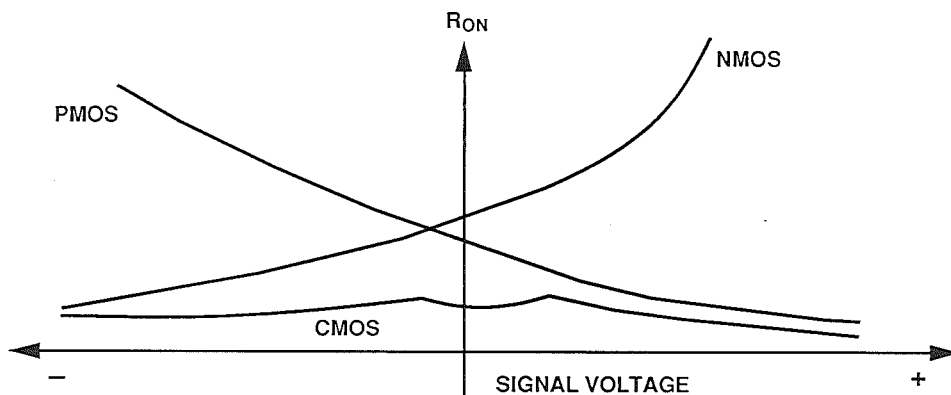


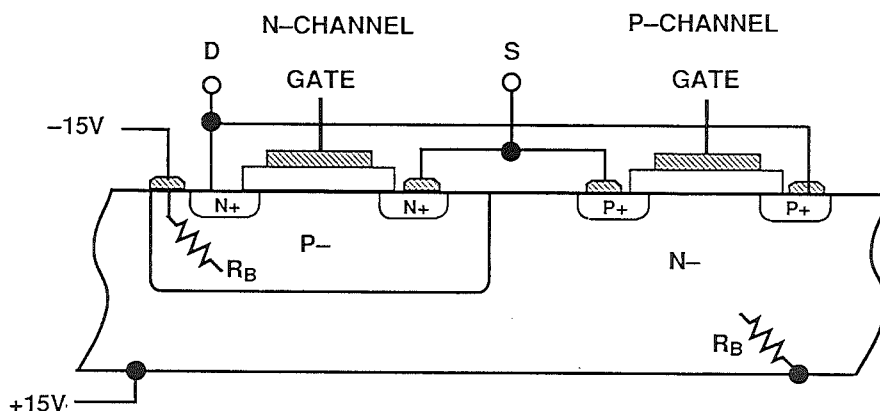
Figure 8.23

## PARASITIC LATCHUP

Most CMOS analog switches are built using junction-isolated CMOS processes. A cross-sectional view of a single switch cell is shown in Figure 8.24. Parasitic SCR (silicon controlled rectifier) latchup can occur if the analog switch terminal has voltages more positive than  $V_{DD}$  (+15V) or more

negative than  $V_{SS}$  (-15V). Even a transient situation, such as power-on with an input voltage present, can trigger a parasitic latchup. If the conduction current is too great (several hundred milliamperes or more), it can damage the switch.

### CROSS SECTION OF JUNCTION-ISOLATED CMOS SWITCH



- Problems Occur if Voltages More Positive Than  $V_{DD}$  or More Negative than  $V_{SS}$  are Applied to an Analog Switch Terminal

8

Figure 8.24

The parasitic SCR mechanism is shown in Figure 8.25. SCR action takes place when either terminal of the switch (source or the drain) is either one diode drop more positive than  $V_{DD}$  or one diode drop more negative than  $V_{SS}$ . In the former case, the  $V_{DD}$  terminal becomes the SCR gate input and provides the current to trigger SCR action.

In the case where the voltage is more negative than  $V_{SS}$ , the  $V_{SS}$  terminal becomes the SCR gate input and provides the gate current. In either case, high current will flow between the supplies. The amount of current depends on the collector resistances of the two transistors, which can be fairly small.

## BIPOLAR TRANSISTOR EQUIVALENT CIRCUIT OF CMOS SWITCH SHOWS PARASITIC ACTION (A CLASSIC SCR LATCH)

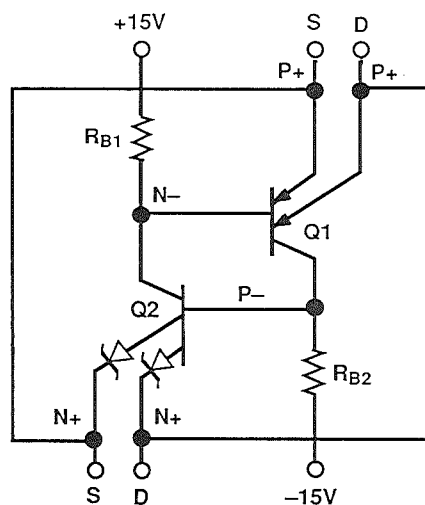


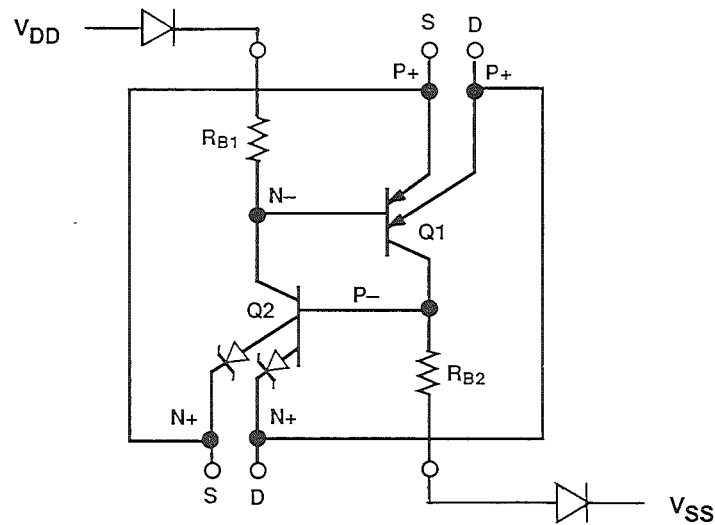
Figure 8.25

In order to prevent this type of SCR latchup, a series diode can be inserted into the  $V_{DD}$  and  $V_{SS}$  terminals as shown in Figure 8.26. The diodes block the SCR gate current. Normally the parasitic transistors Q1 and Q2 have low beta (usually less than 10) and require a comparatively large gate current to fire the SCR. The diodes limit the reverse gate current so that the SCR is not triggered.

If diode protection is used, the analog voltage range of the switch will be reduced by one  $V_{be}$  drop at each rail.

Analog switches must also be protected from possible overcurrent by inserting a series resistor to limit the current to a safe level, generally less than 25mA. This method works only if the switch drives a high impedance load (Figure 8.28).

## DIODE PROTECTION SCHEME FOR CMOS SWITCH



- Protection Diodes CR1 and CR2 Block Base Current Drive to Q1 and Q2 in Event of Overvoltage at S or D

Figure 8.26

## PROTECTING CMOS SWITCH / MUX FROM LATCHUP USING DIODES

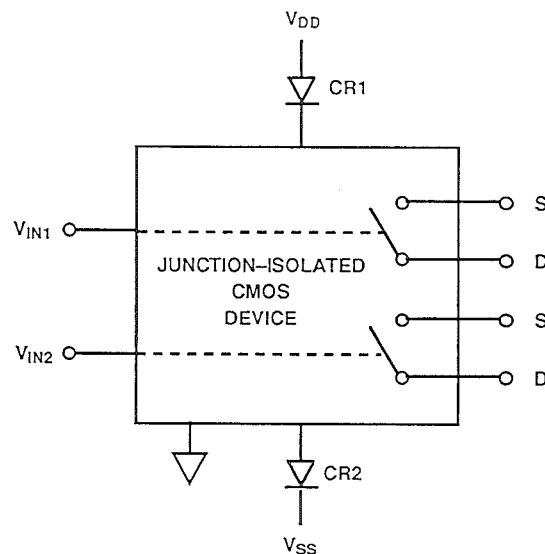
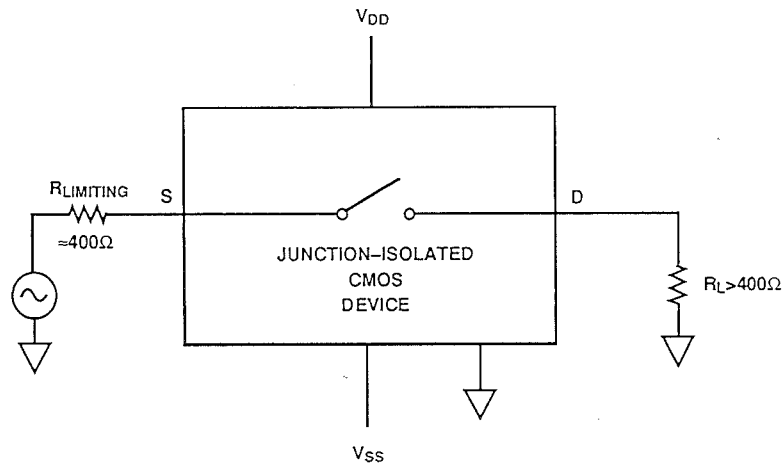


Figure 8.27

## PROTECTING CMOS SWITCH / MUX FROM OVERCURRENT



- External Resistor Limits Current to Safe Value

Figure 8.28

Latchup protection does not provide overcurrent protection and vice versa. If both fault conditions can exist in a

system, then both protection protective diodes and resistors should be used.

## "LATCHPROOF" VERSUS "OVERVOLTAGE PROTECTED"

- *Latchproof* only means the device won't go into an SCR mode.
- It does not guarantee *Overvoltage Protection*.

Figure 8.29

## THE ANATOMY OF THE ANALOG SWITCH

It is important to understand the error sources in an analog switch. Many affect AC and DC performance, while others only affect AC. Figure 8.30

shows the equivalent circuit of two adjacent switches. It includes leakage currents and junction capacitances.

### EQUIVALENT CIRCUIT OF TWO ADJACENT SWITCHES

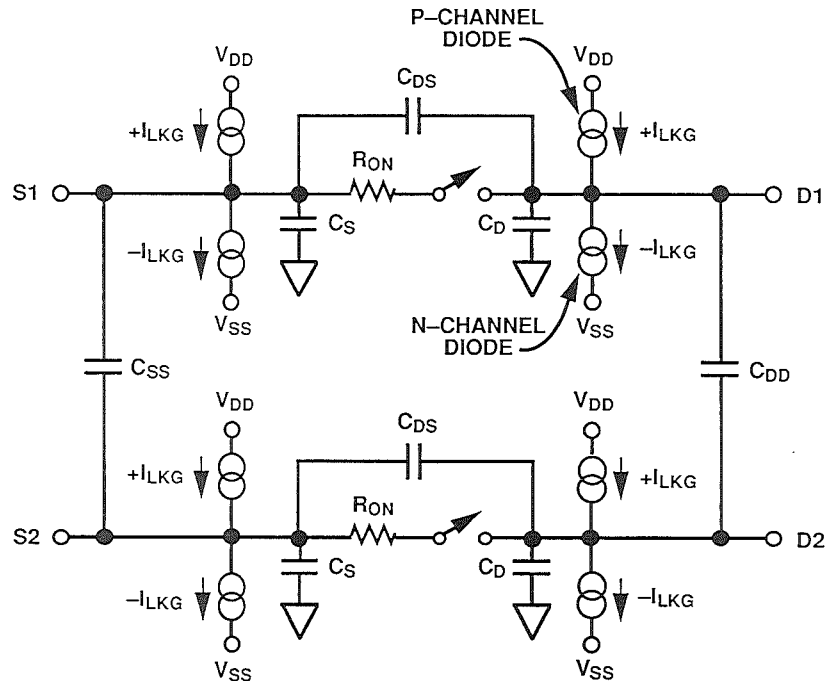


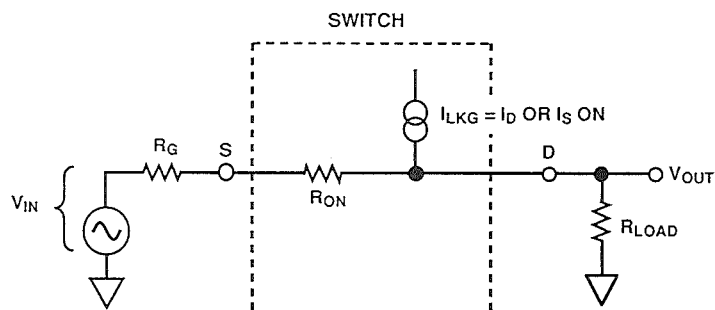
Figure 8.30

DC performance is affected mainly by the switch ON-resistance ( $R_{ON}$ ) and leakage. Low resistance circuits are more subject to errors due to  $R_{ON}$ ,

while high resistance circuits are affected by leakage currents. Figure 8.31 shows how these parameters affect DC performance.



## FACTORS AFFECTING DC PERFORMANCE FOR ON SWITCH CONDITION: $R_{ON}$ , $R_{LOAD}$ , AND $I_{LKG}$



$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_G + R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[ \frac{R_{LOAD}(R_{ON} + R_G)}{R_G + R_{ON} + R_{LOAD}} \right]$$

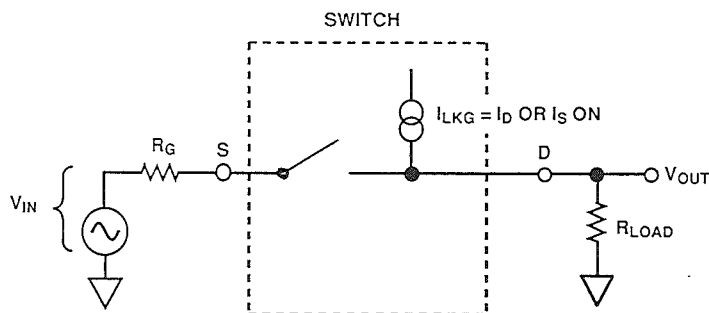
IF  $R_G \rightarrow 0$ ,

$$V_{OUT} = V_{IN} \left[ \frac{R_{LOAD}}{R_{ON} + R_{LOAD}} \right] + I_{LKG} \left[ \frac{R_{LOAD}R_{ON}}{R_{ON} + R_{LOAD}} \right]$$

Figure 8.31

When the switch is OFF, leakage current can introduce errors. (Figure 8.32)

## FACTORS AFFECTING DC PERFORMANCE FOR OFF SWITCH CONDITION: $I_{LKG}$ , AND $R_{LOAD}$



■ Leakage Current Creates Error Voltage at  $V_{OUT}$  Equal to:

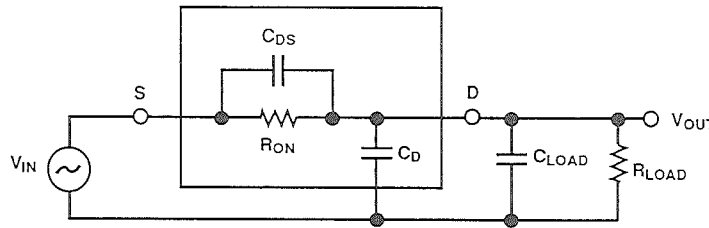
$$V_{OUT} = I_{LKG} \times R_{LOAD}$$

Figure 8.32

Figure 8.33 illustrates the parasitic components that affect the AC performance of CMOS switches. Additional external capacitances will further

degrade performance. These capacitances affect feedthrough, crosstalk and system bandwidth.

## DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY



$$A(s) = \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] \left[ \frac{s R_{ON} C_{DS} + 1}{s \left( \frac{R_{LOAD} R_{ON}}{R_{LOAD} + R_{ON}} \right) (C_{LOAD} + C_D + C_{DS}) + 1} \right]$$

$$A(\text{dB}) = 20 \log \left[ \frac{R_{LOAD}}{R_{LOAD} + R_{ON}} \right] + 10 \log [\omega^2 (R_{ON} C_{DS})^2 + 1] - 10 \log \omega^2 \left[ \left( \frac{R_{LOAD} R_{ON}}{R_{LOAD} + R_{ON}} \right)^2 (C_{LOAD} + C_D + C_{DS})^2 + 1 \right]$$

Figure 8.33

The signal transfer characteristic is dependent on the switch channel capacitance,  $C_{DS}$ . This capacitance creates a frequency zero in the numerator of the transfer function  $A(s)$ . This zero usually occurs at high frequencies because the switch ON resistance is small. The bandwidth is also a function of the switch output capacitance in combination with  $C_{DS}$  and the load capacitance. This frequency pole appears in the denominator of the equation.

The composite frequency domain transfer function may be re-written as shown in Figure 8.34. In most cases, the pole breakpoint frequency occurs first because of the dominant effect of the output capacitance  $C_D$ . Thus, to maximize bandwidth, a switch must have low input and output capacitance and low ON resistance.

## DYNAMIC PERFORMANCE CONSIDERATIONS: TRANSFER ACCURACY VERSUS FREQUENCY

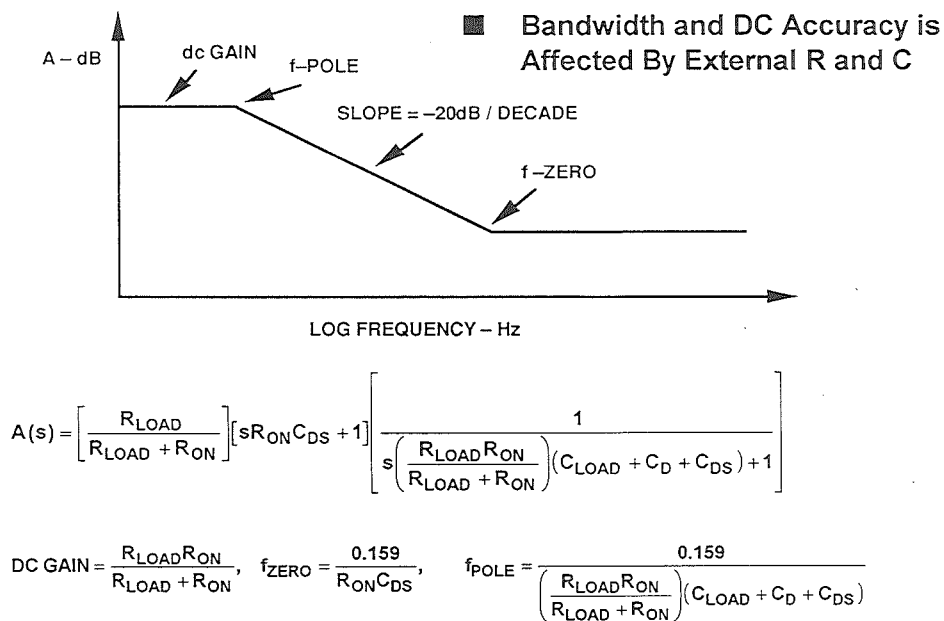


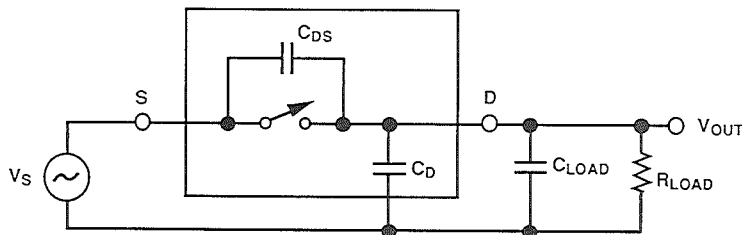
Figure 8.34

The series-pass capacitance,  $C_{DS}$ , not only creates a zero in the response in the ON-state, it degrades the feedthrough performance of the switch

during its OFF state. When the switch is off,  $C_{DS}$  couples the input signal to the output load. (Figure 8.35)

## DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION

■ OFF Isolation is Affected by External R and C Load



$$A(s) = \frac{s(R_{LOAD})(C_{DS})}{s(R_{LOAD})(C_{LOAD} + C_D + C_{DS}) + 1}$$

Figure 8.35

Large values of  $C_{DS}$  will produce large values of feedthrough, proportional to the input frequency. Figure 8.36 illustrates the drop in OFF-isolation as a

function of frequency. The simplest way to maximize the OFF-isolation is to choose a switch that has as small a  $C_{DS}$  as possible.

### DYNAMIC PERFORMANCE CONSIDERATIONS: OFF ISOLATION VERSUS FREQUENCY

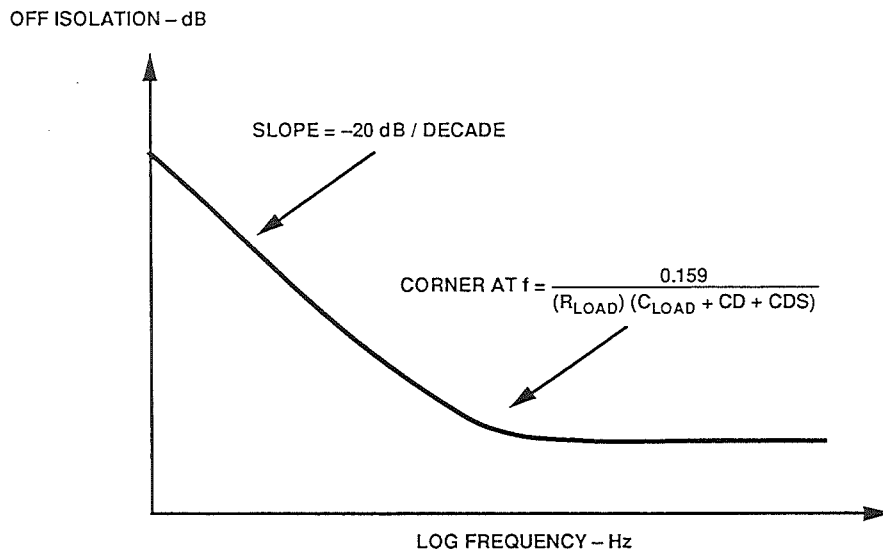


Figure 8.36

8

Figure 8.37 shows typical CMOS analog switch OFF-isolation as a function of frequency. From DC to several kilohertz, the switch has over 100dB isolation.

As the frequency increases, an increasing amount of signal reaches the output. However, even at 1MHz, the switch still has nearly 70dB of isolation.

## TYPICAL CMOS SWITCH OFF ISOLATION PERFORMANCE (ADG511/ADG512)

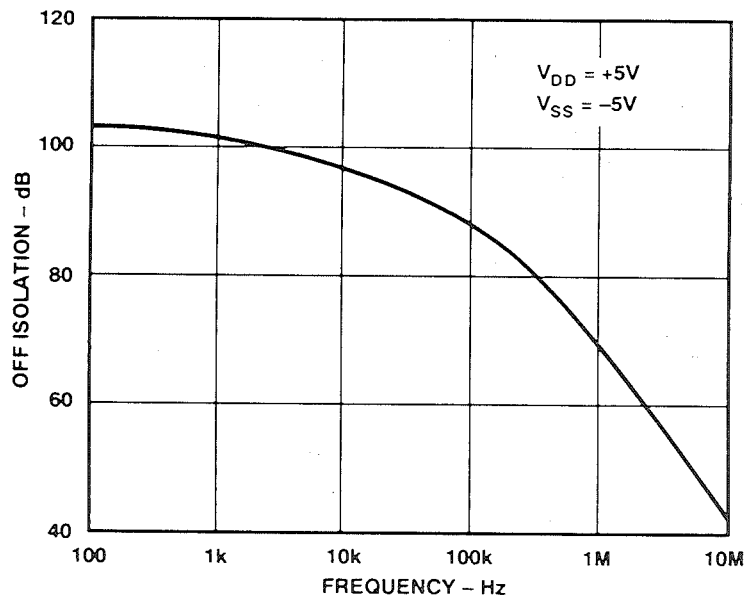


Figure 8.37

Another AC parameter that affects system performance is the charge injection that takes place during switch-

ing. Figure 8.38 shows the equivalent circuit of the charge injection mechanism.

## DYNAMIC PERFORMANCE CONSIDERATIONS: CHARGE INJECTION MODEL

- Step Waveforms of  $\pm(V_{DD} - V_{SS})$  are Applied to  $C_Q$ , the Gate Capacitance of the Output Switches

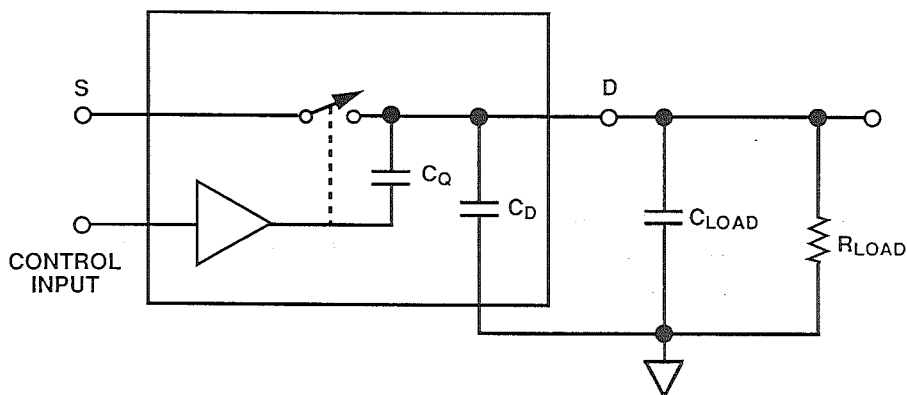


Figure 8.38

When the switch control input is asserted, it causes the control circuit to apply a large voltage change (from  $V_{DD}$  to  $V_{SS}$ , or vice versa) at the gate of the MOSFET switch. This fast change in voltage injects a charge into the switch output through the gate-drain capacitance  $C_Q$ . The amount of charge coupled depends on the gate-drain capacitance.

The charge injection introduces a step change in output voltage when switching (refer to Figure 8.39). The change in voltage is a function of the amount of charge injected, which is in turn a function of the gate-drain capacitance.

## EFFECTS OF CHARGE INJECTION

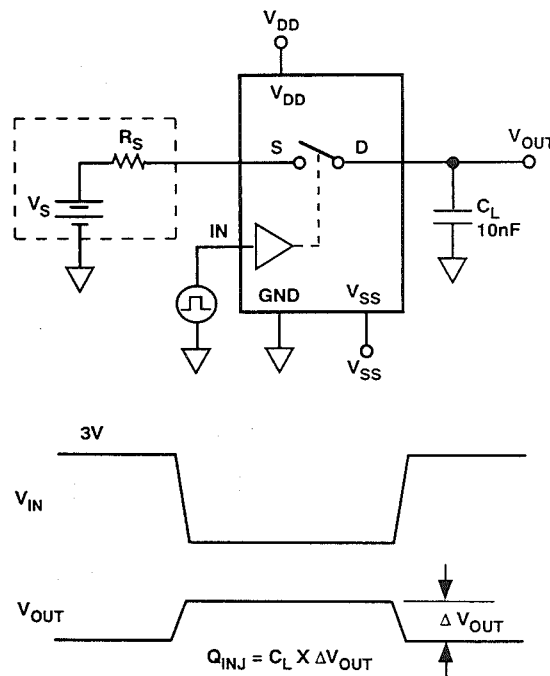


Figure 8.39

Another problem caused by switch capacitance is the retained charge, when channel switching which can

cause transients in the switch output. Figure 8.40 illustrates the phenomenon.

## CHARGE COUPLING CAUSES DYNAMIC SETTLING NOISE WHEN MULTIPLEXING SIGNALS

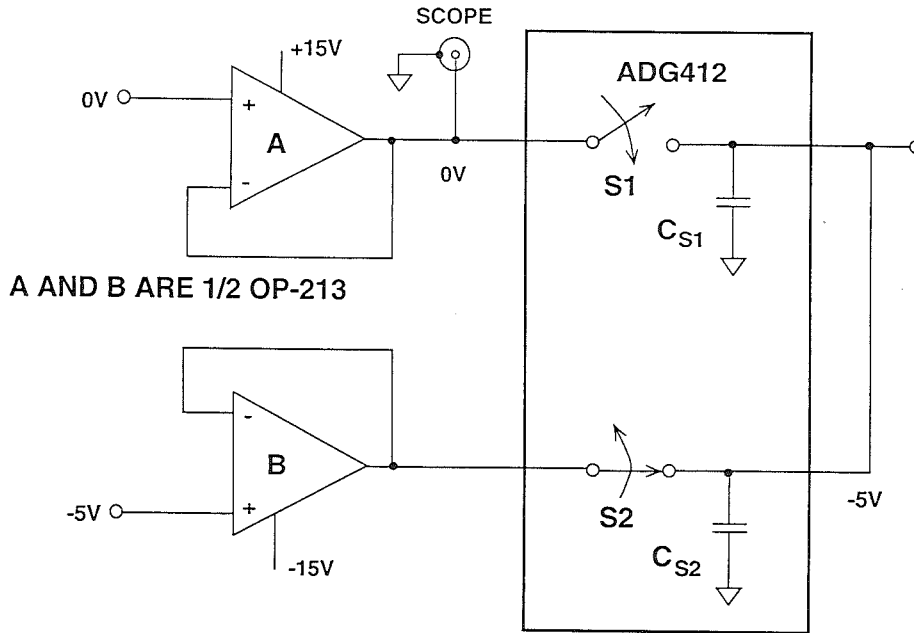


Figure 8.40

Assume that initially S2 is closed and S1 open.  $C_{S1}$  and  $C_{S2}$  are charged to -5V. As S2 opens, the -5V remains on  $C_{S1}$  and  $C_{S2}$ , as S1 closes. Thus, the output of Amplifier A sees a -5V transient. The output will not stabilize until Amplifier A's output fully discharges  $C_{S1}$  and  $C_{S2}$  and settles to 0V. The scope photo in Figure 8.41 depicts this

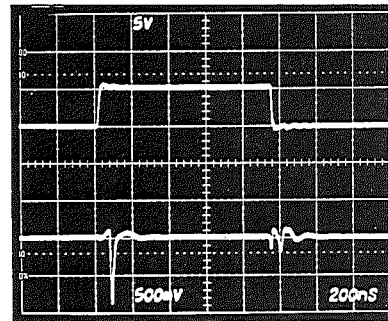
transient. The amplifier's transient load settling characteristics will be an important consideration when choosing the right device.

Crosstalk is related to the capacitances between two switches. This is the  $C_{SS}$  shown in Figure 8.42.

## OUTPUT OF OP AMP SHOWS DYNAMIC SETTLING DUE TO CHARGE COUPLING

SWITCH CONTROL  
5V/div.

AMPLIFIER A OUTPUT  
500mV/div.



HORIZONTAL SCALE: 200ns/div.

Figure 8.41

## CHANNEL-TO-CHANNEL CROSSTALK CONSIDERATION: EQUIVALENT CIRCUIT FOR ADJACENT SWITCHES

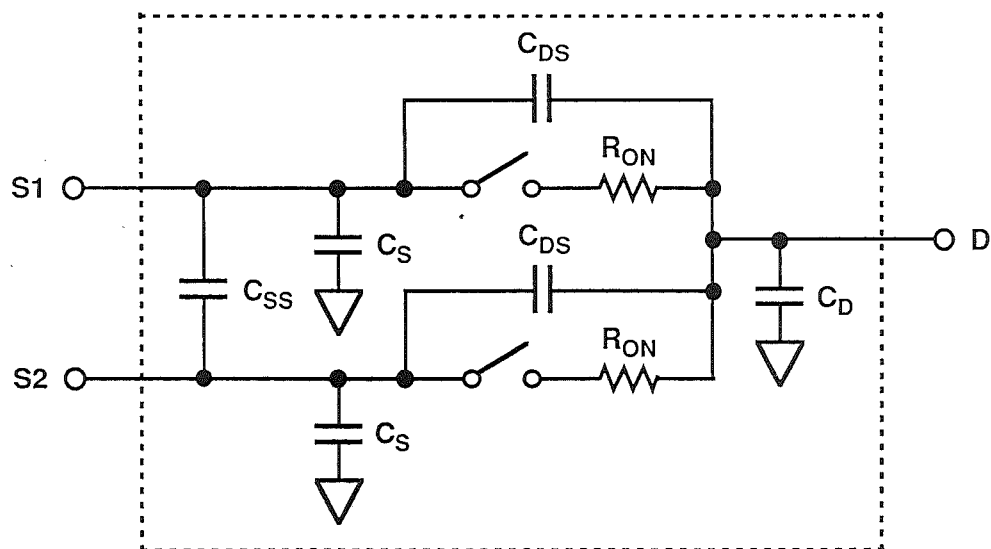


Figure 8.42



Figure 8.43 shows typical crosstalk performance of a CMOS analog switch.

8.44 shows the dynamic transfer function.

Finally, the switch itself has a settling time that must be considered. Figure

## CROSSTALK PERFORMANCE OF ADG511 SWITCH

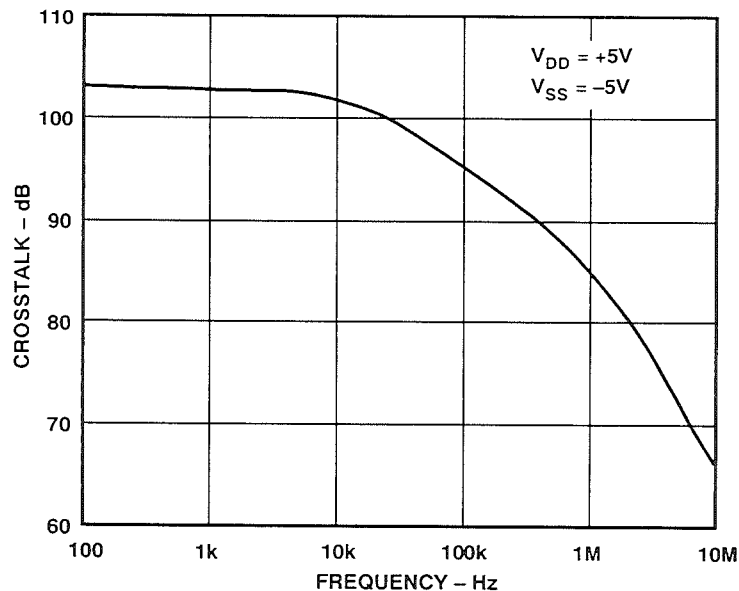
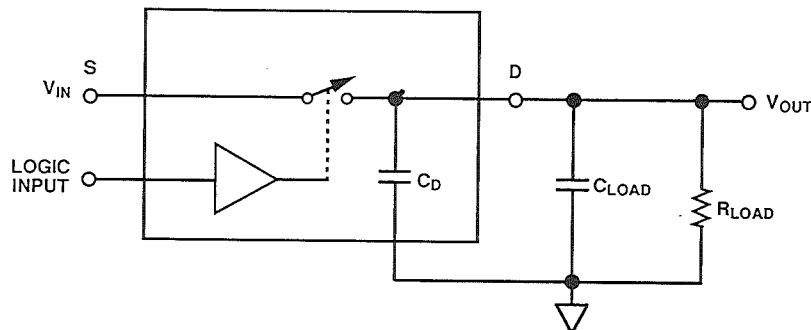


Figure 8.43

## DYNAMIC PERFORMANCE CONSIDERATIONS: SETTLING TIME

- Settling Time is the Time Required for the Switch Output Voltage to Settle to Within a Given Accuracy Band of the Final Value.



$$\text{OFF - TO - ON: } t_{\text{SETT}} = t_{\text{ON}} + \left( \frac{R_{\text{ON}} R_{\text{LOAD}}}{R_{\text{ON}} + R_{\text{LOAD}}} \right) (C_{\text{LOAD}} + C_{\text{D}}) \left( -\ln \frac{\% \text{ERROR}}{100} \right)$$

$$\text{ON - TO - OFF: } t_{\text{SETT}} = t_{\text{OFF}} + (R_{\text{LOAD}}) (C_{\text{LOAD}} + C_{\text{D}}) \left( -\ln \frac{\% \text{ERROR}}{100} \right)$$

Figure 8.44

The settling time can be calculated because the response is a function of the switch and circuit resistances and capacitances. One can assume that this

is a single-pole system and calculate the number of time constants required to settle to the desired system accuracy (Figure 8.45).

### NUMBER OF TIME CONSTANTS REQUIRED TO SETTLE TO GIVEN ACCURACY BAND

RESOLUTION	% REQUIRED FOR 1/2 LSB	# OF TIME CONSTANTS
8 Bits	0.1953	6.24
10 Bits	0.0488	7.63
12 Bits	0.0122	9.01
14 Bits	0.0031	10.38
16 Bits	0.0008	11.74
18 Bits	0.0002	13.12

Figure 8.45

## **TRENCH-ISOLATED LC<sup>2</sup>MOS ANALOG SWITCH FAMILY OFFERS MANY BENEFITS**

Analog Devices uses trench-isolation technology to produce its LC<sup>2</sup>MOS analog switches. The process reduces the latchup susceptibility of the device,

the junction capacitances, increases switching time and leakage current, and extends the analog voltage range to the supply rails.

### **ADG411/ADG511 FAMILY OF TRENCH-ISOLATED LC<sup>2</sup>MOS ANALOG SWITCHES**

- Latch-Up Proof
- Analog Signal Range to Supply Rails
- Fast Switching Times
- Break Before Make Switching
- Low ON-Resistance
- Low Leakage

**Figure 8.46**

Figure 8.47 shows the cross-sectional view of the complementary CMOS structure. The buried oxide layer and the side walls completely isolate the substrate from each transistor junction.

Therefore, no reverse-biased PN junction is formed. Consequently the bandwidth-reducing capacitances and the possibility of SCR latchup are greatly reduced.

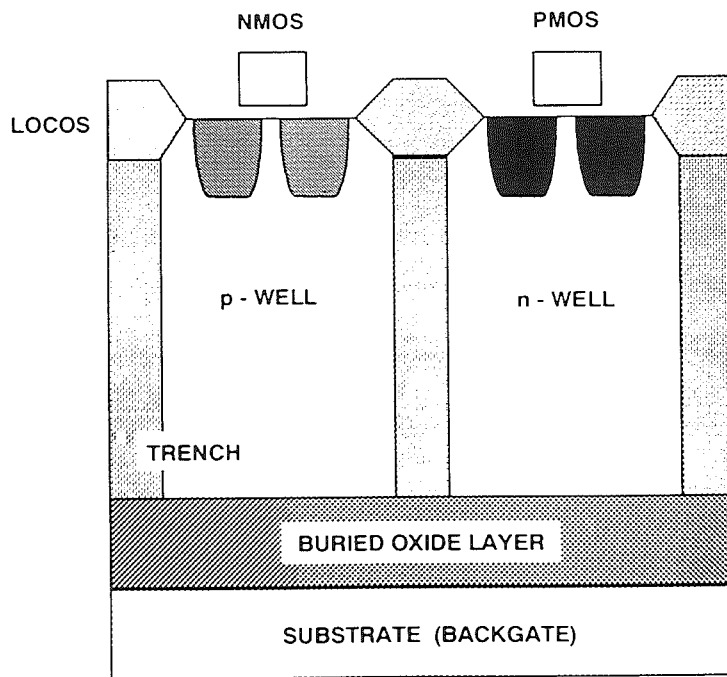
TRENCH-ISOLATION LC<sup>2</sup>MOS STRUCTURE

Figure 8.47

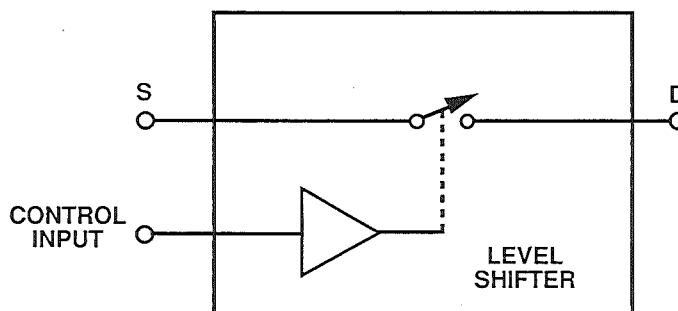
## APPLYING THE ANALOG SWITCH

Switching time is an important consideration in applying analog switches, but switching time should not be confused with settling time. ON and OFF times are simply a measure of the propaga-

tion delay from the control input to the toggling of the switch, and are largely caused by time delays in the drive and level-shift circuits.

### APPLYING THE ANALOG SWITCH: DYNAMIC PERFORMANCE CONSIDERATIONS

- $t_{on}$  and  $t_{off}$  should not be confused with settling time.



- $t_{on}$  and  $t_{off}$  are simply a measure of the propagation delay from control input to operation of the analog switch. It is caused by time delays in the drive / level-shifter logic circuitry.

Figure 8.48

When a CMOS multiplexer switches inputs to an inverting summing amplifier, it should be noted that the ON-resistance, and its nonlinear change as a function of input voltage, will cause errors (refer to Figure 8.49). If the

resistors are large, the switch leakage current may introduce error. Small resistors minimize leakage current error but increase the error due to the finite value of  $R_{ON}$ .

## APPLYING THE ANALOG SWITCH: UNITY GAIN INVERTER WITH SWITCHED INPUT

- Problem: Effect of  $\Delta R_{ON}$  versus  $\Delta V_S$  on Circuit Linearity.
- $R_{ON}$  variation due to  $\Delta V_{IN}$  degrades linearity of  $V_{OUT}$  relative to  $V_{IN}$

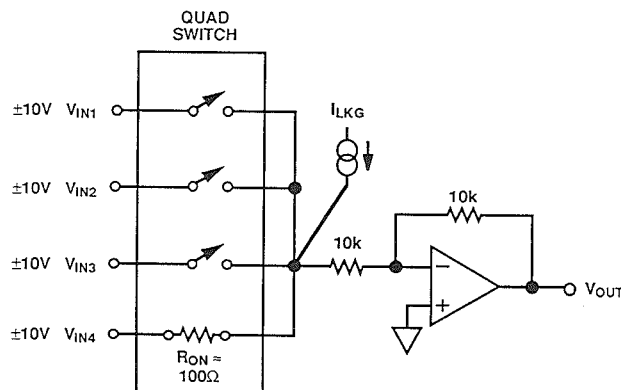


Figure 8.49

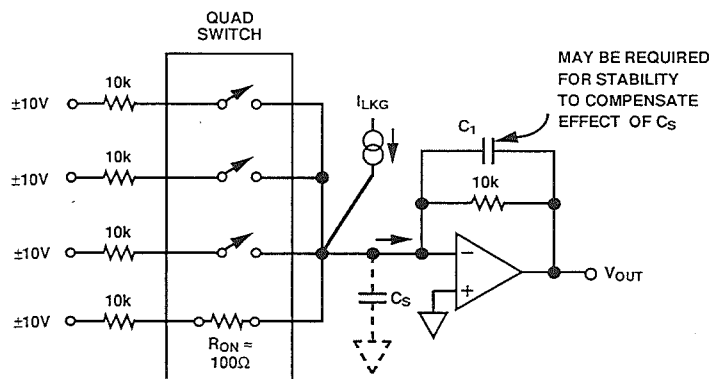
To minimize the effect of  $R_{ON}$  change due to the change in input voltage, it is advisable to put the multiplexing switches at the op amp summing junction as shown in Figure 8.50. This ensures the switches are only modulated with about  $\pm 100\text{mV}$  rather than the full  $\pm 10\text{V}$  - but a resistor is required for each input leg.

It is important to know how much parasitic capacitance has been added to the summing junction as a result of adding a multiplexer, because any capacitance added to that node intro-

duces phase shift to the amplifier closed loop response. If the capacitance is too large, the amplifier may become unstable and oscillate. A small capacitance,  $C1$ , across the feedback resistor may be required to stabilize the circuit.

The finite value of  $R_{ON}$  is a significant error source. The gain-set resistors should be at least 1,000 times larger than the switch ON-resistance to guarantee 0.1% gain accuracy. Higher values yield greater accuracy, but the proper selection of  $C1$  is critical to maintain stability.

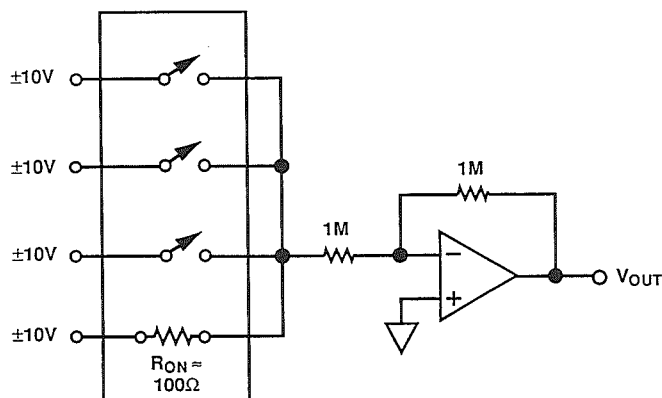
## APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $\Delta V_S$ (AND THUS $\Delta R_{ON}$ )



- Connecting the Switch at the Summing Point
- The switch only sees  $\pm 100mV$ , not  $\pm 10V$ .  $R_{ON}$  variation is minimized, and  $V_{OUT}$  accuracy is improved.

Figure 8.50

## APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $\Delta V_S$ (AND THUS $\Delta R_{ON}$ )



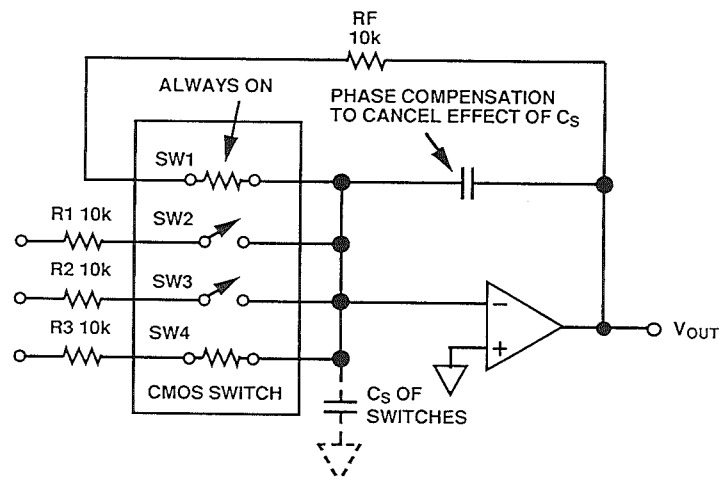
- Using Larger Values of Resistance
- $R_{ON}$  Variation due to Input Signal is Small Compared to the  $1M\Omega$  Switch Load. Effect on Transfer Accuracy is Minimized.
- Bias Current and Leakage are now very important

Figure 8.51

A better method of compensating for  $R_{ON}$  is to place one of the switches in series with the feedback resistor of the inverting amplifier as shown in Figure 8.52. It is a safe assumption that the multiple switches, fabricated on a single

chip, are well-matched in absolute characteristics and tracking over temperature. Therefore, the amplifier is closed-loop gain stable at unity gain, since the total feedforward and feedback resistors are matched.

### APPLYING THE ANALOG SWITCH: MINIMIZING THE INFLUENCE OF $R_{ON}$ AND $\Delta R_{ON}$ VERSUS TEMPERATURE ON CIRCUIT ACCURACY



- Switch in Series With Feedback Resistor Compensates for Gain Error.

Figure 8.52

The best multiplexer drives the non-inverting input of the amplifier. The high input impedance of the non-inverting input eliminates the errors due to  $R_{ON}$ . (Figure 8.53)

When multiplexing signals into an ADC, particularly the successive-approximation (SAR) type, it is advisable to place a buffer between the switch

output and the input of the converter. The transient currents at the ADC input produced by the conversion process (DAC switching) are absorbed by a drive amplifier of sufficiently low output impedance and high bandwidth. Driving the ADC directly with the switches will produce significant conversion errors due to the finite  $R_{ON}$  resistance.

**APPLYING THE ANALOG SWITCH:  
MINIMIZING THE INFLUENCE OF  $\Delta V_S$  (AND THUS  $\Delta R_{ON}$ )  
NON-INVERTING SOLUTION**

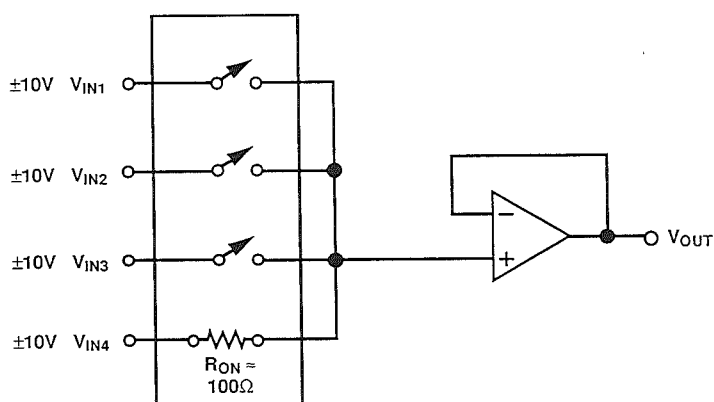


Figure 8.53

**APPLYING THE ANALOG SWITCH:  
BUFFER THE MUX OUTPUT INTO SAR-TYPE  
ADC TO MINIMIZE GAIN ERROR**

8

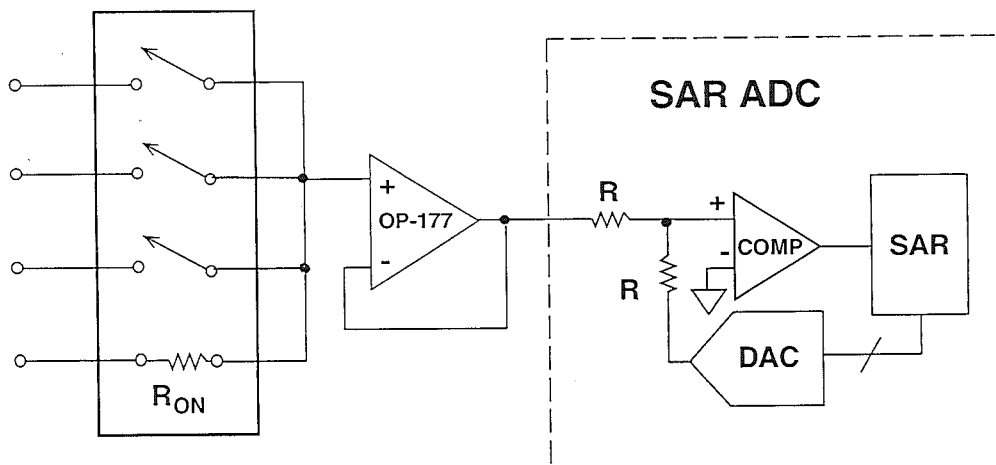


Figure 8.54



## SAMPLE AND HOLD CIRCUITS

*Walt Kester, James Bryant*

The *sample and hold amplifier*, or SHA, is a critical part of many data acquisition systems. It captures an analog signal and holds it during some operation (most commonly analog-digital conversion). The circuitry involved is demanding, and unexpected properties of commonplace components such as capacitors and printed circuit boards may degrade SHA performance.

When the sample-and-hold is in the sample mode, the output follows the input with only a small voltage offset. There do exist SHAs where the output during the *sample* mode does not follow the input accurately, and the output is only accurate during the *hold* period. An example is the AD871. These will not be considered here. Strictly speaking, a sample and hold with good tracking performance should be referred to as a *track and hold* circuit, but in practice the terms are used interchangeably.

In the past, the commonest application of a SHA was to maintain the input to an ADC at a constant value during conversion (with many, but not all,

types of ADC the input may not change by more than 1 LSB during conversion lest the process be corrupted - this either sets very low input frequency limits on such ADCs, or requires that they be used with a SHA to hold the input during each conversion). Today, high density IC processes allow the manufacture of ADCs containing an integral SHA. Wherever possible ADCs with integral SHA (often known as *sampling* ADCs) should be used in preference to separate ADCs and SHAs. The advantage of such a sampling ADC, apart from the obvious ones of smaller size, lower cost, and fewer external components, is that the overall performance is specified, and the designer need not spend time ensuring that there are no specification, interface, or timing issues involved in combining a discrete ADC and a discrete SHA.

Although the largest application of SHAs is driving ADCs, they are also used in DAC deglitchers, peak detectors, analog delay circuits, simultaneous sampling systems, and data distribution systems.

## SAMPLE-AND-HOLD AMPLIFIERS (SHAs)

- Two States of Operation:
  - ◆ *Sample* (or *Track*) the input signal
  - ◆ *Hold* the input signal at the value it has at the instant the Hold Command is asserted
- The terms *Sample-and-Hold* and *Track-and-Hold* are used interchangeably, but some SHAs have degraded track mode performance
- Applications:
  - ◆ Driving ADCs (Holding the signal constant during the conversion process)
  - ◆ Sampling ADCs (on-chip SHA)
  - ◆ DAC Deglitchers
  - ◆ Peak Detectors
  - ◆ Data Acquisition and Distribution Systems

Figure 8.55

## BASIC SHA OPERATION

Regardless of the circuit details or type of SHA in question, all such devices have four major components. The input amplifier, energy storage device (capacitor), output buffer, and switching circuits are common to all SHAs as shown in the typical configuration of Figure 8.56.

The energy-storage device, the heart of the SHA, is almost always a capacitor. The input amplifier buffers the input by presenting a high impedance to the signal source and providing current gain to charge the hold capacitor. In the

*track* mode, the voltage on the hold capacitor follows (or tracks) the input signal (with some delay and bandwidth limiting). In the *hold* mode, the switch is opened, and the capacitor retains the voltage present before it was disconnected from the input buffer. The output buffer offers a high impedance to the hold capacitor to keep the held voltage from discharging prematurely. The switching circuit and its driver form the mechanism by which the SHA is alternately switched between track and hold.

## BASIC SAMPLE-AND-HOLD CIRCUIT

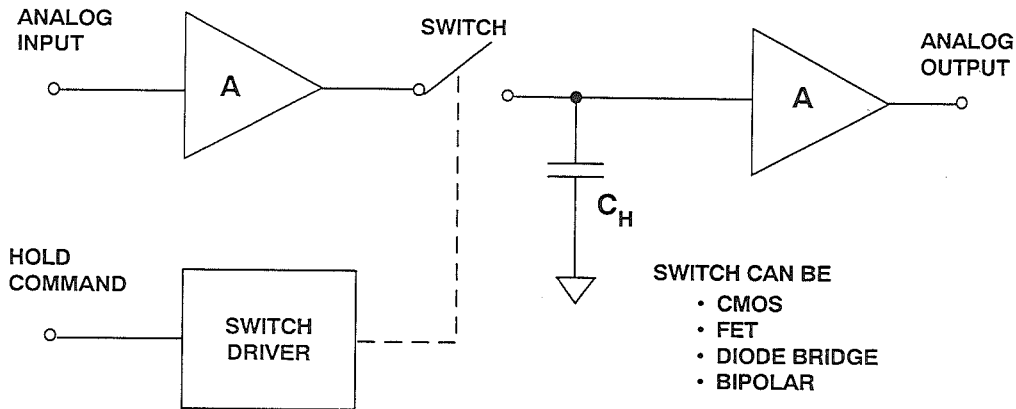


Figure 8.56

There are four groups of specifications that describe basic SHA operation: track mode, track-to-hold transition, hold mode, hold-to-track transition. These specifications are summarized in Figure 8.57, and some of the SHA error

sources are shown in Figure 8.58. Because there are both DC and AC performance implications for each of the four modes, properly specifying a SHA and understanding its operation in a system is a complex matter.

## SAMPLE-AND-HOLD SPECIFICATIONS

SAMPLE MODE	SAMPLE-TO-HOLD TRANSITION	HOLD MODE	HOLD-TO-SAMPLE TRANSITION
<b>STATIC:</b> ♦ Offset ♦ Gain Error ♦ Nonlinearity	<b>STATIC:</b> ♦ Pedestal ♦ Pedestal Nonlinearity	<b>STATIC:</b> ♦ Droop ♦ Dielectric Absorption	
<b>DYNAMIC:</b> ♦ Settling Time ♦ Bandwidth ♦ Slew Rate ♦ Distortion ♦ Noise	<b>DYNAMIC:</b> ♦ Aperture Delay Time ♦ Aperture Jitter ♦ Switching Transient ♦ Settling Time	<b>DYNAMIC:</b> ♦ Feedthrough ♦ Distortion ♦ Noise	<b>DYNAMIC:</b> ♦ Acquisition Time ♦ Switching Transient

Figure 8.57

## SOME SOURCES OF ERROR IN A SAMPLE-AND-HOLD

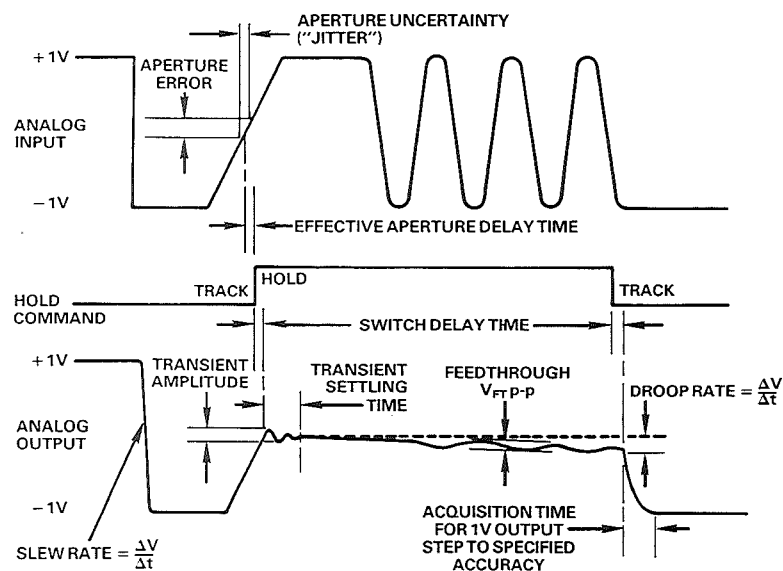


Figure 8.58

## TRACK MODE SPECIFICATIONS

Since a SHA in the sample (or track) mode is simply an amplifier, both the static and dynamic specifications in this mode are similar to those of any amplifier. (SHAs which have degraded performance in the track mode are generally only specified in the hold mode.) The principle track mode specifications are

*offset, gain, nonlinearity, bandwidth, slew rate, settling time, distortion, and noise*, however distortion and noise in the track mode are often of less interest than in the hold mode. Fundamental amplifier specifications are discussed in detail in Section 1 and will not be repeated here.

## TRACK-TO-HOLD MODE SPECIFICATIONS

When the SHA switches from track to hold, there is generally a small amount of charge dumped on the hold capacitor because of non-ideal switches. This results in a hold mode DC offset voltage which is called *pedestal* error. If the SHA is driving an ADC, the pedestal

error appears as a DC offset voltage which may be removed by performing a system calibration. If the pedestal error is a function of input signal level, the resulting nonlinearity contributes to hold mode distortion.

### TRACK-TO-HOLD MODE PEDESTAL, TRANSIENT, AND SETTLING TIME ERRORS

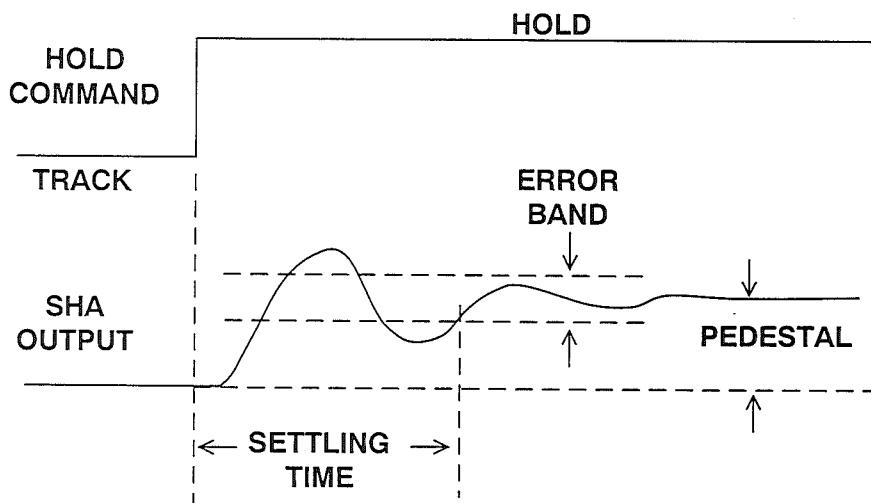


Figure 8.59

Pedestal errors may be reduced by increasing the value of the hold capacitor with a corresponding increase in acquisition time and a reduction in bandwidth and slew rate.

Switching from track to hold produces a transient, and the time required for the SHA output to settle to within a specified error band is called *hold mode settling time*. Occasionally, the peak amplitude of the switching transient is also specified.

Perhaps the most misunderstood and misused SHA specifications are those that include the word *aperture*. The most essential dynamic property of a SHA is its ability to disconnect quickly the hold capacitor from the input buffer amplifier. The short (but non-zero) interval required for this action is called

*aperture time*. The actual value of the voltage that gets held at the end of this interval is a function of both the input signal and the errors introduced by the switching operation itself. Figure 8.61 shows what happens when the hold command is applied with an input signal of arbitrary slope (for clarity, the sample to hold pedestal and switching transients are ignored). The value that finally gets held is a delayed version of the input signal, averaged over the aperture time of the switch as shown in Figure 8.61. The first-order model assumes that the final value of the voltage on the hold capacitor is approximately equal to the average value of the signal applied to the switch over the interval during which the switch changes from a low to high impedance ( $t_a$ ).

## SHA CIRCUIT SHOWING INTERNAL TIMING

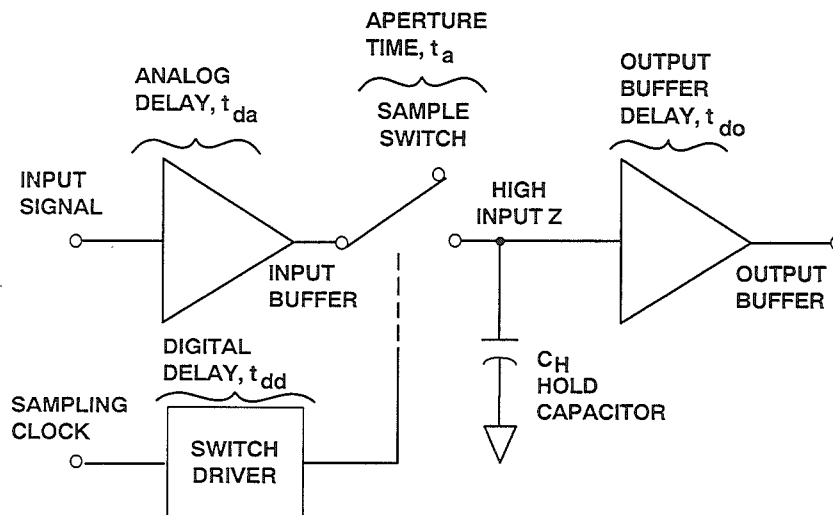


Figure 8.60

# SHA WAVEFORMS

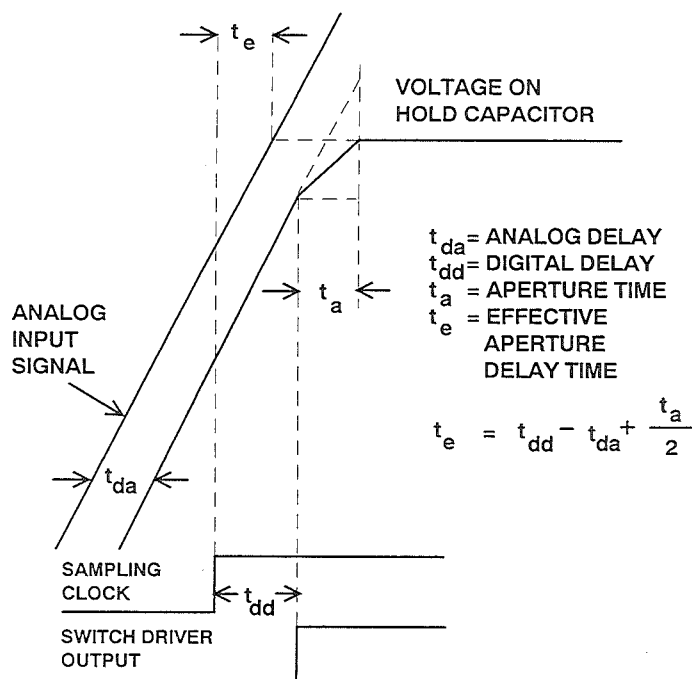


Figure 8.61

The model shows that the finite time required for the switch to open ( $t_a$ ) is equivalent to introducing a small delay in the sampling clock driving the SHA. This delay is constant and may either be positive or negative. It is called *effective aperture delay time*, *aperture delay time*, or simply *aperture delay*, ( $t_e$ ) and is defined as the time difference between the analog propagation delay of the front-end buffer ( $t_{da}$ ) and the switch digital delay ( $t_{dd}$ ) plus one-half the aperture time ( $t_a/2$ ). The effective aperture delay time is usually positive, but may be negative if the sum of one-half the aperture time ( $t_a/2$ ) and the switch digital delay ( $t_{dd}$ ) is less than

the propagation delay through the input buffer ( $t_{da}$ ). The aperture delay specification thus establishes when the input signal is actually sampled with respect to the sampling clock edge.

Aperture delay time can be measured by applying a bipolar sinewave signal to the SHA and adjusting the synchronous sampling clock delay such that the output of the SHA is zero during the hold time. The relative delay between the input sampling clock edge and the actual zero-crossing of the input sinewave is the aperture delay time (see Figure 8.62).

## MEASURING EFFECTIVE APERTURE DELAY TIME

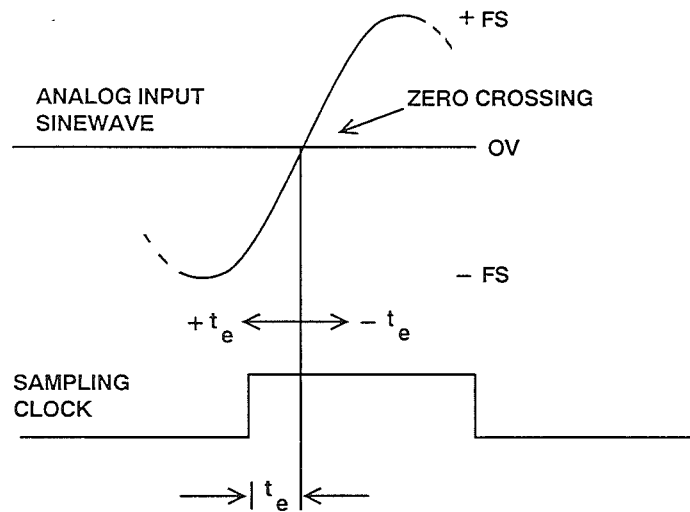


Figure 8.62

Aperture delay produces no errors, but acts as a fixed delay in either the sampling clock input or the analog input (depending on its sign). If there is sample-to-sample variation in aperture delay (*aperture jitter*), then a corresponding voltage error is produced as shown in Figure 8.63. This sample-to-sample variation in the instant the

switch opens is called *aperture uncertainty*, or *aperture jitter* and is usually measured in rms picoseconds. The amplitude of the associated output error is related to the rate-of-change of the analog input. For any given value of aperture jitter, the aperture jitter error increases as the input  $dv/dt$  increases.



## EFFECTS OF APERTURE JITTER ON SHA OUTPUT

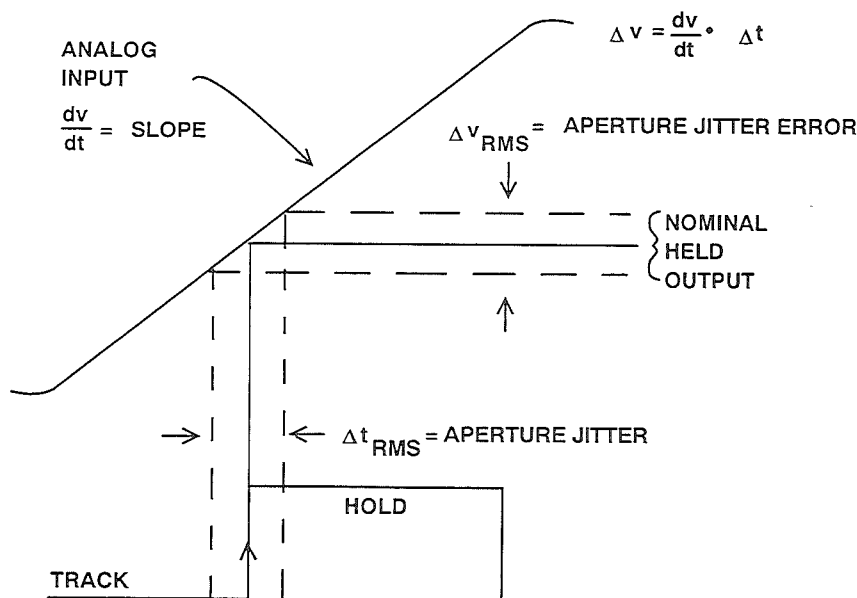


Figure 8.63

Measuring aperture jitter error in a SHA requires a jitter-free sampling clock and analog input signal source, because jitter (or phase noise) on either signal cannot be distinguished from the SHA aperture jitter itself - the effects are the same. In fact, the largest source of timing jitter errors in a system is most often external to the SHA (or the ADC if it is a sampling one) and is caused by noisy or unstable clocks, improper signal routing, and lack of attention to good grounding and

decoupling techniques. SHA aperture jitter is generally less than 50ps rms, and less than 5ps rms in high speed devices.

Figure 8.64 shows the effects of total sampling clock jitter on the signal-to-noise ratio (SNR) of a sampled data system. The total rms jitter will be composed of a number of components, the actual SHA aperture jitter often being the least of them.

## EFFECTS OF SAMPLING CLOCK JITTER ON SNR

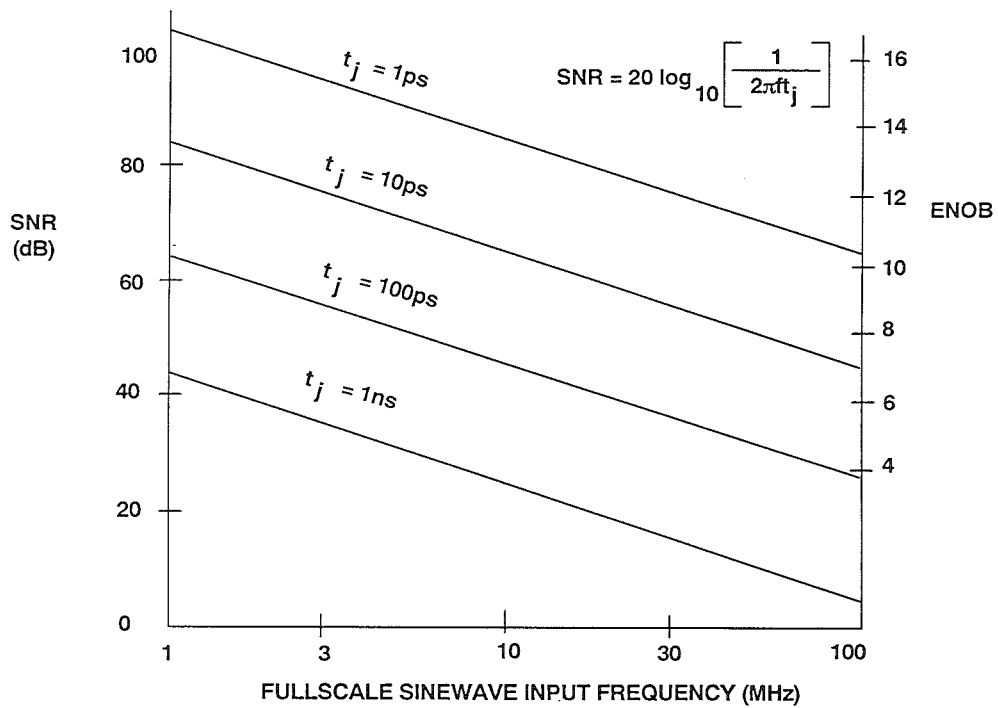


Figure 8.64

## HOLD MODE SPECIFICATIONS

During the hold mode there are errors due to imperfections in the hold capacitor, switch, and output amplifier. If a leakage current flows in or out of the hold capacitor, it will slowly charge or discharge, and its voltage will change. This effect is known as *droop* in the SHA output and is expressed in  $\text{V}/\mu\text{s}$ . Droop can be caused by leakage across a dirty PCB if an external capacitor is used, or by a leaky capacitor, but is most usually due to leakage current in semiconductor switches and the bias current of the output buffer amplifier. An acceptable value of droop is where

the output of a SHA does not change by more than  $1/2$  LSB during the conversion time of the ADC it is driving. Where droop is due to leakage current in reversed biased junctions (switches or FET amplifier gates), it will double for every  $10^\circ\text{C}$  increase in chip temperature - which means that it will increase a thousand fold between  $+25^\circ\text{C}$  and  $+125^\circ\text{C}$ . Droop can be reduced by increasing the value of the hold capacitor, but this will also increase acquisition time and reduce bandwidth in the track mode.

## HOLD MODE DROOP

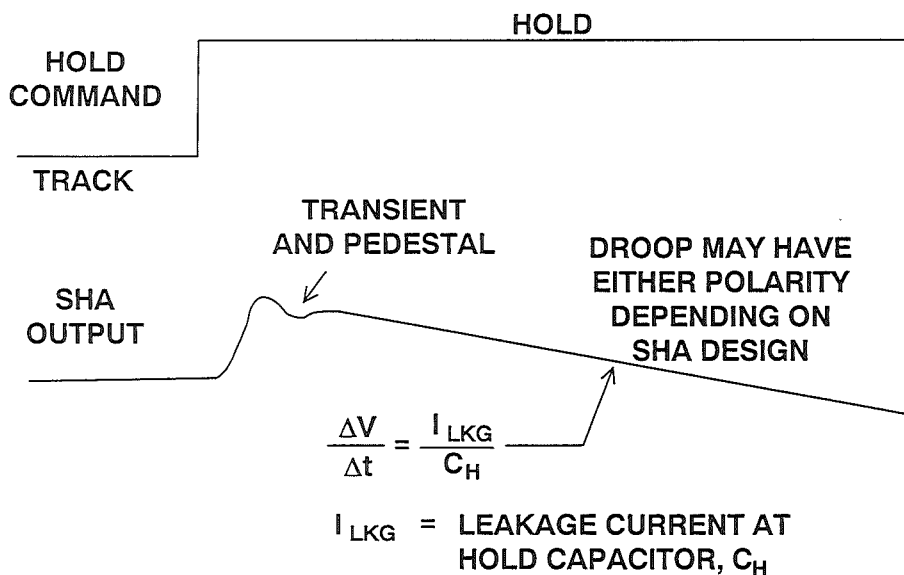
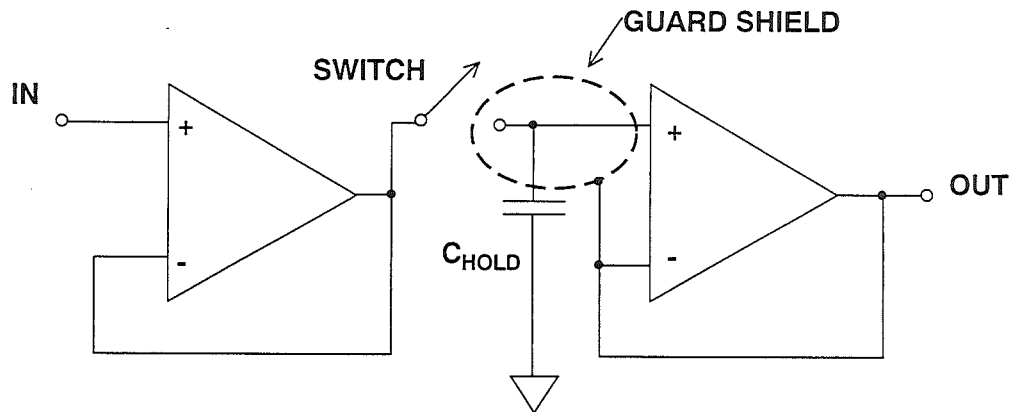


Figure 8.65

Even quite small leakage currents can cause troublesome droop when SHAs use small hold capacitors. Leakage currents in PCBs may be minimized by the intelligent use of guard rings. A guard ring is a ring of conductor which surrounds a sensitive node and is at the same potential. Since there is no voltage between them, there can be no leakage current flow. In a non-inverting application, such as is shown in Figure

8.66, the guard ring must be driven to the correct potential, whereas the guard ring on a virtual ground can be at actual ground potential (Figure 8.67). The surface resistance of PCB material is much lower than its bulk resistance, so guard rings must always be placed on both sides of a PCB - and on multi-layer boards, guard rings should be present in all layers.

## DRIVE THE GUARD SHIELD WITH THE SAME VOLTAGE AS THE HOLD CAPACITOR TO REDUCE BOARD LEAKAGE



Note: Be Sure a Guard Shield is in Each Layer of the PCB

Figure 8.66

## USING A GUARD SHIELD ON A VIRTUAL GROUND SHA DESIGN

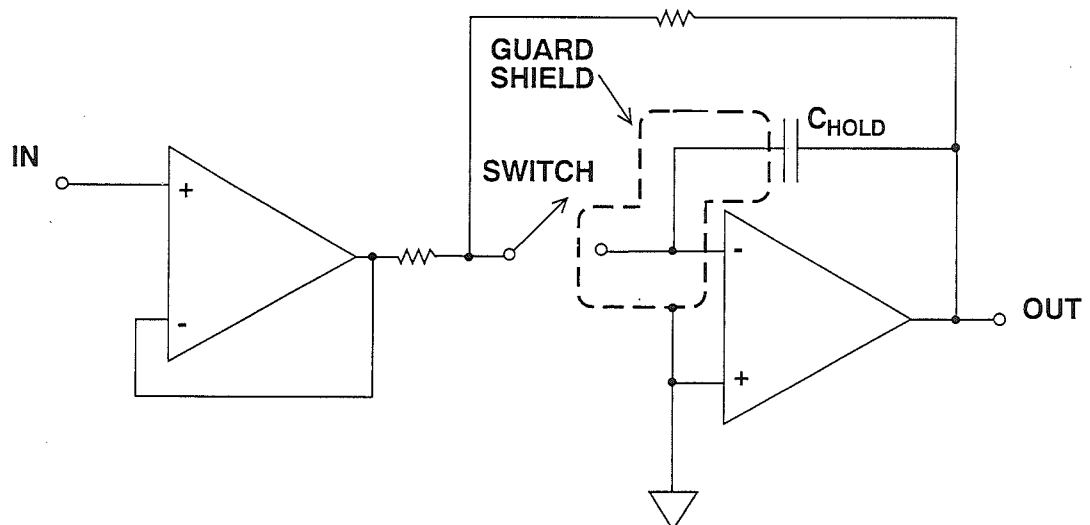


Figure 8.67

Hold capacitors for SHAs must have low leakage, but there is another characteristic which is equally important: low *dielectric absorption*. If a capacitor is charged, then discharged, and then left open circuit, it will recover some of its charge. The phenomenon is known as

*dielectric absorption*, and it can seriously degrade the performance of a SHA, since it causes the remains of a previous sample to contaminate a new one, and may introduce random errors of tens or even hundreds of mV.

## DIELECTRIC ABSORPTION

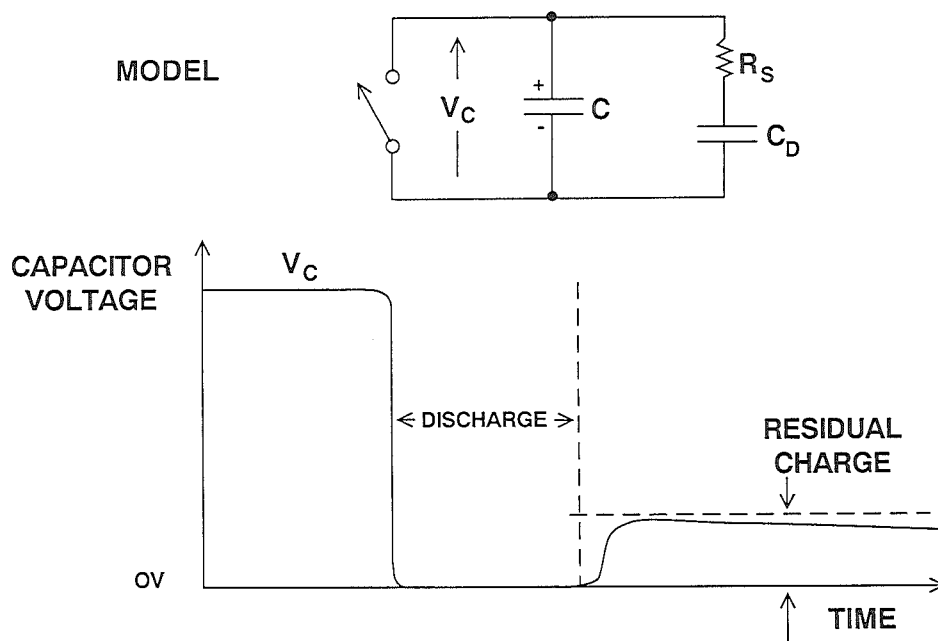


Figure 8.68

Different capacitor materials have differing amounts of dielectric absorption - electrolytic capacitors are dreadful (their leakage is also high), and some high-K ceramic types are bad, while mica, polystyrene and polypropylene are generally good. Unfortunately, dielectric absorption varies from batch to batch, and even occasional batches of

polystyrene and polypropylene capacitors may be affected. It is therefore wise to pay 30-50% extra when buying capacitors for SHA applications and buy devices which are guaranteed by their manufacturers to have low dielectric absorption, rather than types which might generally be expected to have it.

## THE CHOICE OF HOLD CAPACITOR AFFECTS ACCURACY

■ **Must Have:** Low Leakage and Low Dielectric Absorption

■ **Best:**

- ↑ Polystyrene
- ↑ Polypropylene
- ↑ Teflon
- ↑ Polycarbonate

■ **Worst:**

- ↓ Mylar
- ↓ Glass
- ↓ Electrolytic

Figure 8.69

Stray capacity in a SHA may allow a small amount of the AC input to be coupled to the output during hold. This effect is known as *feedthrough* and is dependent on input frequency and amplitude. If the amplitude of the feedthrough to the output of the SHA is more than 1/2 LSB, then the ADC is subject to conversion errors.

In many SHAs, distortion is specified only in the track mode. The *track mode distortion* is often much better than *hold mode distortion*. Track mode distortion does not include nonlinearities due to the switch net-

work, and may not be indicative of the SHA performance when driving an ADC. Modern SHAs, especially high speed ones, specify distortion in both modes. While track mode distortion can be measured using an analog spectrum analyzer, hold mode distortion measurements must be performed using digital techniques as shown in Figure 8.70. A spectrally pure sinewave is applied to the SHA, and a low distortion high speed ADC digitizes the SHA output near the end of the hold time. An FFT analysis is performed on the ADC output, and the distortion components computed.

## MEASURING HOLD MODE DISTORTION

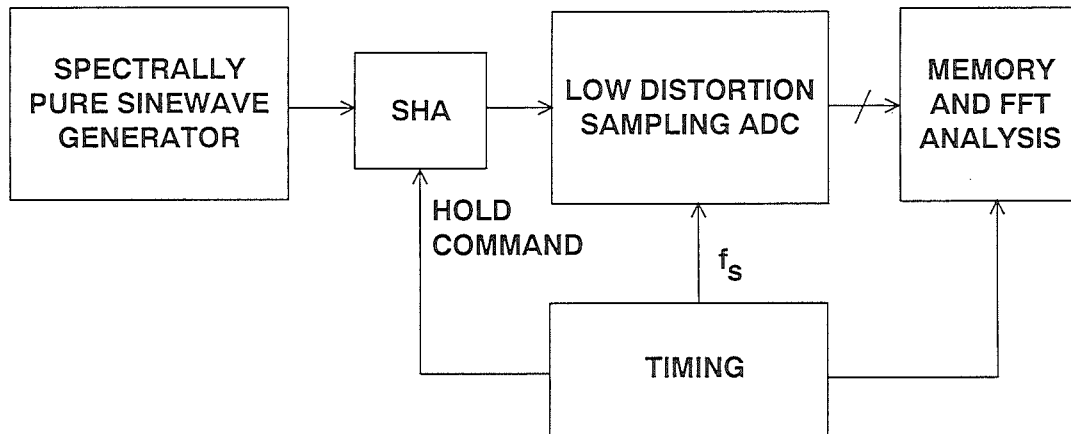


Figure 8.70

SHA *noise* in the track mode is specified and measured like that of an amplifier. Peak-to-peak *hold mode noise* is measured with an oscilloscope and converted to an rms value by dividing by 6. Hold mode noise may be given as a spectral density in nV/ $\sqrt{\text{Hz}}$ , or as an rms

value over a specified bandwidth. Unless otherwise indicated, the hold mode noise must be combined with the track mode noise to yield the total output noise. Some SHAs specify the total output hold mode noise, in which case the track mode noise is included.

## HOLD TO TRACK TRANSITION SPECIFICATIONS

When the SHA switches from hold to track, it must reacquire the input signal (which may have made a full scale transition during the hold mode). *Acquisition time* is the interval of time required for the SHA to reacquire the signal to the desired accuracy when switching from hold to track. The interval starts at the 50% point of the sampling clock edge, and ends when the SHA output voltage falls within the specified error band (usually 0.1% and 0.01% times are given). Some SHAs also specify acquisition time with respect to the voltage on the hold capacitor, neglecting the delay and settling time of the output buffer. The hold capacitor acquisition time specification

is applicable in high speed applications, where the maximum possible time must be allocated for the hold mode. The output buffer settling time must of course be significantly smaller than the hold time.

Acquisition time can be measured directly using certain sampling scope plug-ins which are insensitive to large overdrives. Figure 8.71 shows the hold capacitor acquisition time and the output acquisition time for the AD9100 30MSPS low distortion SHA. Typical acquisition time (measured at the hold capacitor) is 13ns to 0.1% and 16ns to 0.01% for a 2V step.

### ACQUISITION TIME MEASUREMENTS ON THE AD9100 30MSPS SHA

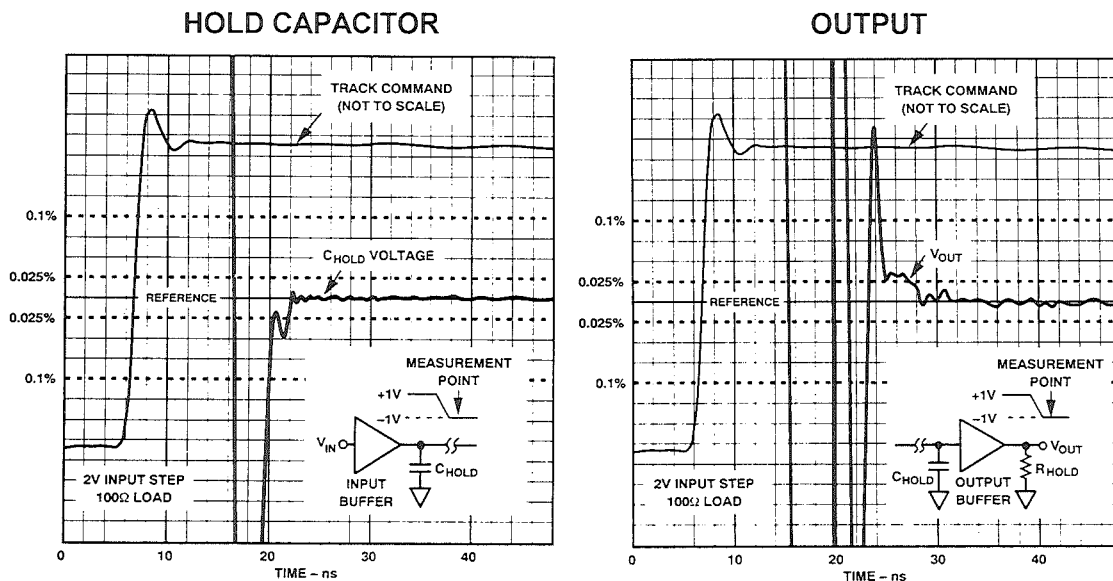


Figure 8.71



## SHA ARCHITECTURES

As with op-amps, there are numerous SHA architectures, and we will examine a few of the most popular ones. The simplest SHA structure is shown in Figure 8.72. The input signal is buffered by an amplifier and applied to the switch. The input buffer may either be open- or closed-loop and may or may not provide gain. The switch can be CMOS, FET, or bipolar (using diodes or transis-

tors) and is controlled by the switch driver circuit. The signal on the hold capacitor is buffered by an output amplifier. This architecture is sometimes referred to as *open-loop* because the switch is not inside a feedback loop. Notice that the entire signal voltage is applied to the switch, therefore it must have excellent common-mode characteristics.

### OPEN-LOOP SHA ARCHITECTURE

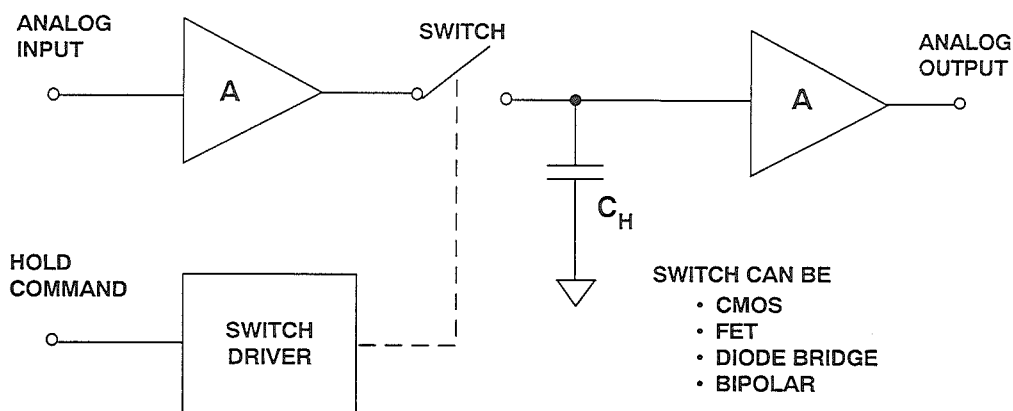


Figure 8.72

An implementation of this architecture is shown in Figure 8.73, where a diode bridge is used for the switch. Reversing the bridge drive currents reverse biases the bridge, and feedback from the

output to the bridge minimizes common-mode errors. This circuit is extremely fast, especially if the input and output buffers are open-loop followers and the diodes are Schottky ones.

## OPEN-LOOP DIODE BRIDGE SHA

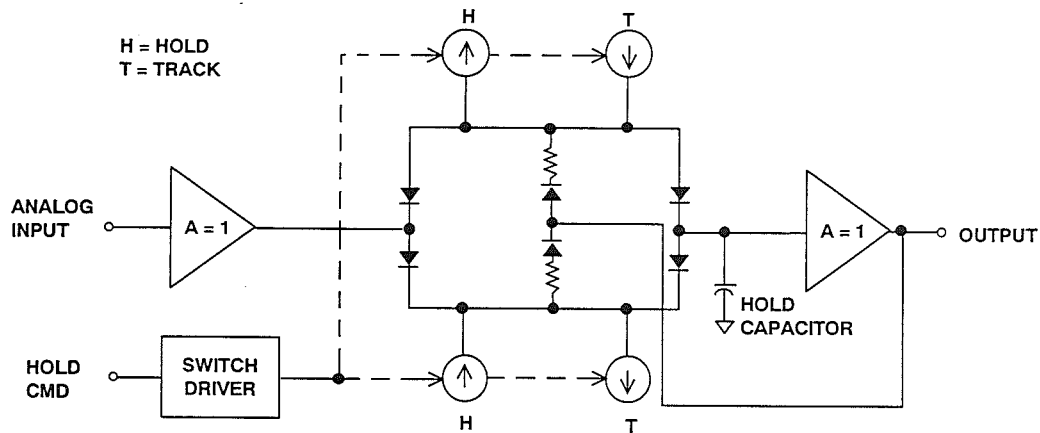


Figure 8.73

The SHA circuit shown in Figure 8.74 represents a classical *closed-loop* design and is used in many CMOS sampling ADCs. Since the switches always operate at virtual ground, there is no common-mode signal across them. Switch S2 is required in order to maintain a constant input impedance and prevent the input signal from coupling to the

output during the hold time. In the track mode, the transfer characteristic of the SHA is determined by the op-amp, and the switches do not introduce DC errors because they are within the feedback loop. The effects of charge injection can be minimized by using the differential switching techniques shown in Figure 8.75.

## CLOSED-LOOP SHA BASED ON INVERTING INTEGRATOR SWITCHED AT THE SUMMING POINT

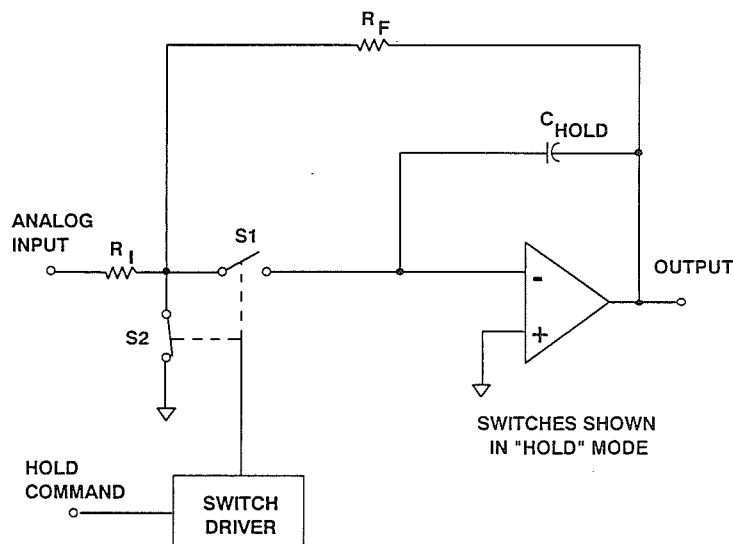


Figure 8.74

## DIFFERENTIAL SWITCHING REDUCES CHARGE INJECTION

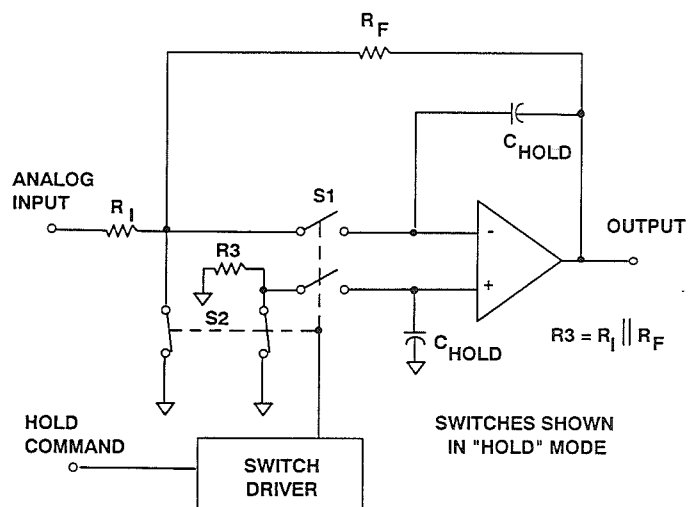


Figure 8.75

High speed sampling ADCs require fast SHAs that have low distortion and good DC characteristics. The architecture shown in Figure 8.76 utilizes closed-loop techniques on a high speed complementary-bipolar process to achieve better than 12-bit AC and DC performance. In the track mode, S1 applies the buffered input signal to the hold capacitor, and S2 provides negative feedback to the input buffer. In the hold mode, both switches are disconnected

from the hold capacitor, and negative feedback to the input buffer is supplied by S1. This architecture is implemented in SHAs such as the AD9100 and AD9101 and provides extremely low hold mode distortion by maintaining high loop gains at high frequency. The output buffer may be configured to provide voltage gain, which allows the switches to operate on lower common-mode voltage, thereby giving lower overall distortion.

### CLOSED-LOOP SHA ARCHITECTURE PROVIDES LOW DISTORTION AND HIGH SPEED (AD9100, AD9101)

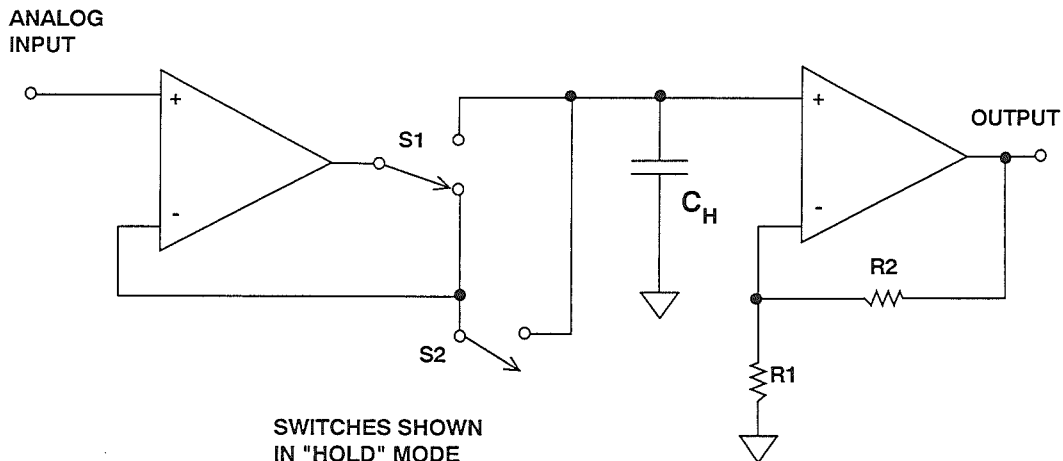


Figure 8.76

# SHA APPLICATIONS

By far the largest application of SHAs is driving ADCs. Most modern ADCs designed for signal processing are sampling ones and contain an internal SHA optimized for the converter design. Sampling ADCs are completely specified for both DC and AC performance and should be used in lieu of discrete SHA/

ADC combinations wherever possible. In a few cases, especially those requiring wide dynamic range and low distortion, there are advantages to using a discrete combination. This complex subject is discussed in more detail in Section 4 and involves many tradeoffs.

## THE ADDITION OF AN EXTERNAL WIDEBAND LOW DISTORTION SHA EXTENDS THE LOW FREQUENCY PERFORMANCE OF AN ADC TO HIGHER FREQUENCIES

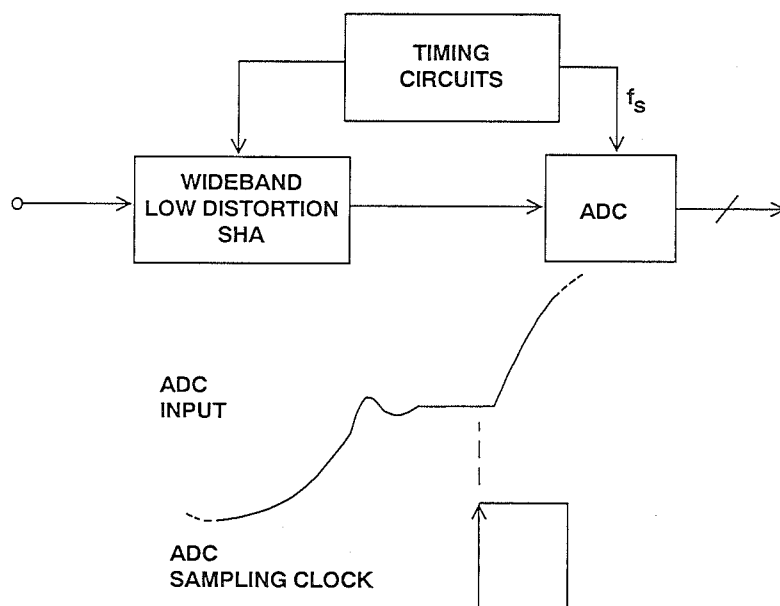


Figure 8.77

A similar application uses a low distortion SHA to minimize the effects of code-dependent DAC glitches as shown in Figure 8.78. Just prior to latching new data into the DAC, the SHA is put into the hold mode so that the DAC switching glitches are isolated from the output. The switching transients produced by the SHA are not code-depen-

dent, occur at the update frequency, and are easily filterable. This technique may be useful at low frequencies to improve the distortion performance of DACs, but has little value when using high speed low-glitch low distortion DACs designed especially for DDS applications.

## DEGLITCHING A DAC OUTPUT USING A SHA REDUCES DISTORTION CAUSED BY CODE-DEPENDENT GLITCHES

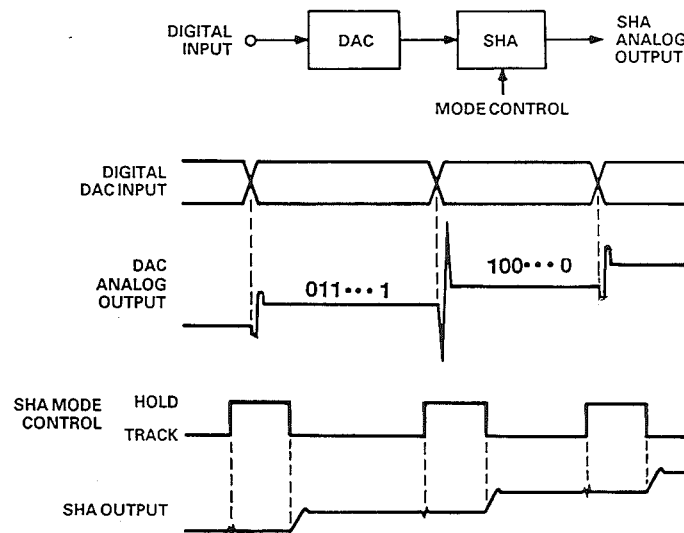


Figure 8.78

Rather than use a single ADC per channel in a simultaneous sampled system, it is often more economical to use multiple SHAs followed by an analog multiplexer and a single ADC

(Figure 8.79). Similarly, in data distribution systems multiple SHAs can be used to route the sequential outputs of a single DAC to multiple channels (Figure 8.80).

## SIMULTANEOUS SAMPLING USING MULTIPLE SHAs AND SINGLE ADC

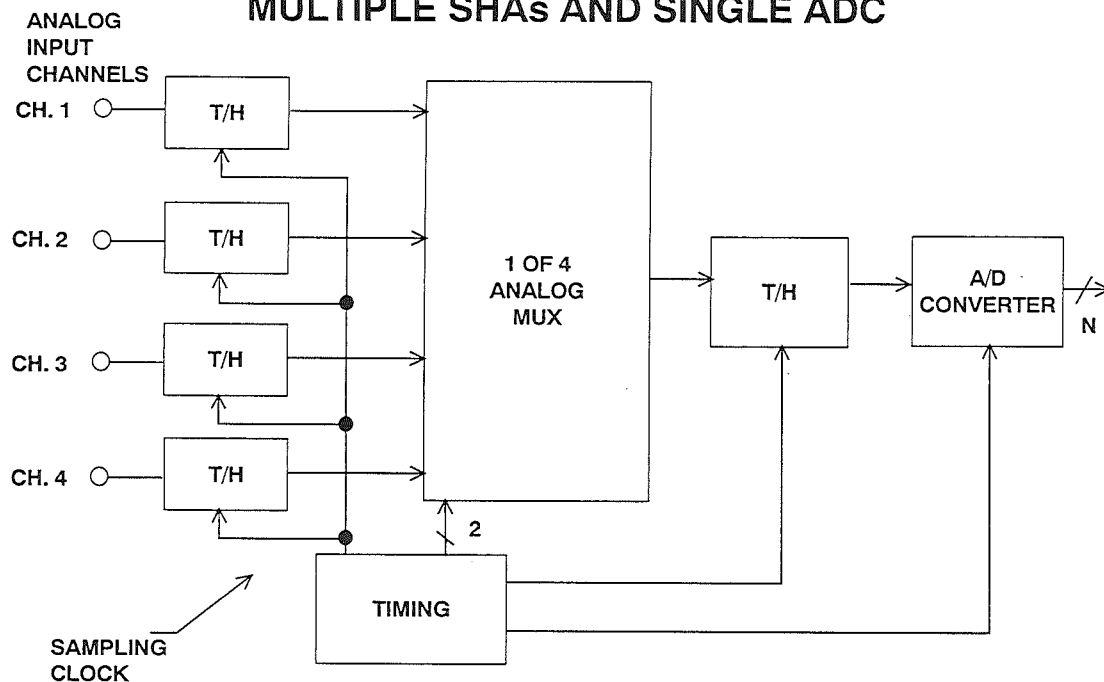


Figure 8.79

## DATA DISTRIBUTION SYSTEM USING MULTIPLE SHAs AND SINGLE DAC

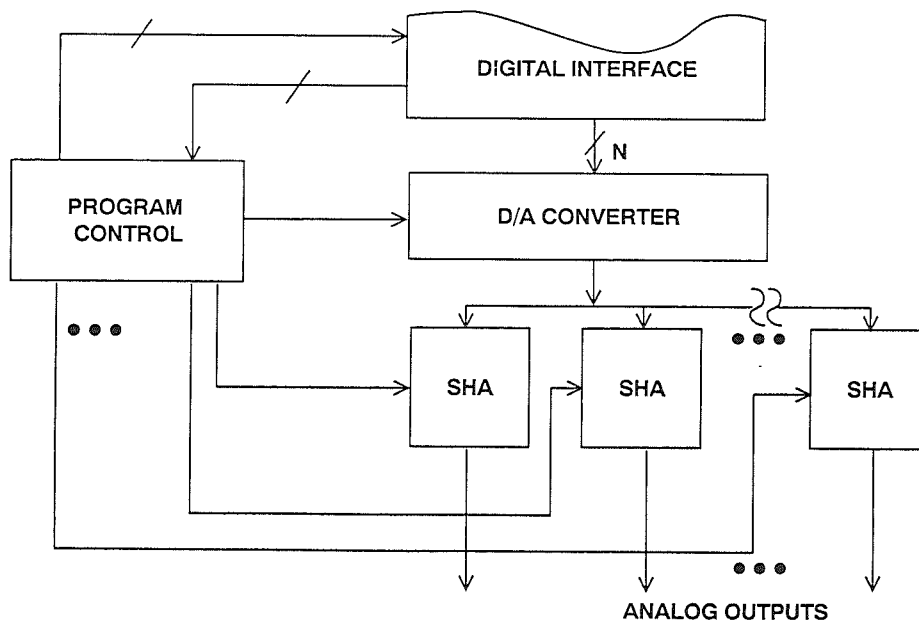


Figure 8.80

A final application for SHAs is shown in Figure 8.81, where SHAs are cascaded to produce analog delay in a sampled data system. SHA 2 is placed in hold just prior to the end of the hold interval for SHA 1. This results in a total pipe-

line delay greater than the sampling period  $T$ . This technique is often used in multi-stage subranging ADCs to allow for the conversion delays of successive stages.

### SHAs USED FOR ANALOG DELAY

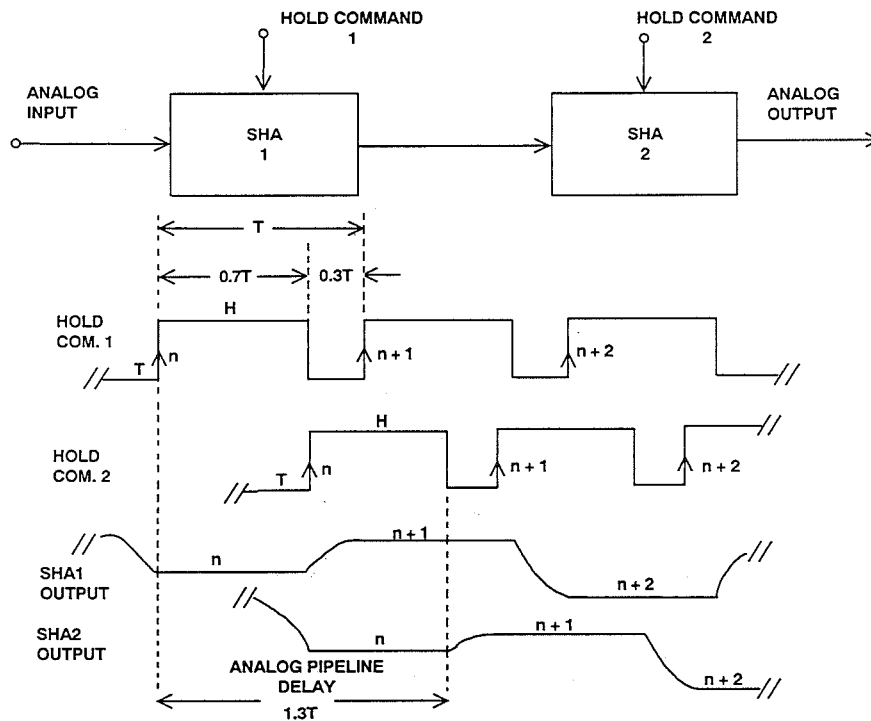


Figure 8.81



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1. Bob Widlar, *New Developments in IC Voltage Regulators*, **IEEE Journal of Solid State Circuits**, Vol. SC-6, February, 1971.
2. Paul Brokaw, *A Simple Three-Terminal IC Bandgap Voltage Reference*, **IEEE Journal of Solid State Circuits**, Vol. SC-9, December, 1974.
3. Paul Brokaw, *More About the AD580 Monolithic IC Voltage Regulator*, **Analog Dialogue**, 9-1, 1975.
4. Walt Jung, *Build an Ultra-Low-Noise Voltage Reference*, **Electronic Design Analog Applications Issue**, June 24, 1993.
5. Joe Buxton, *High Accuracy A/D Conversion*, Chapter 6 in **System Applications Guide**, Analog Devices, 1993.
6. Walt Kester, James Bryant, *Interfacing to High Speed ADCs*, Chapter 13 in **System Applications Guide**, Analog Devices, 1993.
7. Walt Jung, *Getting the Most from IC Voltage References*, **Analog Dialogue**, 28-1, 1994, pp. 13-21.

## SECTION 9

### TRANSDUCER INTERFACING

- Force Transducers
- Introduction to Bridges
- Driving Bridges
- Bridge Applications
- Temperature Transducers:
  - Thermocouples, Thermocouple Principles and Cold-Junction Compensation, Thermocouple Amplifier Considerations, Maintaining Proper Cold-Junction Compensation, Minimizing Parasitic PCB Thermocouple Errors, Thermocouple Linearization Techniques, Resistance Temperature Detector (RTD) Signal Conditioning, Thermistor Signal Conditioning,
- Photodiode Transducers:
  - Photodiode Preamplifier Circuit Considerations, Precautions for Picoampere Circuits, Amplifier Selection, High Speed Fiber Optic Receivers,
- High Impedance Charge Output Transducers:
  - Hydrophones, Accelerometer Amplifiers
- Monolithic Accelerometers
- Charge Coupled Devices (CCDs)
- Hall Effect Magnetic Sensors

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## LINEAR DESIGN SEMINAR

## SECTION 9

# TRANSDUCER INTERFACING

*Walt Kester, Adolfo Garcia, James Bryant*

Because of the many physical variables involved, real world signal processing requires a wide variety of sensing elements. Most are based on resistance, capacitance, current, or voltage output elements, thereby simplifying the interface to electronic measuring and processing equipment. Most of these transducers produce low level outputs which require conditioning before further processing. Conditioning with

precision while maintaining low noise performance presents a significant design challenge.

This section discusses the most popular sensors, how they operate, their outputs, and appropriate conditioning circuitry. Space does not permit a discussion of all sensors, but the general principles presented should still be applicable.

### REAL WORLD PHYSICAL VARIABLES

VARIABLE	SENSOR*	OUTPUT
Force (Pressure)	Strain Gauge	Resistance
	Piezo Transducer	Voltage
Temperature	Thermocouple	Voltage
	Silicon Bandgap	Voltage or Current
	RTD	Resistance
	Thermistor	Resistance
Light Intensity	Photodiode	Current
Acceleration	Accelerometer	Capacitance
Magnetic Field	Hall Effect	Voltage
Displacement	LVDT	AC Voltage
	Potentiometer	Voltage

- ALL GENERATE LOW LEVEL SIGNALS REQUIRING PRECISION LOW-NOISE CONDITIONING
- \* Not all these sensors are considered in this section

Figure 9.1

## FORCE TRANSDUCERS

The most popular electrical elements used in force measurements include the resistance strain gauge, the semiconductor strain gauge, and piezoelectric transducers. The strain gauge measures force indirectly by measuring the deflection it produces in a calibrated carrier.

The resistance strain gauge is a resistive element which changes in length, hence resistance, as the force applied to the base on which it is mounted causes stretching or compression. It is perhaps the most well known transducer for converting force into an electrical variable.

Unbonded strain gauges consist of a wire stretched between two points as

shown in Figure 9.2. Force acting on the wire (area =  $A$ , length =  $L$ , resistivity =  $\rho$ ) will cause the wire to elongate or shorten, which will cause the resistance to increase or decrease proportionally according to:

$$R = \rho L/A$$

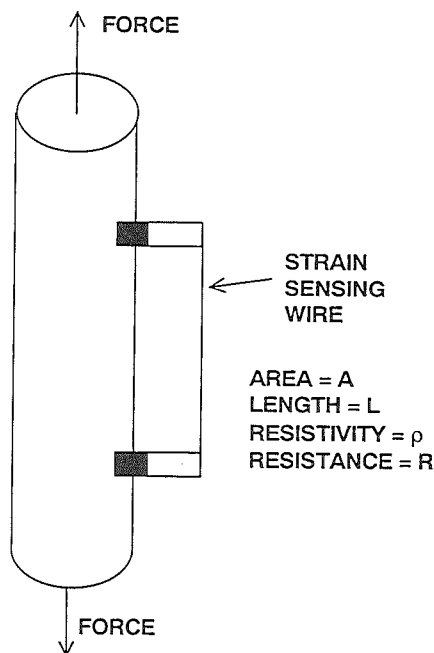
and

$$\Delta R/R = G \cdot \Delta L/L,$$

where  $G$  = Gauge factor (2.0 to 4.5 for metals, and more than 150 for semiconductors).

The dimensionless quantity  $\Delta L/L$  is a measure of the force applied to the wire and is expressed in *microstrains* ( $1\mu\varepsilon = 10^{-6}$  cm/cm).

### UNBONDED WIRE STRAIN GAUGE



$$R = \frac{\rho L}{A}$$

$$\frac{\Delta R}{R} = \frac{G \cdot \Delta L}{L}$$

$G$  = GAUGE FACTOR,  
2.0 TO 4.5 FOR METALS  
>150 FOR SEMICONDUCTORS

$$\frac{\Delta L}{L} = \text{MICROSTRAINS } (\mu\varepsilon) \\ = 10^{-6} \text{ cm/cm}$$

Figure 9.2

Bonded strain gauges consist of a thin wire or conducting film arranged in a coplanar pattern and cemented to a base or carrier. The gauge is normally mounted so that as much as possible of the length of the conductor is aligned in

the direction of the stress that is being measured. Lead wires are attached to the base and brought out for interconnection. Bonded devices are considerably more practical and are in much wider use than unbonded devices.

### BONDED WIRE STRAIN GAUGE

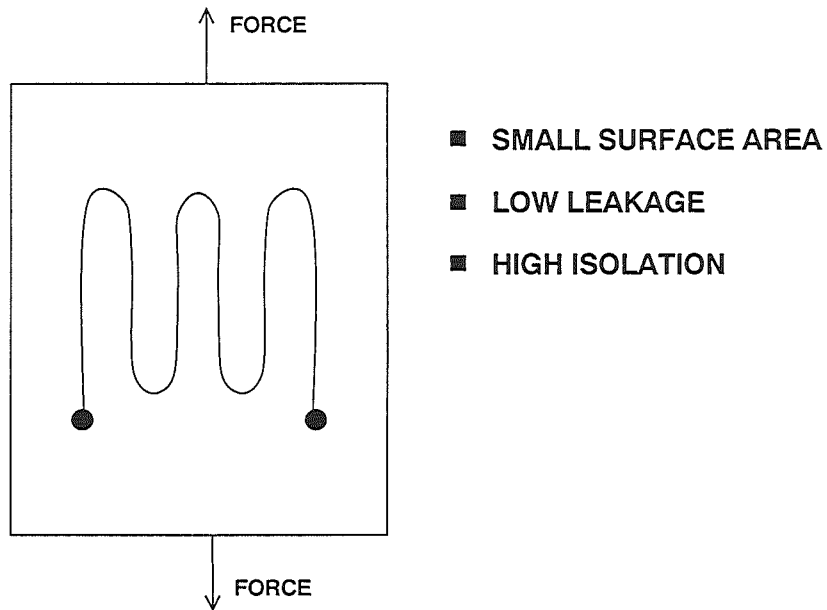
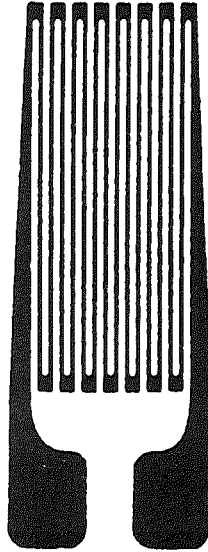


Figure 9.3

Perhaps the most popular version is the foil-type gauge, produced by photo-etching techniques, and using similar metals to the wire types (alloys of copper-nickel (Constantan), nickel-chromium (Nichrome), nickel-iron, platinum-tungsten, etc. (see Figure 9.4). Gauges having wire sensing elements present a small surface area to the specimen; this reduces leakage currents at high temperatures and permits

higher isolation potentials between the sensing element and the specimen. Foil sensing elements, on the other hand, have a large ratio of surface area to cross-sectional area and are more stable under extremes of temperature and prolonged loading. The large surface area and thin cross section also permit the device to follow the specimen temperature and facilitate the dissipation of self-induced heat.

## METAL FOIL STRAIN GAUGE



- PHOTO ETCHING TECHNIQUE
- LARGE AREA
- STABLE OVER TEMPERATURE
- THIN CROSS SECTION
- GOOD HEAT DISSIPATION

Figure 9.4

Strain gauges are low-impedance devices; they require significant excitation power to obtain reasonable levels of output voltage. A typical strain-gauge based load cell bridge will have (typically) a  $350\Omega$  impedance and is specified as having a sensitivity in terms of millivolts full scale per volt of excitation. The load cell is composed of four individual strain gauges arranged as a bridge as shown in Figure 9.5. For a 10V bridge excitation voltage with a

rating of  $3\text{mV/V}$ , 30 millivolts of signal will be available at full scale loading. The output can be increased by increasing the drive to the bridge, but self-heating effects are a significant limitation to this approach: they can cause erroneous readings or even device destruction. Further details regarding the accurate measurement of strain gauge resistance are covered in the section on bridges.

## LOAD CELL COMPOSED OF FOUR STRAIN GAUGES

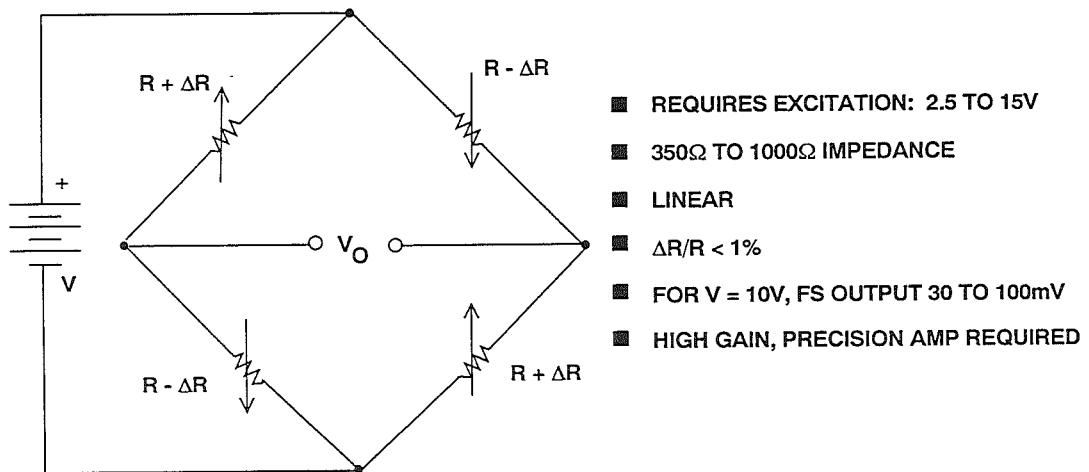


Figure 9.5

Semiconductor strain gauges make use of the resistance change in semiconductor materials in order to obtain greater sensitivity and higher-level output. Such bridges may have 30 times the sensitivity of bridges employing metal films, but are temperature sensitive and difficult to compensate. They are not in as widespread use as the more stable metal-film devices for precision

work; however, where sensitivity is important and temperature variations are small, they may have some advantage. Instrumentation is similar to that for metal-film bridges but is less critical because of the higher signal levels and decreased transducer accuracy. A comparison between metal and semiconductor strain gauges is given in Figure 9.6 (Reference 1, page 51).



## COMPARISON BETWEEN METAL AND SEMICONDUCTOR STRAIN GAUGES

PARAMETER	METAL STRAIN GAUGE	SEMICONDUCTOR STRAIN GAUGE
Measurement Range	0.1 to 40,000 $\mu\epsilon$	0.001 to 3000 $\mu\epsilon$
Gauge Factor	2.0 to 4.5	50 to 200
Resistance, $\Omega$	120, 350, 600, ..., 5000	1000 to 5000
Resistance Tolerance	0.1% to 0.2%	1% to 2%
Size, mm	0.4 to 150 Standard: 3 to 6	1 to 5

Figure 9.6

Piezoelectric force transducers are employed where the forces to be measured are dynamic (i.e., continually changing over the period of interest - usually of the order of milliseconds). These devices utilize the effect that changes in charge are produced in certain materials when they are subjected to physical stress. In fact, piezoelectric transducers are *displacement* transducers with quite large charge outputs for very small displacements, but they are invariably used as force transducers on the assumption that in an elastic material, displacement is proportional to force. Piezoelectric devices produce substantial output voltage in instruments such as accelerometers for vibration studies. Output impedance is high, and charge amplifier

configurations, with low input capacitance, are required for signal conditioning.

The output of a piezoelectric transducer can be modeled as a voltage source in series with a small capacitor as shown in Figure 9.7. Step inputs of physical force result in an effective capacitance change. The op-amp summing voltage is held at zero, and the change in charge is transferred to the feedback capacitor, developing an output voltage at low impedance. The output of this circuit is inversely proportional to the value of the feedback capacitance. The op-amp must have extremely low bias current which is supplied by the very large feedback resistor.

## CHARGE AMPLIFIER USED WITH PIEZOELECTRIC TRANSDUCER

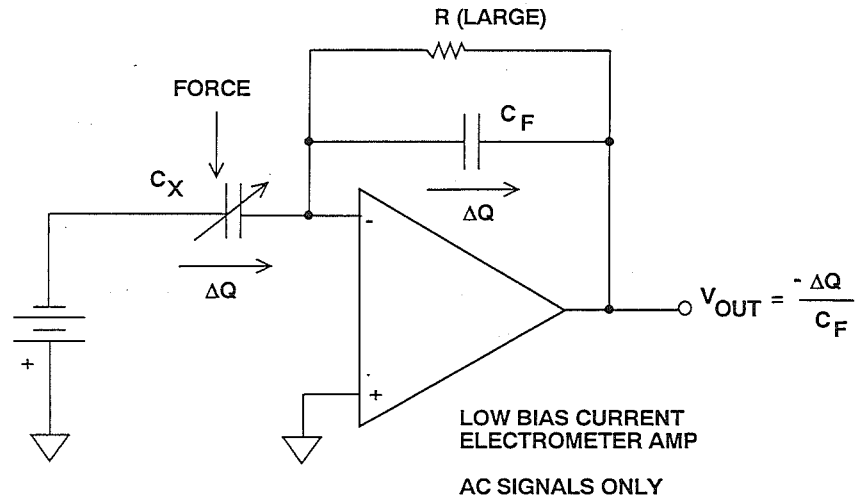


Figure 9.7

Pressures in liquids and gases are measured electrically by a variety of pressure transducers. A variety of mechanical converters (including diaphragms, capsules, bellows, manometer tubes, and Bourdon tubes) are used to measure pressure by measuring an associated length, distance, displacement, and to measure pressure changes

by the motion produced. The output of this mechanical interface is then applied to an electrical converter such as a strain gauge or piezoelectric transducer. Unlike strain gauges, piezoelectric pressure transducers are typically used for high-frequency pressure measurements (such as sonar applications or crystal microphones).

## PRESSURE TRANSDUCERS

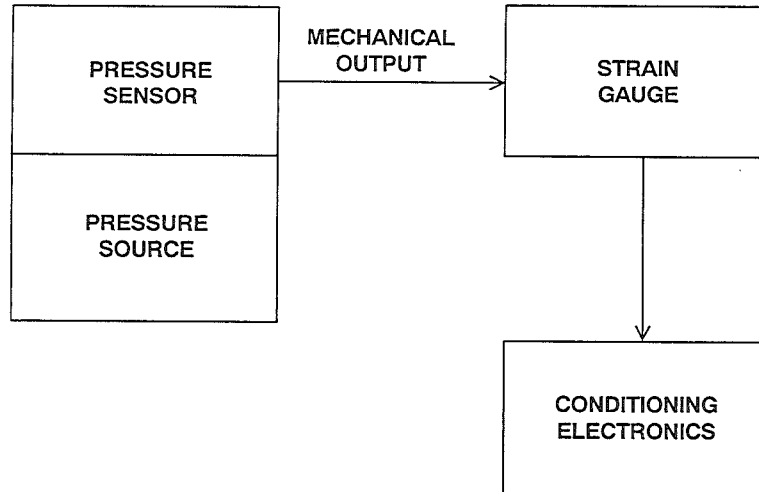


Figure 9.8

There are many ways of defining flow (mass flow, volume flow, laminar flow, turbulent flow). Usually the *amount* of a substance flowing (mass flow) is the most important, and if the fluid's density is constant, a volume flow measurement is a useful substitute that is generally easier to perform. One commonly used class of transducers, which measure flow rate indirectly, involves the measurement of pressure. Flow can be derived by taking the differential pressure across two points in a flowing medium - one at a static point and one in the flow stream. *Pitot tubes* are one form of device used to perform this function. The flow rate is obtained by

measuring the differential pressure with standard pressure transducers as shown in Figure 9.9.

The cantilevered vane shown in Figure 9.10 is a simple way to measure flow and amenable to strain gauge instrumentation.

We have seen that the resistive strain gauge is a fundamental sensor used in a wide variety of force, pressure, and flow measurements. It is therefore important to understand bridge circuits, since they are by far the most common means of converting resistance changes into voltages.

## PITOT TUBE USED TO MEASURE FLOW RATE

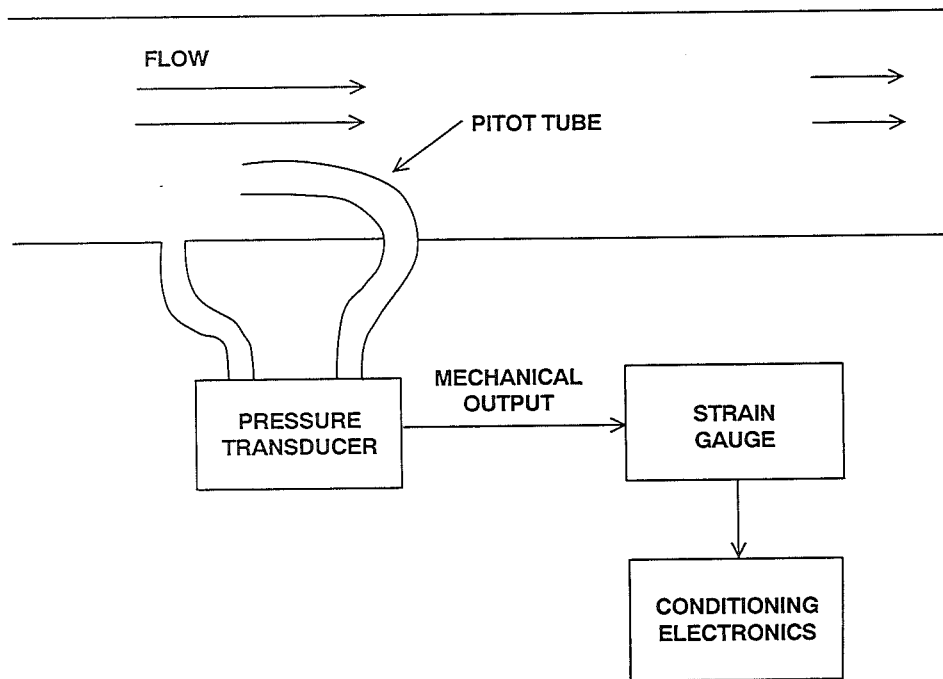


Figure 9.9

## BENDING VANE (STRAIN GAUGE) USED TO MEASURE FLOW RATES

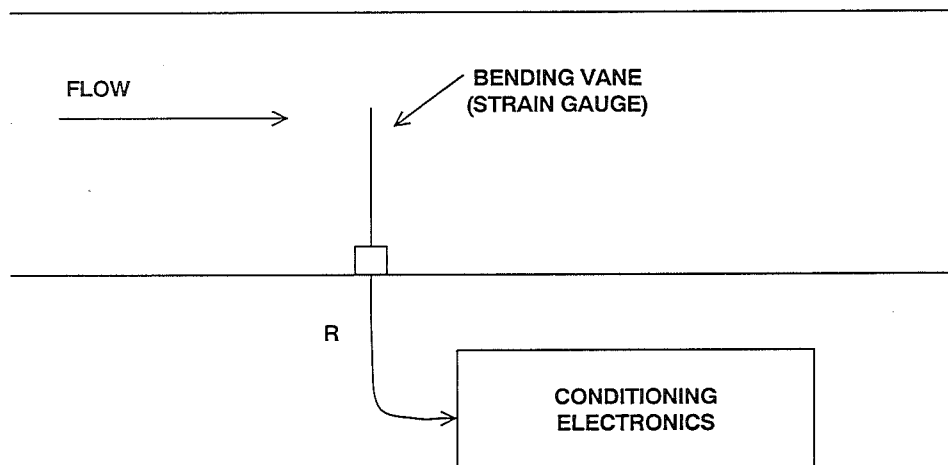


Figure 9.10

## **INTRODUCTION TO BRIDGES**

Resistive elements are the most common transducers. They are inexpensive to manufacture and easy to interface with amplifier circuits. Furthermore, it is possible to integrate sensing elements directly on ICs. Resistive elements can be made sensitive to temperature, strain (by pressure or by flex), and light. Using these basic elements, many complex physical phenomena can be measured; such as fluid or mass flow (by sensing the temperature difference between two calibrated resistances) and dew-point humidity (by measuring two different temperature points), etc.

Transducer elements' resistances can range from less than  $100\Omega$  to several

hundred  $k\Omega$ , depending on the transducer design and the physical environment to be measured. For example, RTDs (Resistance Temperature Devices) are typically  $100\Omega$ . Thermistors are typically  $3500\Omega$  or higher. There are also high impedance piezoelectric or capacitance-modulating transducers whose impedances range from 10's to 100's of  $M\Omega$ .

Most of these transducers produce very low level signals, and therefore high gain is necessary in order to get usable signal levels. Amplifying these signals with precision while maintaining low noise performance presents a significant design challenge.

### **RESISTANCE OF POPULAR TRANSDUCERS**

■ RTD (Resistance Temperature Device)	$100\Omega$
■ Pressure transducers	$350 - 3500\Omega$
■ Strain Gauge	$120, 350, 3500\Omega$
■ Weigh-Scale load cells	$350 - 3500\Omega$
■ Thermistor	$100\Omega - 10M\Omega$
■ Relative humidity	$100k\Omega - 10M\Omega$

**Figure 9.11**

Resistive sensors such as RTDs and strain gauges produce small percentage changes in resistance in response to a change in a physical variable such as temperature or force. Platinum RTDs have a temperature coefficient of about 0.385%/°C. This corresponds to a 38.5% resistance change over a 0°C to 100°C.

Strain gauges present a significant measurement challenge because the typical change in resistance over the entire operating range of a strain gauge may only be 0.1%. Accurately measuring small resistance changes is there-

fore critical to applying resistive sensors.

One technique for measuring resistance (shown in Figure 9.12) is to force a constant current through the resistive sensor and accurately measure the voltage output. This requires an extremely stable current source because any change in the current will be misinterpreted as a resistance change. The power dissipation in the resistive sensor must be small so that self-heating does not produce errors, therefore the drive current must be small.

### MEASURING RESISTANCE INDIRECTLY USING A CONSTANT CURRENT SOURCE

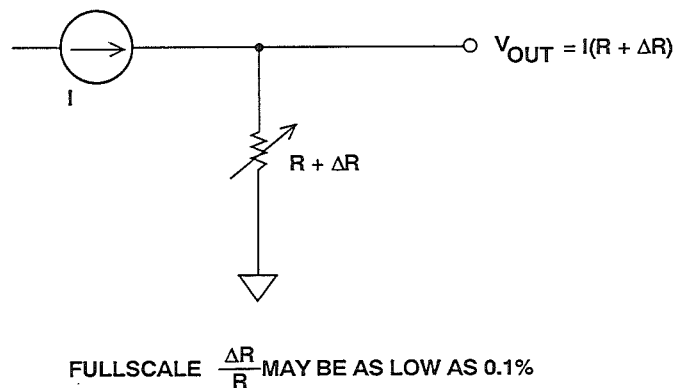
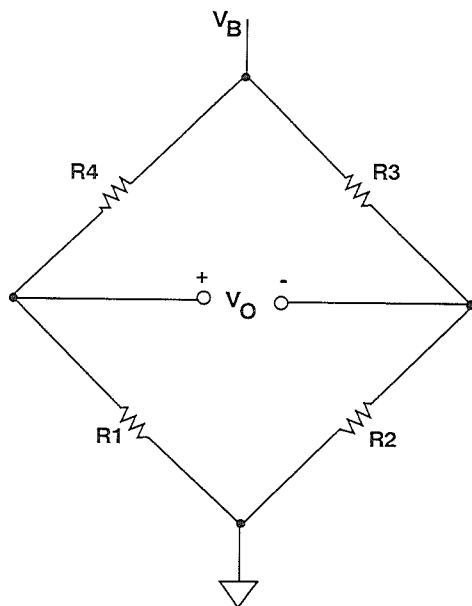


Figure 9.12

Bridges offer an attractive alternative for measuring small resistance changes accurately. The basic Wheatstone bridge (actually developed by S. H. Christie in 1833) is shown in Figure 9.13. It consists of four resistors connected to form a quadrilateral, a source

of excitation (voltage or current) connected across one of the diagonals, and a voltage detector connected across the other diagonal. The detector measures the difference between the outputs of two voltage dividers connected across the excitation.

## THE WHEATSTONE BRIDGE



$$V_O = \frac{R1}{R1 + R4} V_B - \frac{R2}{R2 + R3} V_B$$

$$= \left( \frac{R1}{R4} - \frac{R2}{R3} \right) V_B$$

AT BALANCE,

$$V_O = 0 \quad \text{IF} \quad \frac{R1}{R4} = \frac{R2}{R3}$$

Figure 9.13

A bridge measures resistance indirectly by comparison with a similar resistance. The two principal ways of operating a bridge are as a null detector or as a device that reads a difference directly as voltage or current.

When  $R1/R4 = R2/R3$ , the resistance bridge is at a *null*, irrespective of the mode of excitation (current or voltage, AC or DC), the magnitude of excitation, the mode of readout (current or voltage), or the impedance of the detector.

Therefore if the ratio of  $R2/R3$  is fixed at  $K$ , a null is achieved when  $R1 = K \cdot R4$ . If  $R1$  is unknown and  $R4$  is an accurately determined variable resistance, the magnitude of  $R1$  can be found by adjusting  $R4$  until null is achieved. Conversely, in transducer-type measurements,  $R4$  may be a fixed reference, and a null occurs when the magnitude of the external variable (strain, temperature, etc.) is such that  $R1 = K \cdot R4$ .

Null measurements are principally used in feedback systems involving electro-mechanical and/or human elements. Such systems seek to force the active element (strain gauge, RTD, thermistor, etc.) to balance the bridge by influencing the parameter being measured.

For the majority of transducer applications employing bridges, the deviation of one or more resistors in a bridge from

an initial value is measured as an indication of the magnitude (or a change) in the measured variable.

Figure 9.14 shows the three commonly used bridges suitable for sensor applications and the corresponding equations which relate the bridge output voltage to the excitation voltage and the bridge resistance values.

## BASIC BRIDGE CONFIGURATIONS

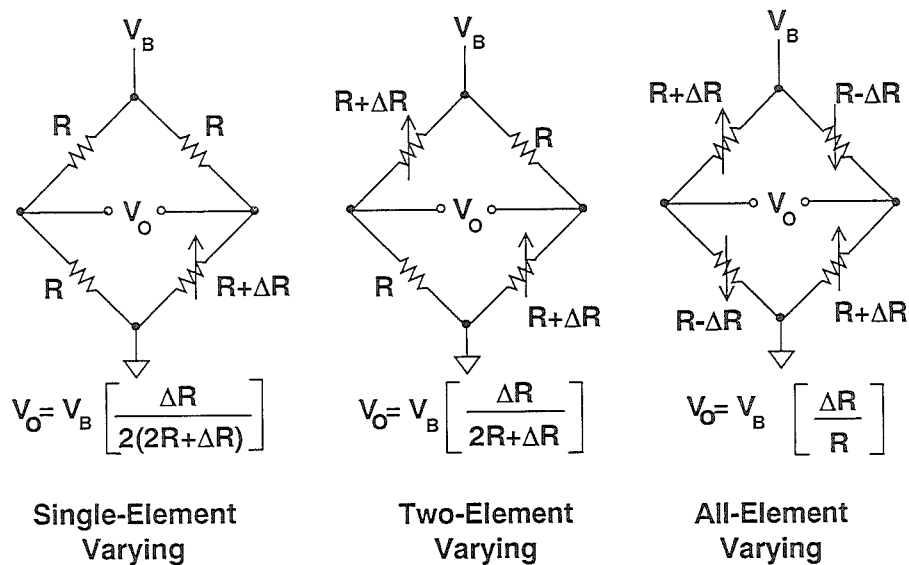


Figure 9.14

The *single-element varying* bridge is most suited for temperature sensing using RTDs or thermistors. All the resistances are nominally equal, but one of them (the sensor) is variable by an amount  $\Delta R$ . As the equation indicates, the relationship between the bridge output and  $\Delta R$  is not linear. For example, if  $R = 100\Omega$  and  $\Delta R = \pm 0.1\Omega$  ( $\pm 0.1\%$  change in resistance), the output of the bridge is  $\pm 2.49875\text{mV}$  for  $V_B = 10\text{V}$ . This corresponds to an end-point

linearity error of  $\pm 0.0125\%$ . (Bridge end-point linearity error is calculated as the worst error in % FS from a straight line which connects the origin and the end points at  $\pm \text{FS}$ , i.e. the FS gain error is not included). If  $\Delta R = \pm 1\Omega$ , ( $\pm 1\%$  change in resistance), the output of the bridge is  $\pm 24.8756\text{mV}$ , representing an end-point linearity error of approximately  $\pm 0.125\%$ . The end-point linearity error of the single-element bridge can be expressed in equation form:

$$\begin{aligned} &\text{Single-Element Varying} \\ &\text{Bridge End-Point Linearity Error} \approx \% \text{ Change in Resistance} \div 8 \end{aligned}$$



In some applications, this error may be acceptable, but there are methods available to linearize bridges which will be discussed shortly.

The *sensitivity* of a bridge is the ratio of the maximum expected change in the output voltage to the excitation voltage. For the examples given above, the sensitivities are  $500\mu\text{V/V}$  (for  $\pm 0.1\%$  resistance change) and  $5\text{mV/V}$  (for  $\pm 1\%$  resistance change).

The *two-element varying* bridge produces twice the signal output but requires two identical sensors. The nonlinearity is the same as that of the single-element varying bridge. The two-element varying bridge is commonly found in pressure transducers and flow meter systems.

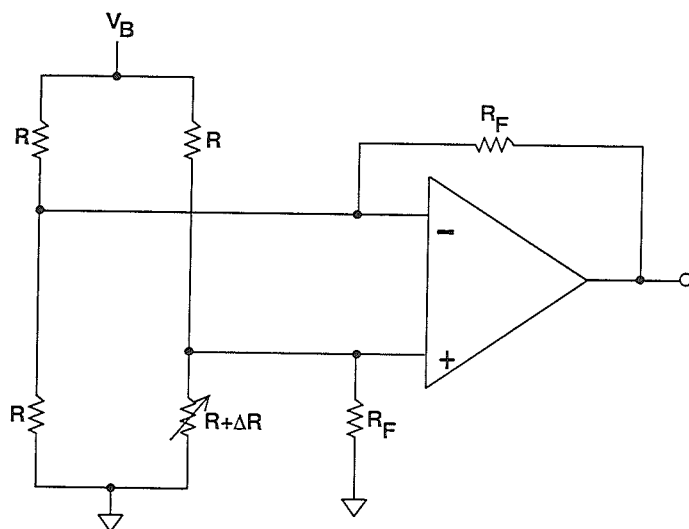
The *all-element varying* bridge produces the most signal for a given resistance change and is inherently linear. It is an industry-standard configuration for load

cells which are constructed from four identical strain gauges.

The output of a single-element varying bridge may be amplified by an op-amp connected in the inverting mode as shown in Figure 9.15. This circuit has poor gain accuracy and also unbalances the bridge due to loading from  $R_F$  and the op amp bias current. A much better approach is to use an instrumentation amplifier as shown in Figure 9.16. This efficient circuit provides better gain accuracy and does not unbalance the bridge.

Bridges can be driven with constant current sources rather than voltage sources. This eliminates errors due to DC voltage drops in the wiring to the bridge. The circuit shown in Figure 9.17 is an example and has the advantage of reduced nonlinearity (0.062% rather than 0.125% for a 1% FS resistance change).

## SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 1



### Advantages:

- No signal in = zero volts out
- Single supply operation
- Single op amp stage

### Disadvantages:

- Nonlinear operation:
- 0.125% nonlinearity for 1% fullscale  $\Delta R$  change
- Poor gain accuracy
- Unbalanced output  $R$  due to varying element

Figure 9.15

## SINGLE-ELEMENT VARYING BRIDGE, AMPLIFIER CONFIGURATION 2

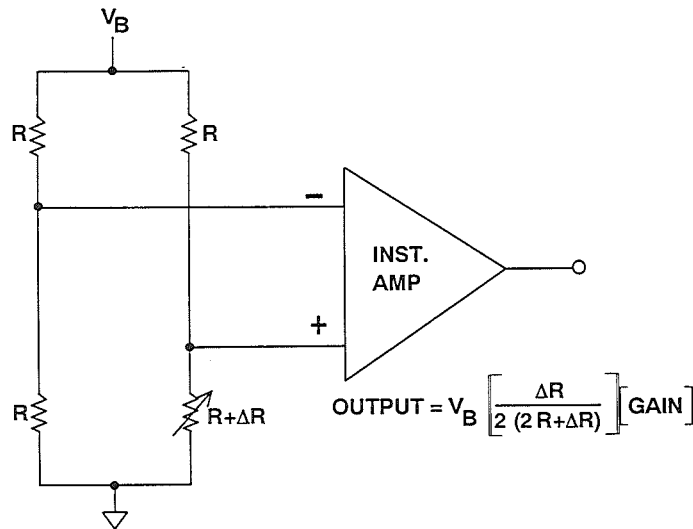


Figure 9.16

## DRIVING A SINGLE-ELEMENT VARYING BRIDGE WITH A CONSTANT CURRENT SOURCE

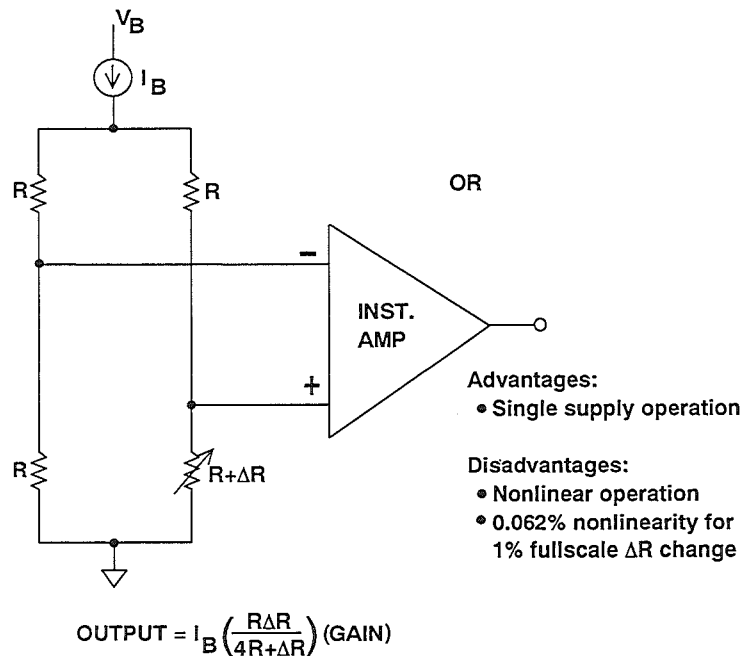


Figure 9.17

Various techniques are available to linearize bridges, but it is important to distinguish between the linearity of the bridge equation and the linearity of the transducer response to the phenomenon being sensed. For example, if the active element is an RTD, the bridge used to implement the measurement might have adequate linearity; yet the output could still be nonlinear due to the RTD's nonlinearity. Manufacturers of transducers employing bridges address the nonlinearity issue in a variety of ways, including keeping the resistive swings in the bridge small, shaping complementary nonlinear response into the active elements of the bridge, using resistive trims for first-order corrections, and others.

Figure 9.18 shows a single-element varying active bridge in which an op-amp produces a null by adding a voltage in series with the variable arm. That voltage is equal in magnitude and

opposite in polarity to the incremental voltage across the varying element and is linear with  $\Delta R$ . Since it is an op-amp output, it can be used as a low impedance output point for the bridge measurement. This active bridge has a gain of two over the standard single-element varying bridge, and the output is linear, even for large values of  $\Delta R$ . Because of the small output signal this bridge must usually be followed by an amplifier.

Two other circuits for linearizing a single-element varying bridge are shown in Figures 9.19 and 9.20. In Figure 9.19, the bottom of the bridge is driven by an op-amp, which maintains a constant current in the varying resistance. The output signal is taken from the right-hand leg of the bridge and amplified by a non-inverting op-amp. The op-amp in Figure 9.20 performs the same function, but the bridge output is amplified by a second op-amp configured in the inverting mode.

## LINEARIZING A SINGLE-ELEMENT VARYING BRIDGE, METHOD 1

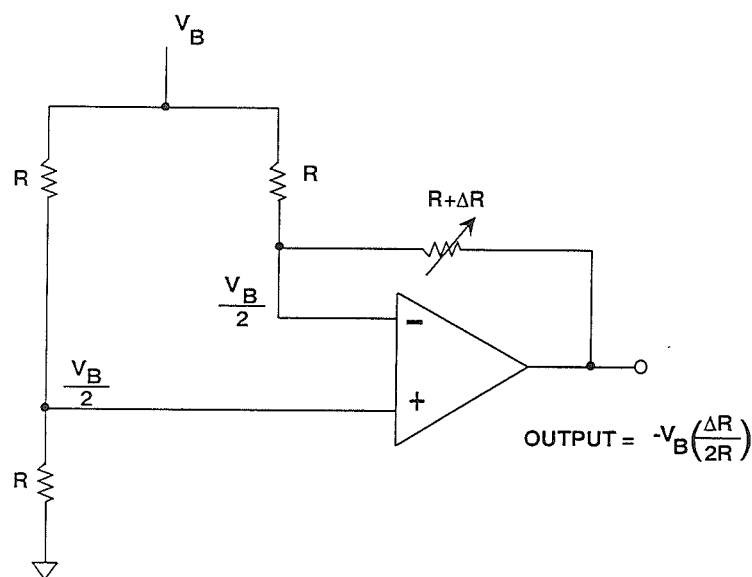


Figure 9.18

## LINEARIZING A SINGLE-ELEMENT VARYING BRIDGE, METHOD 2: NON-INVERTING OUTPUT AMPLIFIER

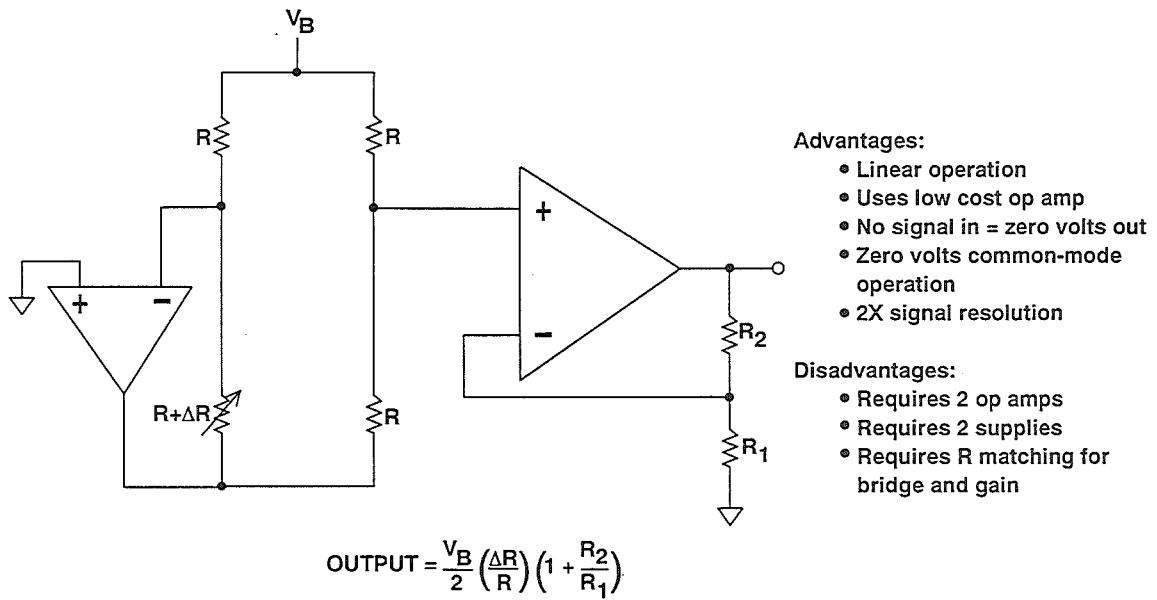


Figure 9.19

## LINEARIZING A SINGLE-ELEMENT VARYING BRIDGE, METHOD 2: INVERTING OUTPUT AMPLIFIER

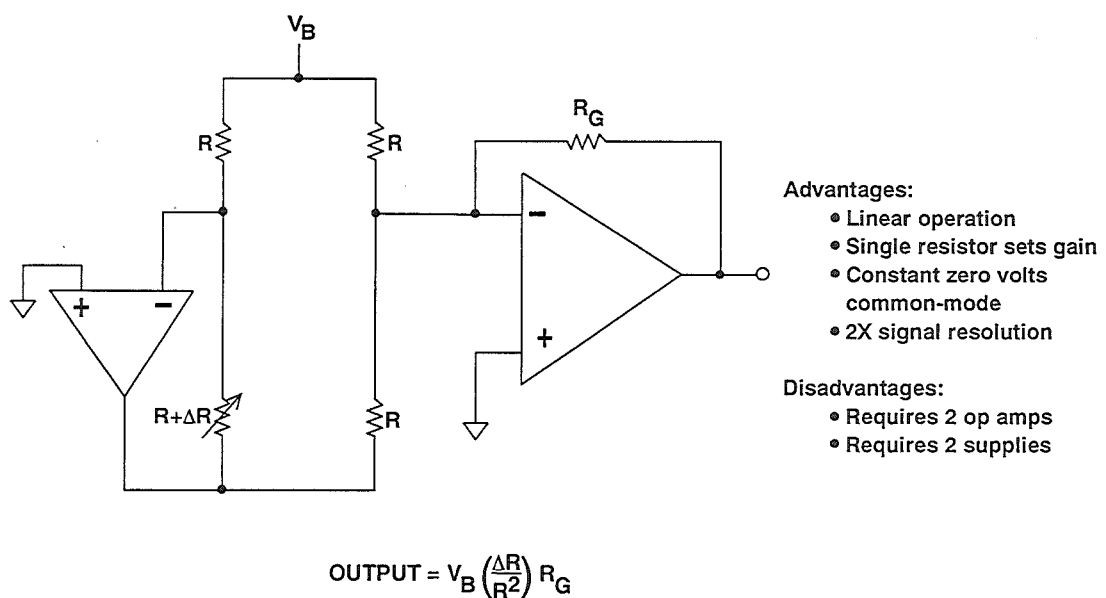


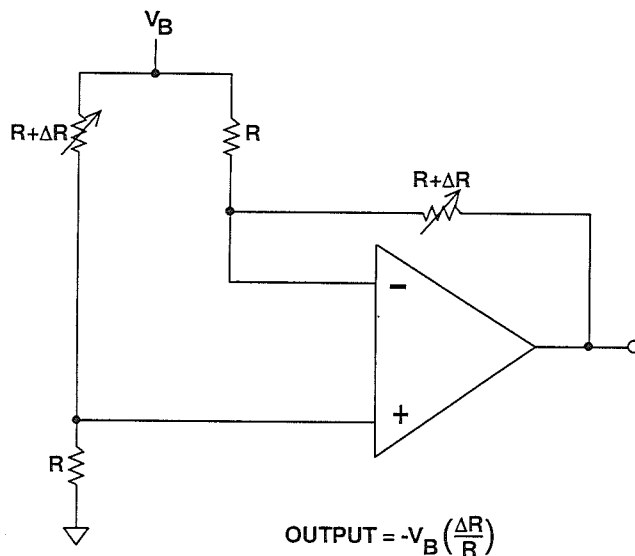
Figure 9.20

A circuit for linearizing a two-element varying bridge is shown in Figure 9.21. This circuit is similar to Figure 9.18 and has twice the gain. Additional gain may be necessary.

The two-element varying bridge circuit in Figure 9.22 uses an op-amp to main-

tain a constant current through the bridge ( $V_R/R_{SENSE}$ ). The current through each leg of the bridge remains constant ( $I_B/2$ ) as the resistances change, therefore the output is a linear function of  $\Delta R$ . An instrumentation amplifier provides the additional gain.

### LINEARIZING A TWO-ELEMENT VARYING BRIDGE, METHOD 1



#### Advantage:

- Linear operation

#### Disadvantages:

- Low signal output implies larger errors
- Requires second amp for gain

Figure 9.21

## LINEARIZING A TWO-ELEMENT VARYING BRIDGE, METHOD 2

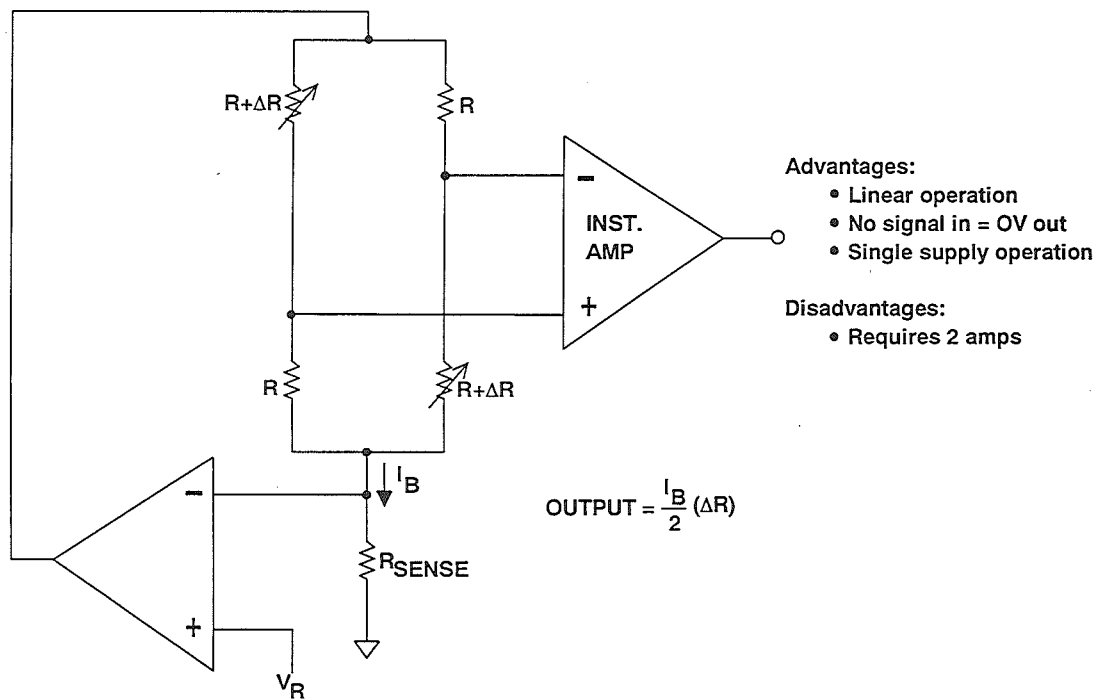


Figure 9.22

## DRIVING BRIDGES

Wiring resistance and noise pickup are the biggest problems associated with remotely located bridges. Figure 9.23 shows how Kelvin sensing can be used to eliminate the effects of voltage dropped across the wiring resistance. The current in the sense lines is minimal, therefore the op-amps maintain a

constant bridge voltage independent of the wiring resistance in the drive and return paths.

Another method often used to eliminate wiring resistance errors is to drive the bridge with a constant current source as shown in Figure 9.24.

## DRIVING BRIDGES USING KELVIN SENSING

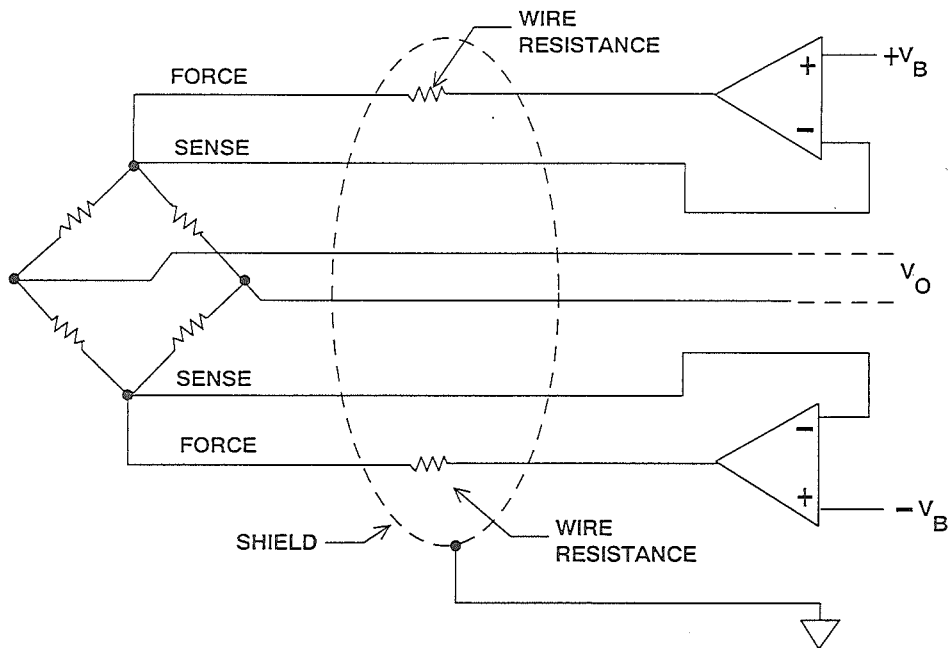


Figure 9.23

## DRIVING BRIDGES USING A CONSTANT CURRENT SOURCE

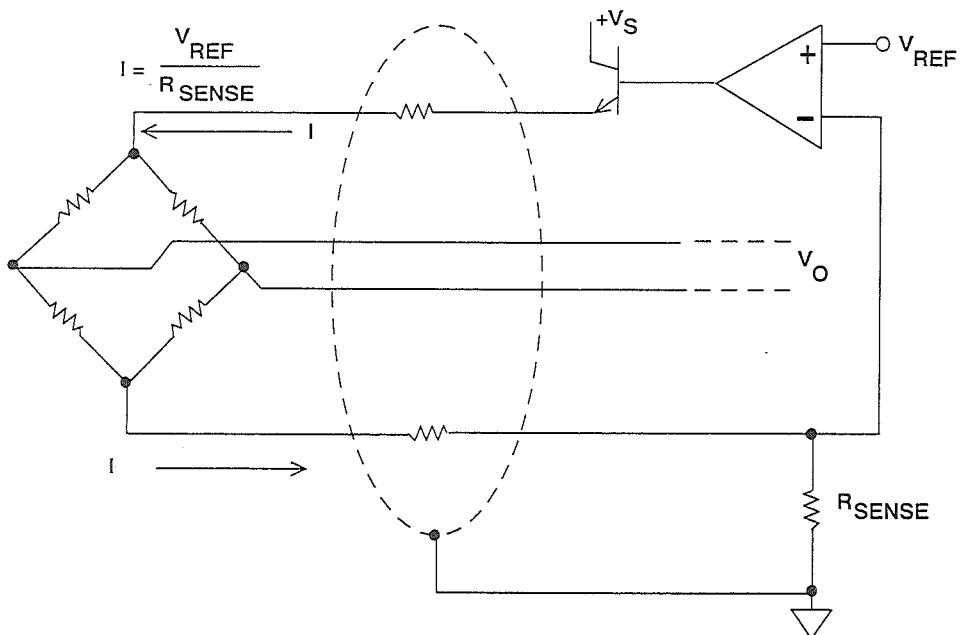


Figure 9.24

Remotely located transducers are a potential source of EMI/RFI pickup. It is recommended that shielded cable be used between the sensor and the instrumentation electronics. The optimum point to ground the shield is at the electronics, thereby shunting stray RF

currents into a low impedance ground plane. Under no circumstances should the shield be grounded at both ends; this will cause ground-loop currents to flow in the shield and induce unwanted voltages on the conductors.

### GROUNDING THE SHIELD AT THE RECEIVING END MINIMIZES RF PICKUP

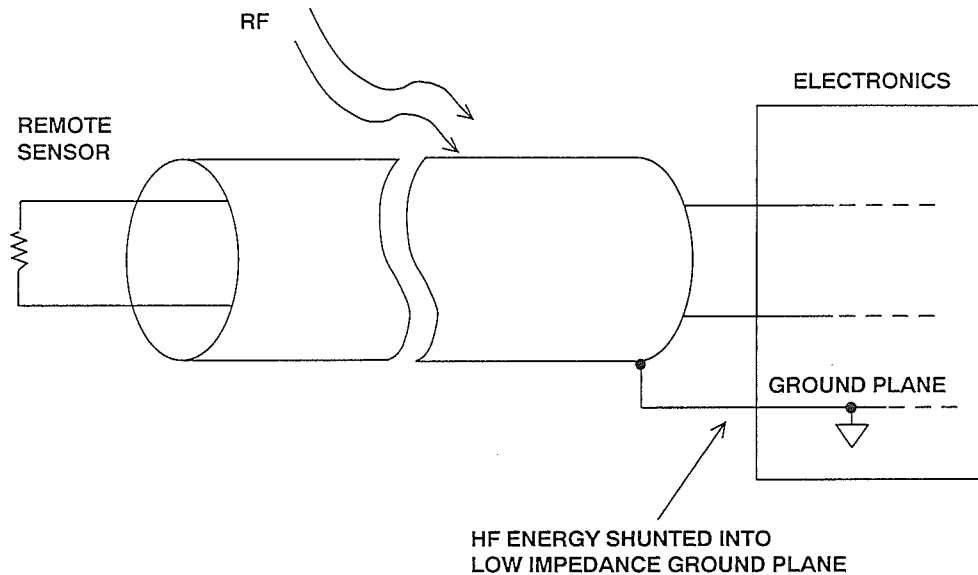


Figure 9.25



# BRIDGE APPLICATIONS

An example of an all-element varying bridge circuit is a fatigue monitoring strain sensing circuit as shown in Figure 9.26. The full bridge is an integrated unit that can be attached to the surface on which the strain or flex is to be measured. In order to facilitate remote sensing, current excitation is used. The OP-177 servos the bridge current to 10mA around a reference voltage of 1.235V. The strain gauge

produces an output of  $10.25\text{mV}/1000\mu\epsilon$ . The signal is amplified by the AD620 instrumentation amplifier. Full-scale strain voltage may be set by adjusting the  $100\Omega$  gain potentiometer such that, for a strain of  $-3500\mu\epsilon$ , the output reads  $-3.500\text{V}$ ; and for a strain of  $+5000\mu\epsilon$ , the output registers a  $+5.000\text{V}$ . The measurement may then be displayed with a digital voltmeter.

## FATIGUE LOAD STRAIN SENSOR AMPLIFIER

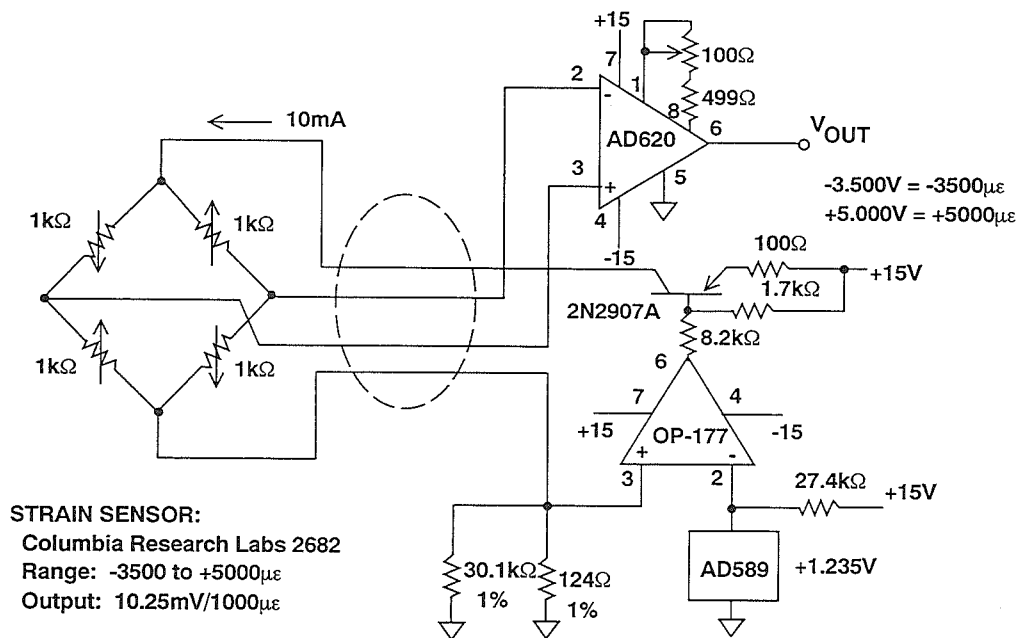
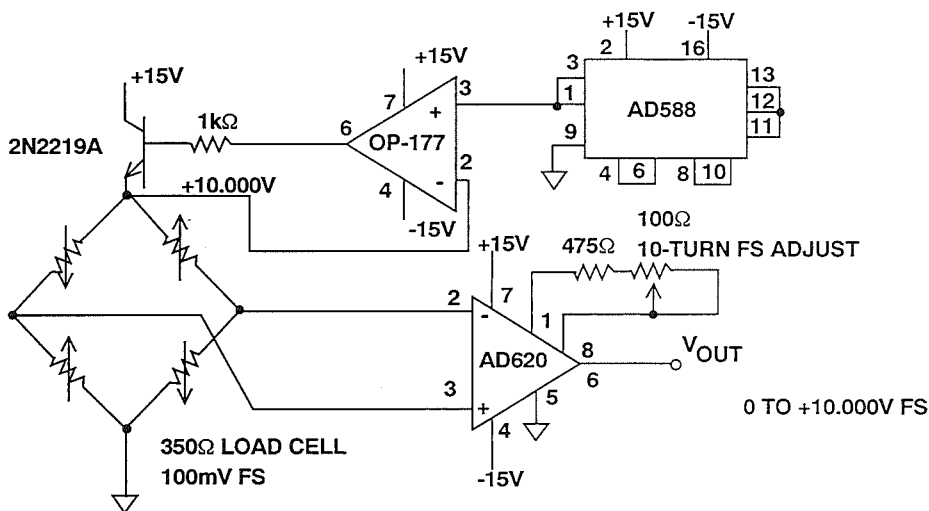


Figure 9.26

Another example is a weigh-scale amplifier circuit shown in Figure 9.27. A typical load cell has a bridge resistance of  $350\Omega$ . A  $10.000\text{V}$  bridge excitation produces linear bridge behavior. To ensure this linearity is preserved, an instrumentation amplifier is used. This design has a minimum number of

critical resistors and amplifiers, making the entire implementation accurate, stable, and cost effective. The only requirement is that the  $475\Omega$  resistor and the  $100\Omega$  potentiometer have low temperature coefficients so that the amplifier gain does not drift over temperature.

# WEIGH-SCALE LOAD CELL AMPLIFIER

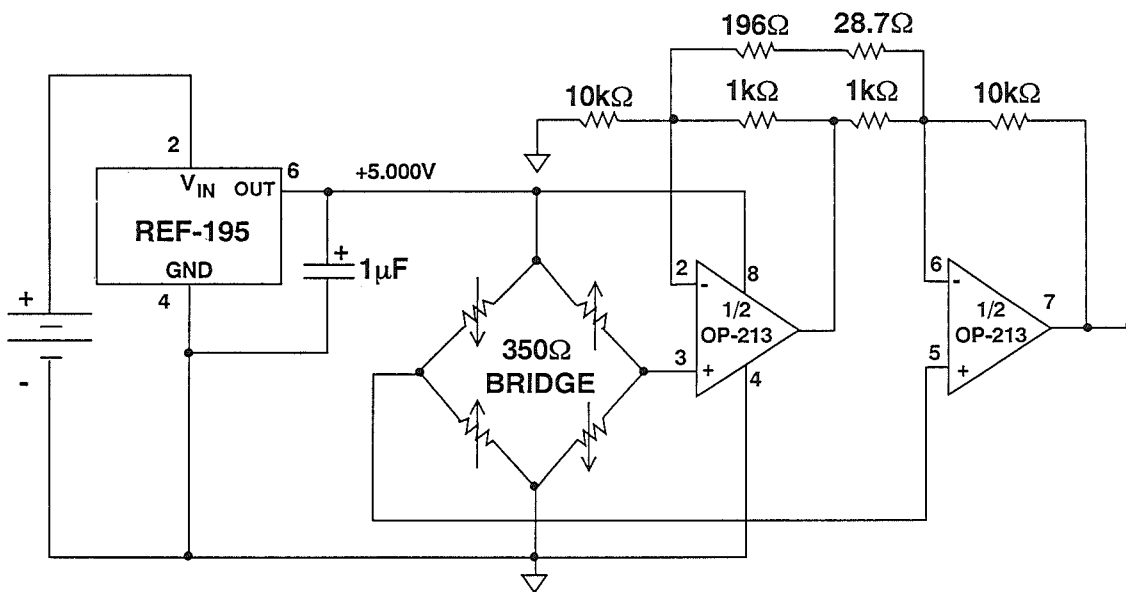


**Figure 9.27**

A precision weigh-scale transducer is usually configured as a  $350\Omega$  bridge. Figure 9.28 shows a load-cell amplifier that is powered from a single supply. The excitation voltage to the bridge must be precise and stable, otherwise it introduces an error in the measure-

ment. In this circuit, a precision 5V reference is used as the bridge drive. The REF-195 reference can supply more than 30mA to a load, so it can drive the 350Ω bridge without the need of a buffer.

## PRECISION SINGLE-SUPPLY LOAD-CELL AMPLIFIER



**Figure 9.28**

The bridge signal is amplified by the two OP-213 op amps connected as an instrumentation amplifier. The resistor network sets the gain according to the formula:

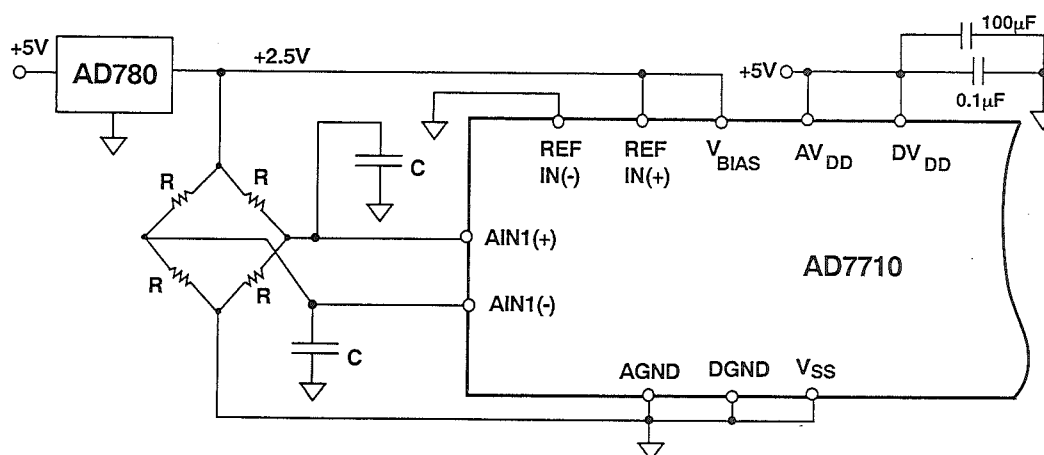
$$G = 1 + \frac{10\text{k}\Omega}{1\text{k}\Omega} + \frac{20\text{k}\Omega}{196\Omega + 28.7\Omega} = 100$$

For optimum common-mode rejection, the resistor ratios must be precise. High tolerance resistors ( $\pm 0.5\%$  or better) should be used.

For zero bridge signal, the amplifier will swing to within 2.5mV of 0V. This is the minimum output limit of the OP-213. Therefore, if an offset adjustment is required, one should start the adjustment from a positive voltage and adjust downward until the output stops changing. This is the point where the amplifier limits the swing. Because of the single supply design, the amplifier cannot sense signals which have negative polarity.

The AD7710/AD7711/AD7712/AD7713-family of 22-bit ADCs make a simple matter of interfacing bridges to a data converter. The simplified circuit in Figure 9.29 is an example. The bridge is connected directly to the differential inputs of the ADC. The internal PGA provides a gain of up to 128 to the bridge output (a 350 $\Omega$  bridge requires 7.1mA @ 2.5V). The AD780 precision reference has sufficient drive current to supply both the bridge and the ADC reference input. With the internal PGA gain set for 64, a 40mV bridge output represents a full scale input to the ADC. The external reference in conjunction with the filter capacitors on the ADC input provide low noise so that an effective resolution (ENOB) of 17 bits is achieved at a 10Hz conversion rate. More details on the operation of the AD77xx-series of ADCs can be found in Reference 4.

## WEIGH SCALE APPLICATION USING THE AD7710



- High impedance differential input interfaces directly to bridge
- External reference used for accuracy
- Wide range of impedances can be used for bridge
- Add capacitors to input to filter noise

Figure 9.29

## TEMPERATURE TRANSDUCERS

Accurate measurement of temperature is critical to most measurement and process control applications. Thermocouples are capable of measuring extreme temperatures, but require cold-junction-compensation techniques, are non-linear, and have low-level outputs. Semiconductor temperature sensors provide integrated and accurate

solutions and high-level outputs, but operate over a more limited range. Resistance Temperature Devices (RTDs) are accurate and linear, but require excitation current and bridge circuits. Thermistors have the most sensitivity but are the most non-linear. The characteristics of temperature sensors are summarized in Figure 9.30.

### TEMPERATURE TRANSDUCERS

SEMICONDUCTOR	THERMOCOUPLE	RTD	THERMISTOR
Limited Range: -55 to +150°C	Widest Range: -184 to +2300°C	Range: -200 to +850°C	Range: 0 to +100°C
Linearity: 1°C Repeatability: 0-1°C Accuracy: 1°C	Repeatable Characteristics	Fair Linearity	Poor Linearity
Requires Excitation Source	Needs Cold Junction Compensation	Requires Excitation	Requires Excitation
10mV/K or 1μA/K Output Typical	Low-Voltage Output	Low Cost	High Sensitivity
	Small		

Figure 9.30

Modern semiconductor temperature sensors offer high accuracy and high linearity over an operating range of about -55°C to +150°C. Internal amplifiers can scale the output to convenient values, such as 10mV/°C. They are also useful in cold-junction-compensation circuits for wide temperature range thermocouples.

All semiconductor temperature sensors make use of the relationship between a bipolar junction transistor's (BJT) base-emitter voltage to its collector current:

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right)$$

where  $k$  is Boltzmann's constant,  $T$  is the absolute temperature,  $q$  is the charge of an electron, and  $I_S$  is a current related to the geometry and the temperature of the transistors. (The equation assumes a voltage of at least a few hundred mV on the collector, and ignores Early effects.)

If we take  $N$  transistors identical to the first (see Figure 9.31) and allow the total current  $I_C$  to be shared equally among them, we find that the new base-emitter voltage is given by the equation

$$V_N = \frac{kT}{q} \ln \left( \frac{I_C}{N \cdot I_S} \right)$$

Neither of these circuits is of much use by itself because of the strongly temperature dependent current  $I_S$ , but if we have equal currents in one BJT and  $N$  similar BJTs then the expression for the *difference* between the two base-emitter voltages is proportional to absolute temperature and does not contain  $I_S$ .

## BASIC RELATIONSHIPS FOR SEMICONDUCTOR TEMPERATURE SENSORS

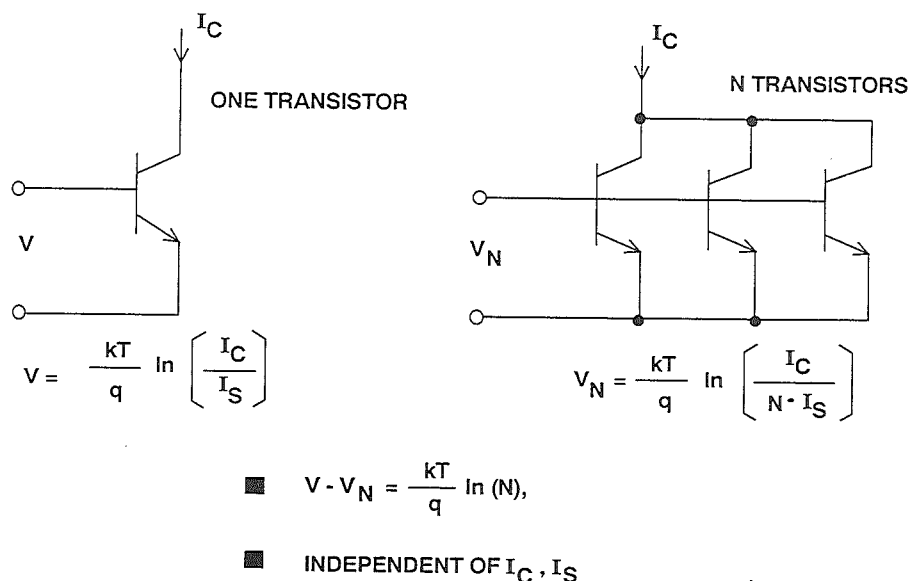


Figure 9.31

$$V - V_N = \frac{kT}{q} \ln\left(\frac{I_c}{I_s}\right) - \frac{kT}{q} \ln\left(\frac{I_c}{N \cdot I_s}\right)$$

$$V - V_N = \frac{kT}{q} \left[ \ln\left(\frac{I_c}{I_s}\right) - \ln\left(\frac{I_c}{N \cdot I_s}\right) \right]$$

$$V - V_N = \frac{kT}{q} \ln \left[ \frac{\left(\frac{I_c}{I_s}\right)}{\left(\frac{I_c}{N \cdot I_s}\right)} \right] = \frac{kT}{q} \ln(N)$$

So if we arrange a circuit containing  $N+1$  NPN BJTs, a temperature stable resistor, and a PNP current mirror as shown in Figure 9.32, the total current in the circuit will be proportional to its absolute temperature (PTAT), as will the voltage across the resistor (which is the difference between  $V$  and  $V_N$  in the equations above).

## CLASSIC BANDGAP TEMPERATURE SENSOR

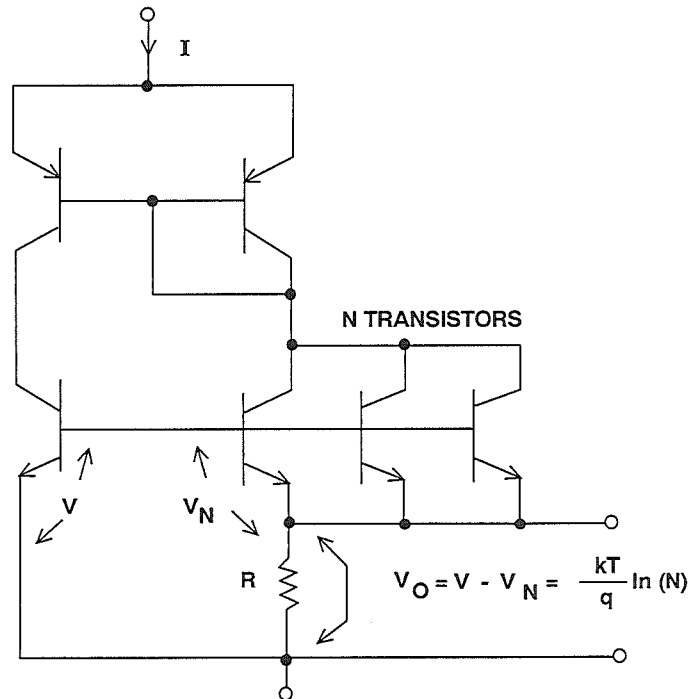


Figure 9.32

This circuit is the basic *band-gap* temperature sensor, and is widely used in semiconductor temperature sensors. The circuit in Figure 9.32 is incomplete, because it has two stable states - one with all the transistors biased on, and one with all the transistors turned off; therefore, turn-on circuitry is required to ensure that when a voltage is applied the transistors will turn on. This is done in different ways in different circuits.

The AD590, AD592, and AC2626 are two terminal temperature sensors with a current equal to  $1\mu\text{A}/\text{K}$  (provided there is at least 4V applied to them). They are slightly vulnerable to RFI and should be decoupled at HF where there is a risk of this exposure.

The AD22100 is a low-cost sensor for automotive use. It uses a +5V supply, and its output is  $22.5\text{mV}/^\circ\text{C}$  from  $-50^\circ\text{C}$  (at which temperature its output is 0.25V) to  $+150^\circ\text{C}$ , but its output is proportional to the supply (i.e. if the supply is x% high, so is the output).

The TMP-01 is a sensor with an output of  $5\text{mV}/\text{K}$  which also contains a voltage

reference and two comparators with programmable hysteresis. It operates with supplies from 5 to 12V.

The AD537 is a voltage-to-frequency converter (VFC) which also contains a temperature sensor with  $1\text{mV}/\text{K}$  output, so that it may be used as a temperature-to-frequency converter.

The AD594, AD595, AD596, and AD597 are special-purpose instrumentation amplifiers, intended for use with thermocouples, which contain temperature sensors to provide cold-junction compensation. (Thermocouples have two junctions and measure temperature *differences*, and to use one successfully it is necessary to compensate for the temperature of the cold junction. This series of devices work on the assumption that the cold junction is at the same temperature as the IC chip. It is therefore essential to ensure that the cold junction is close to the IC [not on the other side of the PC board] and that there are no local heat sources to disrupt it.

## **THERMOCOUPLES**

Thermocouples are small, rugged, relatively inexpensive, and operate over the widest range of all temperature sensors. They are especially useful for making measurements at extremely high temperatures (up to  $+2300^\circ\text{C}$ ) in hostile environments. They produce only millivolts of output, however, and require precision amplification for further processing. They are more linear than many other sensors, and

their non-linearity has been well characterized. Some common thermocouples are shown in Figure 9.33. The most common metals used are Iron, Platinum, Rhodium, Rhenium, Tungsten, Copper, Alumel (composed of Nickel and Aluminum), Chromel (composed of Nickel and Chromium) and Constantan (composed of Copper and Nickel).

## SOME COMMON THERMOCOUPLES

JUNCTION MATERIALS	TYPICAL USEFUL RANGE (°C)	VOLTAGE SWING OVER RANGE (mV)	ANSI DESIGNATION
Platinum-6% Rhodium / Platinum-30% Rhodium	38 to 1800	13.6	B
Tungsten-5% Rhenium / Tungsten-26% Rhenium	0 to 2300	37.0	(C)
Chromel / Constantan	0 to 982	75.0	E
Iron / Constantan	-184 to 760	50.0	J
Chromel / Alumel	-184 to 1260	56.0	K
Platinum / Platinum-13% Rhodium	0 to 1593	18.7	R
Platinum / Platinum-10% Rhodium	0 to 1538	16.0	S
Copper / Constantan	-184 to 400	26.0	T

Figure 9.33

Figure 9.34 shows the voltage-temperature curves of four commonly used thermocouples, referred to a 0°C fixed-temperature reference junction. Of the thermocouples shown, Type J thermocouples are the most sensitive, producing the largest output voltage for a given temperature change. On the other

hand, Type S thermocouples are the least sensitive. These characteristics are very important to consider when designing signal conditioning circuitry in that the thermocouples' relatively low output signals require low-noise, low-drift, high-gain amplifiers.



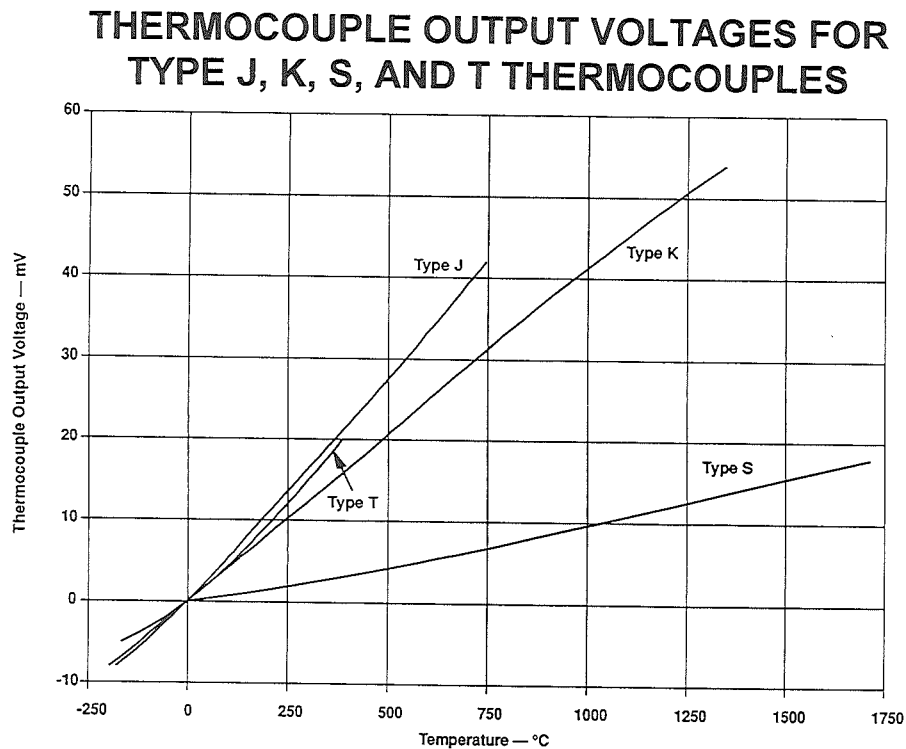


Figure 9.34

To understand thermocouple behavior, it is necessary to consider the non-linearities in their response to temperature differences. Figure 9.34 shows the relationships between sensing junction temperature and voltage output for a number of thermocouple types (in all cases, the reference *cold* junction is maintained at 0°C). It is evident that the responses are not quite linear, but the nature of the non-linearity is not so obvious.

Figure 9.35 shows how the Seebeck coefficient (the *change* of output voltage

with *change* of sensor junction temperature - i.e., the first derivative of output with respect to temperature) varies with sensor junction temperature (we are still considering the case where the reference junction is maintained at 0°C).

When selecting a thermocouple for making measurements over a particular range of temperature, we should choose a thermocouple whose Seebeck coefficient varies as little as possible over that range.

## THERMOCOUPLE SEEBECK COEFFICIENT VERSUS TEMPERATURE

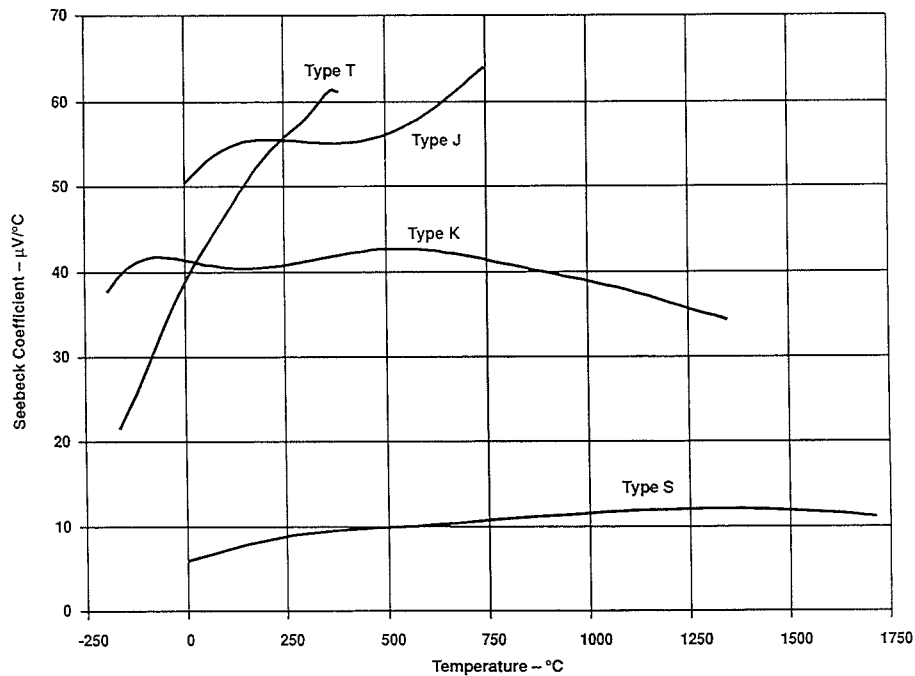


Figure 9.35

To consider two examples: a Type J thermocouple has a Seebeck coefficient which varies by less than  $1\mu\text{V}/^\circ\text{C}$  between 200 and  $500^\circ\text{C}$ , which makes it ideal for measurements in this range; a Type T thermocouple, on the other hand, has a Seebeck coefficient which increases steadily with increasing temperature, making its output non-linear (but predictably non-linear) over any range. A Type T (copper-constantan) device is useful, though, despite its non-linearity, because its materials are cheap, and one of them (copper) is widely used as an electrical conductor.

Presenting these data on thermocouples serves two purposes: First, Figure 9.34 illustrates the range and sensitivity of the four thermocouple types so that the

system designer can, at a glance, determine that a Type S thermocouple has the widest useful temperature range, but a Type J thermocouple is more sensitive. Second, the Seebeck coefficients provide a quick guide to a thermocouple's linearity. Using Figure 9.35, the system designer can choose a Type K thermocouple for its linear Seebeck coefficient over the range of  $400^\circ\text{C}$  to  $800^\circ\text{C}$  or a Type S over the range of  $900^\circ\text{C}$  to  $1700^\circ\text{C}$ . The behavior of a thermocouple's Seebeck coefficient is important in applications where variations of temperature rather than absolute magnitude are important. These data also indicate what performance is required of the associated signal conditioning circuitry.

# THERMOCOUPLE PRINCIPLES AND COLD-JUNCTION COMPENSATION

To use thermocouples successfully we must understand their basic principles.

Consider the diagrams in Figure 9.36.

## THERMOCOUPLE BASICS

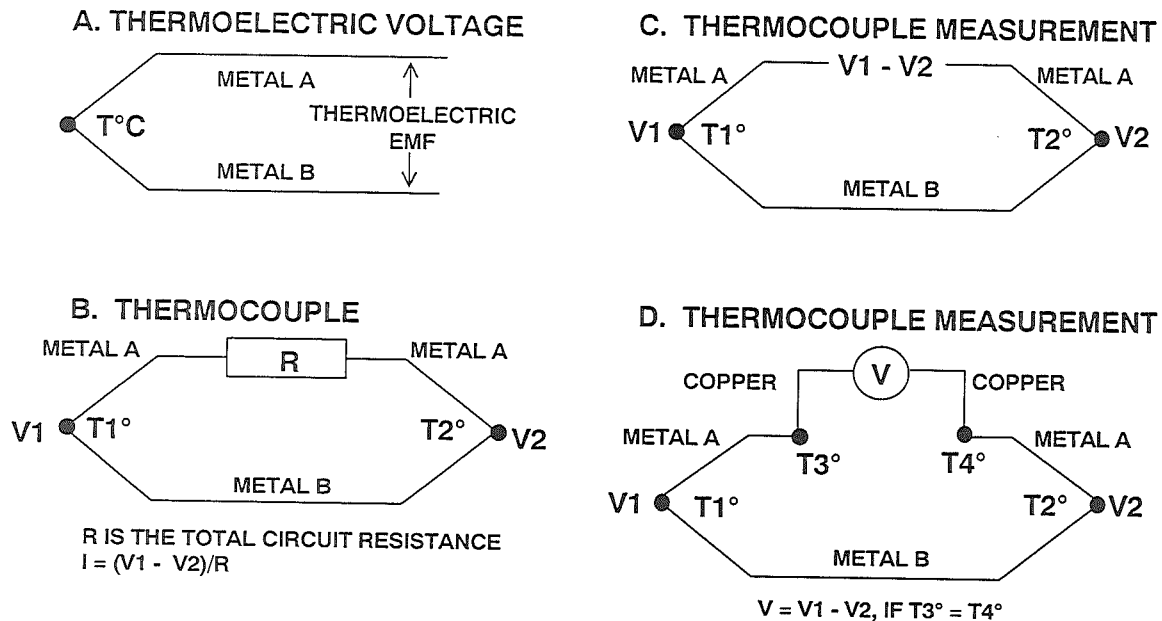


Figure 9.36

If we join two dissimilar metals at any temperature above absolute zero, there will be a potential difference between them (their "thermoelectric e.m.f." or "contact potential") which is a function of the temperature of the junction (Figure 9.36A). A thermocouple consists of two pieces of dissimilar metals (usually two wires) joined at two places. If the two junctions are at different temperatures, there will be a net e.m.f. in the circuit, and a current will flow determined by the e.m.f. and the total resistance in the circuit (Figure 9.36B). If we break one of the wires, the voltage across the break will be equal to the net thermoelectric e.m.f. of the circuit, and if we measure this voltage, we can use it to calculate the temperature difference between the two junctions (Figure

9.36C). We must always remember that a thermocouple measures the temperature difference between two junctions, not the absolute temperature at one junction. We can only measure the temperature at the measuring junction if we know the temperature of the other junction (often called the "reference" junction or the "cold" junction).

But it is not so easy to measure the voltage generated by a thermocouple. Suppose that we attach a voltmeter to the circuit in Figure 9.36C (Figure 9.36D). The wires with which we attach the voltmeter will form further thermojunctions where they are attached. If both these additional junctions are at the same temperature (it does not matter what temperature), then the

“Law of Intermediate Metals” states that they will make no net contribution to the total e.m.f. of the system. If they are at different temperatures, they will introduce errors. Since *every pair of dissimilar metals in contact generates a thermoelectric e.m.f.* (including copper/solder, kovar/copper [kovar is the alloy used for IC leadframes] and aluminum/kovar [at the bond inside the IC]), it is obvious that in practical circuits the problem is even more complex, and it is necessary to take extreme care to ensure that all the junctions in the circuitry around a thermocouple, except the measurement and reference junc-

tions themselves, are at the same temperature.

Thermocouples generate a voltage, albeit a very small one, and do not require excitation. But they do require that the reference junction (often called the “cold” junction, even though, in some systems, it may be at a higher temperature than the measurement junction!) be at a well-defined temperature. A conceptually simple approach to this need is shown in Figure 9.37, but although an ice/water bath is easy to define, it is inconvenient to maintain.

### CLASSICAL COLD-JUNCTION COMPENSATION USING AN ICE-POINT (0°C) REFERENCE JUNCTION

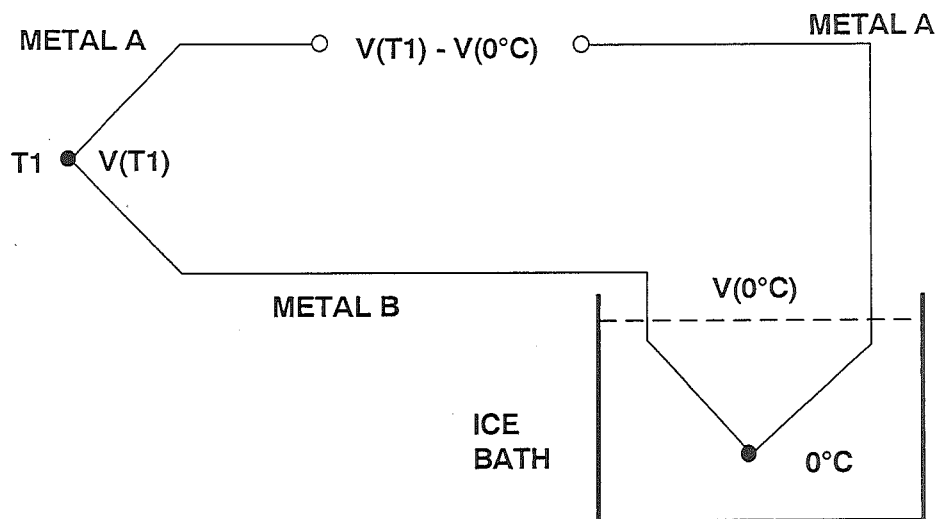


Figure 9.37

Today an ice-point reference, and its inconvenient ice/water bath, is generally replaced by electronics. A temperature sensor of another sort (often a semiconductor sensor, sometimes a thermistor) measures the temperature of the cold junction and is used to inject a voltage into the thermocouple circuit which compensates for the difference between the actual cold junction temperature and its ideal value (usually 0°C). Ideally, the compensation voltage should be an exact match for the difference voltage required, which is why the diagram gives the voltage as  $f(T_2)$  (a *function* of  $T_2$ ) rather than  $KT_2$ , where  $K$  is a simple constant. In practice, since the cold junction is rarely more than a few tens of degrees from 0°C, and generally varies by little more than  $\pm 10^\circ\text{C}$ , a linear approximation ( $V=KT_2$ ) to the more complex reality is suffi-

ciently accurate and is what is often used. (The expression for the output voltage of a thermocouple with its measuring junction at  $T^\circ\text{C}$  and its reference at  $0^\circ\text{C}$  is a polynomial of the form  $V = K_1T + K_2T^2 + K_3T^3 + \dots$ , but the values of the coefficients  $K_2$ ,  $K_3$ , etc. are very small for most common types of thermocouple. References 8 and 17 give the values of these coefficients for a wide range of thermocouples.) Some thermocouple amplifiers (for example Analog Devices' AD594/5/6/7 series) incorporate cold junction compensation in the IC amplifier - with such devices it is very important that the IC chip is at the same temperature as the cold junction of the thermocouple, which is usually achieved by keeping the two in close proximity and isolated from any heat sources.

## USING A TEMPERATURE SENSOR FOR COLD-JUNCTION COMPENSATION

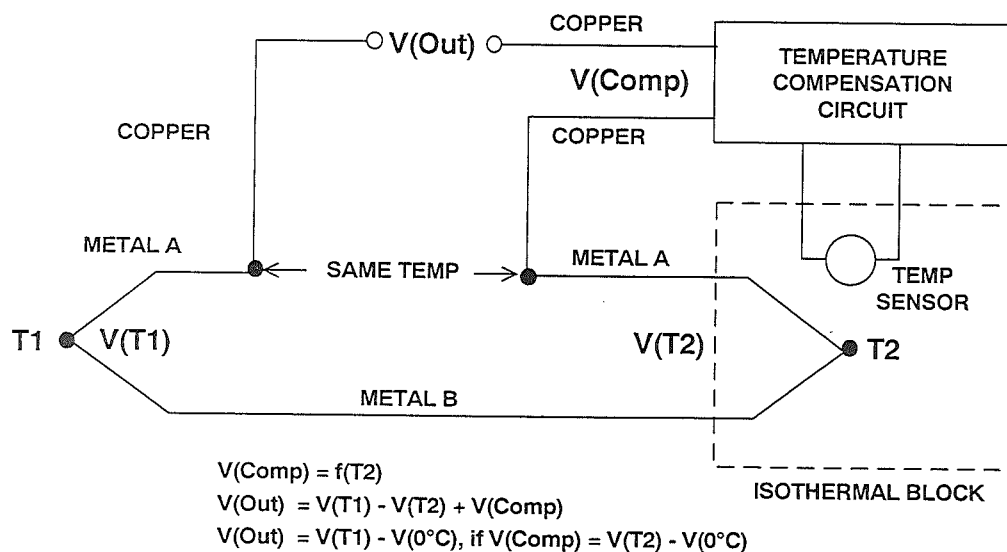


Figure 9.38

When electronic cold-junction compensation is used, it is common practice to eliminate the additional thermocouple

wire and terminate the thermocouple leads in the isothermal block in the arrangement shown in Figure 9.39.

### TERMINATING THERMOCOUPLE LEADS DIRECTLY TO AN ISOTHERMAL BLOCK

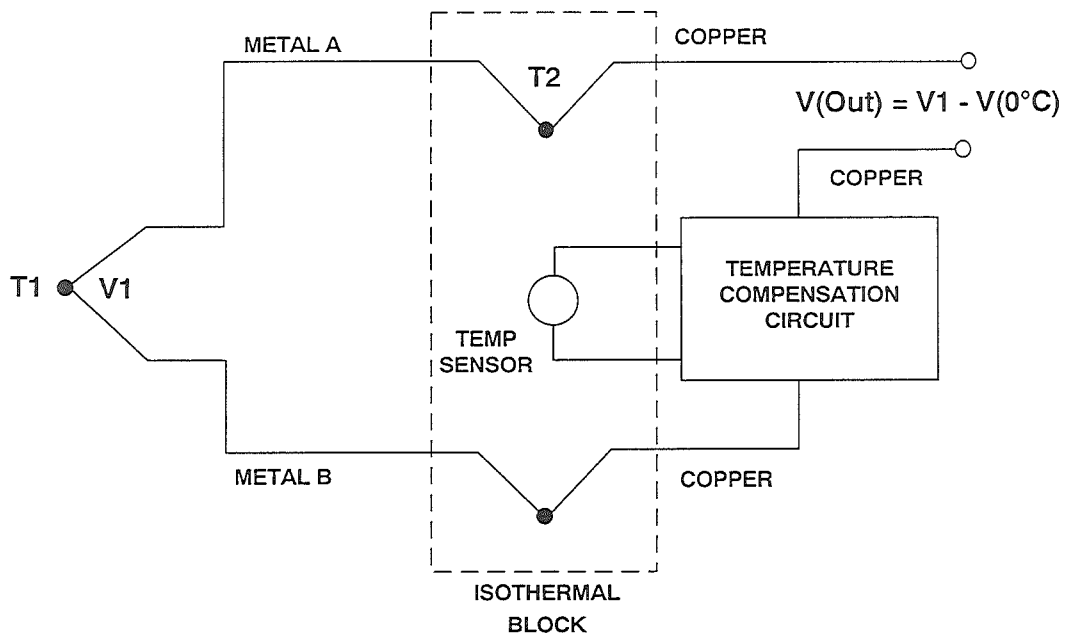


Figure 9.39

### THERMOCOUPLE AMPLIFIER CONSIDERATIONS

There are a number of ways to design thermocouple signal conditioning amplifiers. The appropriate thermocouple for the temperature range is chosen to minimize the accuracy required of the circuit. The selection of the thermocouple which is most linear in the required temperature range permits straightforward designs with a minimum of components. The best way to achieve accurate measurements over narrow or wide temperature ranges is to use cold-junction compensation and a thermocouple whose Seebeck coefficient is linear over the temperature range of

interest. It is not always that straightforward — in many cases, a designer must use whatever thermocouple is available. To illustrate the issues of thermocouple signal conditioning, let us begin by considering a Type T thermocouple amplifier.

Once the measurement temperature range is known, the next step is to decide what type of linearization must be applied to the thermocouple's non-linear output. Thermocouples do not have a constant Seebeck coefficient over temperature, and some type of linear

approximation must be used to linearize them. The first example is a signal conditioning amplifier for a Type T thermocouple which measures temperatures over the range of 0°C to 100°C. In

Figure 9.40, a Type T thermocouple response is shown with two linear approximations: end-point and least squares.

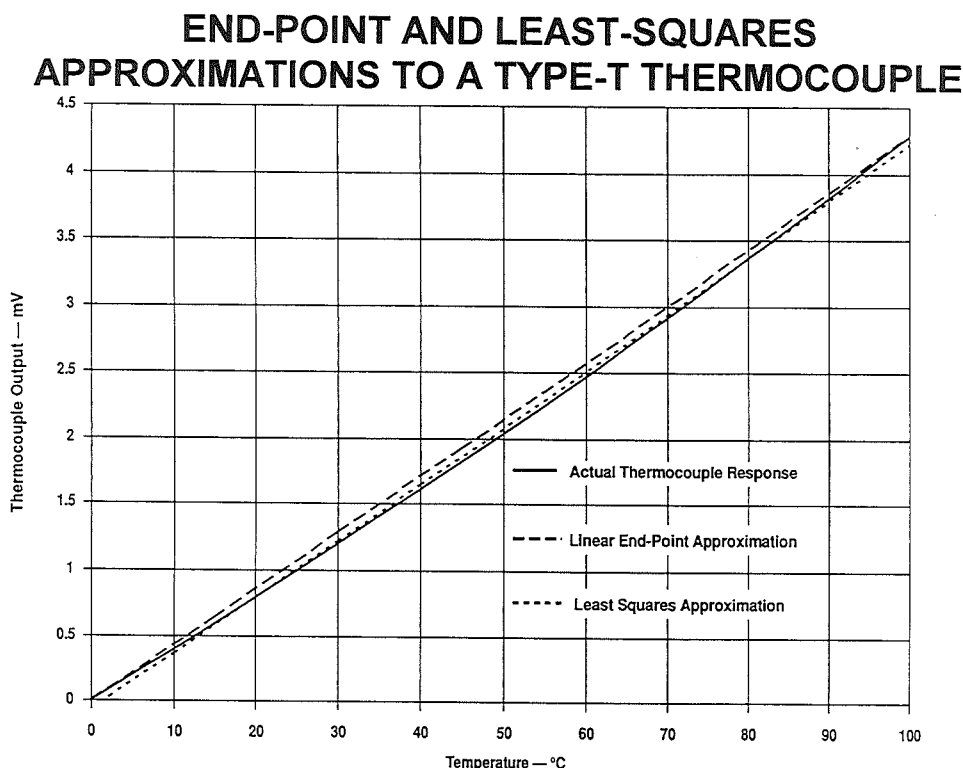


Figure 9.40

An end-point approximation consists of a straight line between the two end-points of the temperature range. The error is zero at the endpoints and is a maximum at the midpoint of the range,  $-2.5^{\circ}\text{C}$  at  $50^{\circ}\text{C}$  in this example. The slope of the line is  $42.8\mu\text{V}/^{\circ}\text{C}$ , and this is the Seebeck coefficient value used when the cold-junction compensator is designed. On the other hand, a least squares approximation to the thermocouple's response intersects the response at two points and exhibits a minimum mean-square error over the temperature range of interest. The error in this example is zero at  $20^{\circ}\text{C}$

and at  $80^{\circ}\text{C}$ , with the maximum error at the midpoint and the endpoints. Typically with this approach the error becomes too large at either temperature extreme, and the designer is forced to adjust the slope or the intercept to reduce the overall error. Fortunately, many scientific calculators provide a least squares curve fitting capability. The algorithm only works if there are enough data points. In this example, data points were in  $5^{\circ}\text{C}$  increments from  $0^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ , and the approximation yielded an error of  $-1.5^{\circ}\text{C}$  at the endpoints and  $+0.9^{\circ}\text{C}$  at midscale. The Seebeck coefficient is  $42.8\mu\text{V}/^{\circ}\text{C}$ , and

the intercept is  $-65 \mu\text{V}$ . The only difference between the two approximations is the offset. The only way to reduce the error in the approximation is to reduce the measurement temperature range or use linearization techniques. This example shows that linear approximations to a thermocouple's characteristic are accurate for small temperature ranges.

coefficient of  $42.8 \mu\text{V}/^\circ\text{C}$  is used in a circuit which measures temperature over the range  $0^\circ\text{C}$  to  $100^\circ\text{C}$  to an accuracy of  $\pm 0.4^\circ\text{C}$ . The amplifier, shown in Figure 9.41, is designed to provide a  $10\text{mV}/^\circ\text{C}$  output and requires a gain of 233.8. Changing  $R_3$  as shown in the table allows the circuit to work with other types of thermocouples.

To illustrate the design of a Type T thermocouple amplifier, a Seebeck

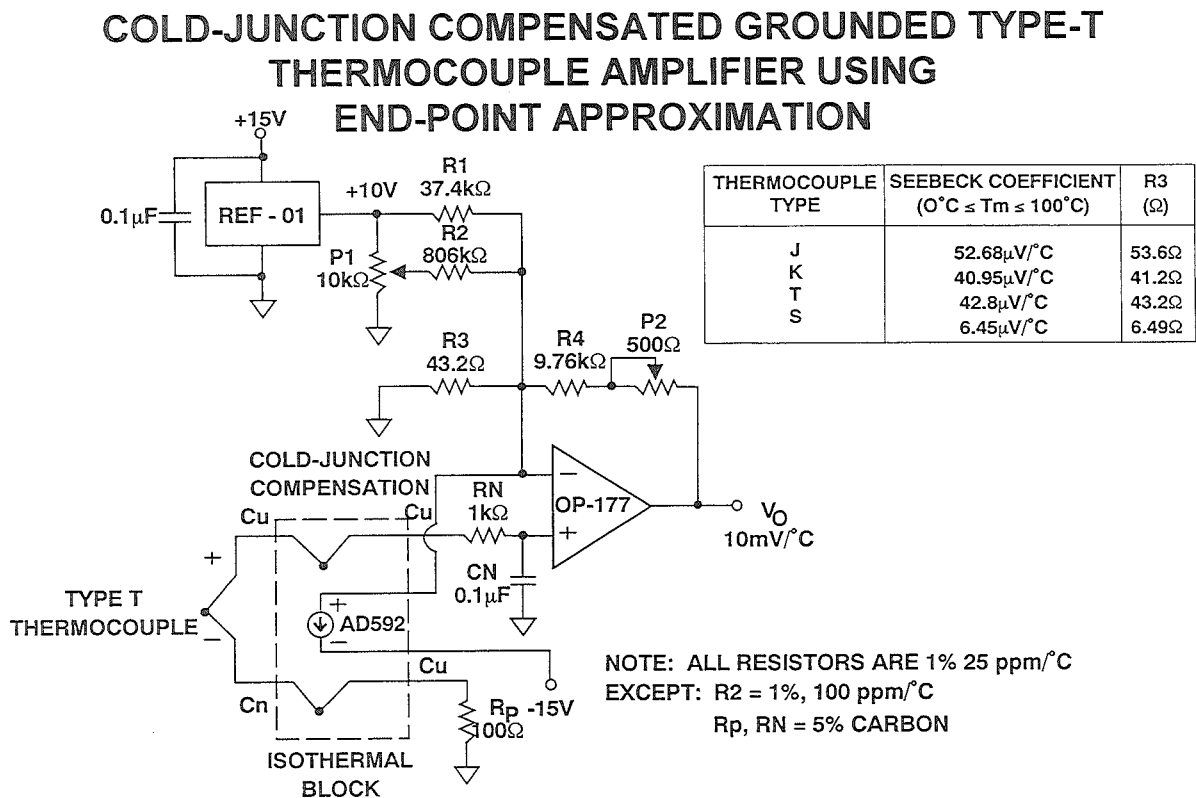


Figure 9.41

A grounded thermocouple is used here because this minimizes noise pickup from long leads.  $R_N$  and  $C_N$  serve as a noise filter to any noise that the lead wires pick up. The cutoff frequency of 1.6kHz can be lowered by increasing  $C_N$ . Although larger values of  $R_N$  might be used at the input of the OP-177, they will increase input bias-

current induced offset and drift effects. A resistor,  $R_p$ , is used in series with exposed thermocouples as protection against contact with some high potential.

Cold-junction compensation uses an AD592 monolithic temperature sensor at the thermocouple's reference (cold)



junction. The sensor monitors the temperature of the cold-junction and provides a temperature-dependent current to the amplifier's summing junction. An offset current nulling the sensor's output current at 0°C is produced by R1 and a precision 10V reference.

Calibration of the circuit is a two-step process. First, the circuit is allowed to warm-up for 5 minutes to allow the temperature sensor, reference, resistors, and op amp to stabilize. To protect the circuit from ambient thermal gradients or air currents, which can affect calibration, the circuit should be covered or enclosed in a box. For 0°C calibration, the thermocouple terminals are short-circuited, and P1 is adjusted such that the output voltage equals the temperature of the isothermal block, according to the relationship  $10\text{mV}/^\circ\text{C} \cdot T_A$ . This trims out amplifier offset voltage and bias currents, resistor tolerances, and errors in the reference and the temperature sensor. For full-scale adjustment, the short is replaced by a precision dc voltage source set to the thermocouple's output voltage at 100°C. For a Type T thermocouple, the voltage is 4.277mV. P2 is then adjusted such that the output voltage is 1V above its previously measured value; that is,  $V_{\text{OUT}} = 1\text{V} + 10\text{mV}/^\circ\text{C} \cdot T_A$ . For example, if the ambient temperature of the factory or lab is 45°C (whew!!), then P2 is adjusted so that  $V_{\text{OUT}} = 1.45\text{V}$ . The temperature of the isothermal block must not change during calibration.

The largest source of error over this temperature range comes from the approximation made to the thermocouple's characteristic. As we have shown, a Type T thermocouple exhibits a Seebeck coefficient of  $38.9\mu\text{V}/^\circ\text{C}$  at 0°C that increases to  $46.3\mu\text{V}/^\circ\text{C}$  at 100°C. Therefore, using a constant  $42.8\mu\text{V}/^\circ\text{C}$  over this range induces a

$2.5^\circ\text{C}$  error in the measurements. A Type K characteristic induces less than a  $0.7^\circ\text{C}$  error, and a Type J characteristic induces less than  $1^\circ\text{C}$  error. In applications where the output is digitized, it may be made more accurate by using software linearization with correction factors stored in a lookup table.

The OP-177 is an excellent choice for this application for a number of reasons: (1) its low input bias current allows the use of a filter and current limiting without generating large parasitic offset voltages and drift; (2) its low input offset voltage reduces static errors at the output, and its low offset drift contributes less than  $0.06^\circ\text{C}$  error for ambient temperatures between 20°C and 50°C; and (3) the amplifier's open-loop gain of greater than 5 million keeps the amplifier's gain error below  $0.004^\circ\text{C}$  over the entire ambient temperature range.

The AD594/AD595 is a complete instrumentation amplifier and thermocouple cold junction compensator on a monolithic chip. It combines an ice point reference with a precalibrated amplifier to provide a high level ( $10\text{mV}/^\circ\text{C}$ ) output directly from the thermocouple signal. Pin-strapping options allow it to be used as a linear amplifier-compensator or as a switched output set-point controller using either fixed or remote set-point control. It can be used to amplify its compensation voltage directly, thereby becoming a stand-alone Celsius transducer with  $10\text{mV}/^\circ\text{C}$  output.

The AD594/AD595 includes a thermocouple failure alarm that indicates if one or both thermocouple leads become open. The alarm output has a flexible format which includes TTL drive capability. The device can be powered from a single-ended supply (which may be as low as +5V), but by including a negative

supply, temperatures below 0°C can be measured. To minimize self-heating, an unloaded AD594/AD595 will operate with a supply current of 160μA, but is also capable of delivering ±5mA to a load.

The AD594 is precalibrated by laser wafer trimming to match the characteristics of type J (iron/constantan) thermocouples, and the AD595 is laser trimmed for type K (chromel/alumel). The temperature transducer voltages and gain control resistors are available at the package pins so that the circuit

can be recalibrated for other thermocouple types by the addition of resistors. These terminals also allow more precise calibration for both thermocouple and thermometer applications. The AD594/AD595 is available in two performance grades. The C and the A versions have calibration accuracies of ±1°C and ±3°C, respectively. Both are designed to be used with cold junctions between 0 to +50°C. The circuit shown in Figure 9.42 will provide a direct output from a type J thermocouple (AD594) or a type K thermocouple (AD595) capable of measuring 0 to +300°C.

## AD594/AD595 MONOLITHIC THERMOCOUPLE AMPLIFIERS WITH COLD-JUNCTION COMPENSATION

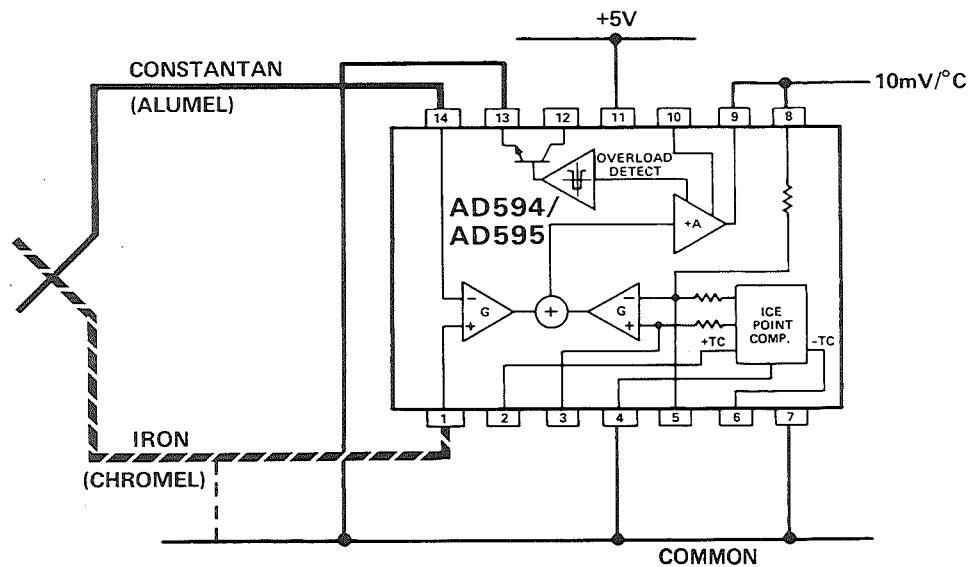


Figure 9.42

The AD596/AD597 are monolithic set-point controllers which have been optimized for use at elevated temperatures as are found in oven control applications. The device cold-junction compensates and amplifies a type J or K thermocouple to derive an internal signal proportional to temperature. They can be configured to provide a voltage output (10mV/°C) directly from type J or K thermocouple signals. The device is packaged in a 10-pin metal can

and is trimmed to operate over an ambient range from +25°C to +100°C. The AD596 will amplify thermocouple signals covering the entire -200°C to +760°C temperature range recommended for type J thermocouples while the AD597 can accommodate -200°C to +1250°C type K inputs. They have a calibration accuracy of  $\pm 4^\circ\text{C}$  at an ambient temperature of 60°C and an ambient temperature stability specification of  $0.05^\circ\text{C}/^\circ\text{C}$  from +25°C to +100°C.

## MAINTAINING PROPER COLD-JUNCTION COMPENSATION

One of the largest sources of error in thermocouple signal conditioning circuits is poor cold-junction compensation. Since a thermocouple output voltage is a function of the temperature difference between its two junctions, any temperature difference between the reference junction and the cold-junction temperature sensor will produce an error signal.

It is therefore essential that the layout of the temperature sensor and the thermocouple reference junction minimizes any temperature gradients. Errors are often introduced when the cold junction is not properly transferred to the PC board. An example of correct transfer of the cold junction to the PC board is shown in Figure 9.43.

## TRANSFERRING THE COLD-JUNCTION FROM AN ENCLOSURE OR CONNECTOR TO THE PC BOARD

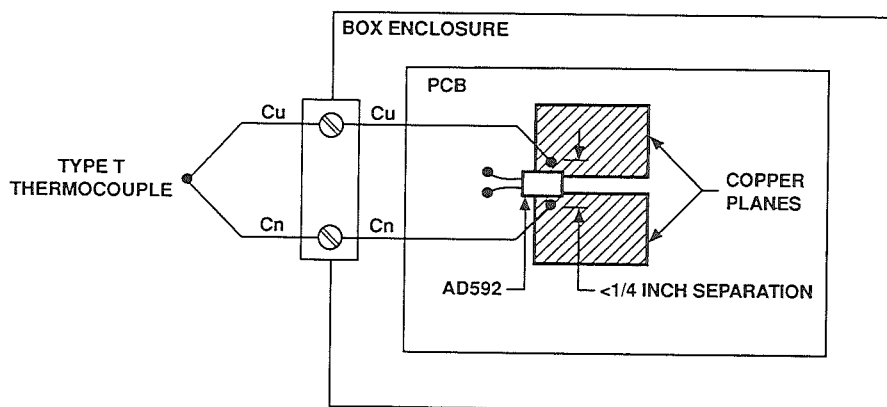


Figure 9.43

The layout illustrates how to extend the cold-junction reference from the terminal block (or connector) to the PC board, and how to locate the temperature sensor relative to the thermocouple

reference junction. The wires from the terminal block (or connector) to the PC board must be of the same material as that used for the thermocouple wires.

## MINIMIZING PARASITIC PCB THERMOCOUPLE ERRORS

Thermojunction voltages are generated whenever dissimilar conductors make contact. There are many such contacts in an electronic circuit board, where conductors include copper, kovar and alloy-42 (IC leads), aluminum (IC Bond wires), solder, plating (gold, nickel, silver and others), nichrome and cer-mets (in resistors), and brass and steel (in terminal blocks). Circuit boards are therefore full of unnoticed thermocouples. If they are all at the same temperature, their net effect is zero, but in reality all PC boards have innumerable temperature gradients, and thermocouple effects can seriously affect the accuracy of low-level DC measurements, including thermocouple measurements.

When designing such boards, the engineer should ensure that no temperature gradients exist which might induce thermoelectric voltages and so affect the accuracy of the system. If temperature gradients cannot be eliminated (the usual case), junctions and components should be placed isothermally and as close together as possible, especially the

cold-junction sensor, the cold-junction itself, the amplifier input leads, and the gain resistor, so that parasitic thermoelectric voltages cancel out. Figure 9.44 is an example of a printed circuit board layout of the circuit in Figure 9.41 illustrating the isothermal placing and close location of the thermocouple terminating junction, the temperature sensor, the amplifier input pins, and the gain setting resistors.

Beware of amplifier offset voltage warm-up drift caused by mismatched materials in the wire bond/lead system of an IC package. This effect can be as high as tens of microvolts in TO-5 cans with Kovar leads. It has nothing to do with the actual offset drift specification and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation and can be minimized by avoiding TO-5 cans, using low-supply current amplifiers, and by using the lowest possible supply voltages. Its effects be minimized by calibrating and specifying the system after a warm-up period.

## PROPERLY LOCATING ALL COMPONENTS THAT ARE SENSITIVE TO THERMAL GRADIENTS

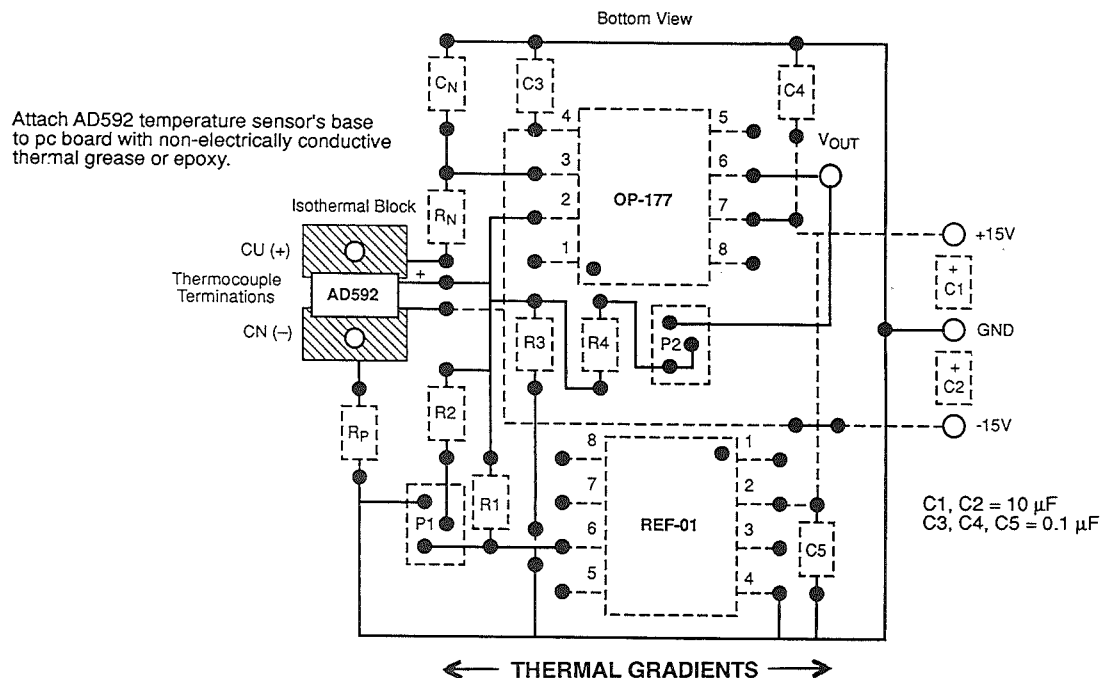


Figure 9.44

## THERMOCOUPLE LINEARIZATION TECHNIQUES

To improve accuracy, the thermocouple's response can be linearized. There are a number of techniques that can be used to linearize a thermocouple, including breakpoint correction, analog computation, and digital correction (Reference 5).

Thermocouple non-linearity correction using analog computation makes use of analog multipliers and operational amplifiers to synthesize a function that models the thermocouple's voltage-temperature characteristic. For more detailed information on this subject, the

reader should consult References 2 and 6.

Another technique for linearizing a thermocouple's response is to use breakpoints that change the gain of the circuit as the signal increases. Breakpoints use as many straight-line segments as are required by system accuracy to fit the thermocouple characteristic. This approach is circuit intensive: the number of linear segments determines the number of amplifiers the linearizer requires (see Section 2 of Reference 3).

An increasingly popular technique for thermocouple linearization is to digitize the output of an accurate thermocouple amplifier and apply continuous correction to thermocouple output with factors that are stored in ROM (Reference 7 and 18). One method uses a power series polynomial to implement the correction and has the form:

$$T = a_0 + a_1X + a_2X^2 + \dots + a_nX^n$$

where  $T$  is the thermocouple temperature,  $X$  is the thermoelectric voltage, and  $a_0, a_1, a_2, \dots$ , and  $a_n$  are the coefficients of the polynomial for each type of ther-

mocouple. The coefficients for each thermocouple can be found in References 8 and 17. Another advantage of digital techniques is the elimination of trimming potentiometers. Computers and microprocessors can be programmed to execute a calibration sequence at any time and are far more efficient than analog linearization circuits in this application. Digital signal conditioners such as the AD1B60 (to be described shortly) provide complete signal conditioning and provide software linearization for a number of sensors.

## RESISTANCE TEMPERATURE DETECTOR (RTD) SIGNAL CONDITIONING

The Resistance Temperature Detector, or the RTD, is a sensor whose resistance changes with temperature. Typically built of a platinum (Pt) wire wrapped around a ceramic bobbin, the RTD exhibits behavior which is more accurate and more linear over wide temperature ranges than a thermocouple. Figure 9.45 illustrates the temperature coefficient of a 100-ohm RTD and the Seebeck coefficient of a Type S thermocouple. Over the entire range (approximately  $-200^\circ\text{C}$  to  $+850^\circ\text{C}$ ), the RTD is a more linear device. Hence, linearizing an RTD is less complex.

Unlike a thermocouple, however, an RTD is a passive sensor and requires current excitation to produce an output voltage. The RTD's low temperature coefficient of  $0.385\%/^\circ\text{C}$  requires similar high-performance signal conditioning circuitry to that used by a thermocouple; however, the voltage drop across an RTD is much larger than a thermocouple output voltage. A system designer may opt for large value RTDs with higher output, but large-

valued RTDs exhibit slow response times. Furthermore, although the cost of RTDs is higher than that of thermocouples, they use copper leads, and thermoelectric effects from terminating junctions do not affect their accuracy. And finally, because their resistance is a function of the absolute temperature, RTDs require no cold-junction compensation.

Caution must be exercised using current excitation because the current through the RTD causes heating. This self-heating changes the temperature of the RTD and appears as a measurement error. Hence, careful attention must be paid to the design of the signal conditioning circuitry so that self-heating is kept below  $0.5^\circ\text{C}$ . Manufacturers specify self-heating errors for various RTD values and sizes in still and in moving air. To reduce the error due to self-heating, the minimum current should be used for the required system resolution, and the largest RTD value chosen that results in acceptable response time.

## LINEARITY COMPARISON BETWEEN PLATINUM RTD AND TYPE-S THERMOCOUPLE

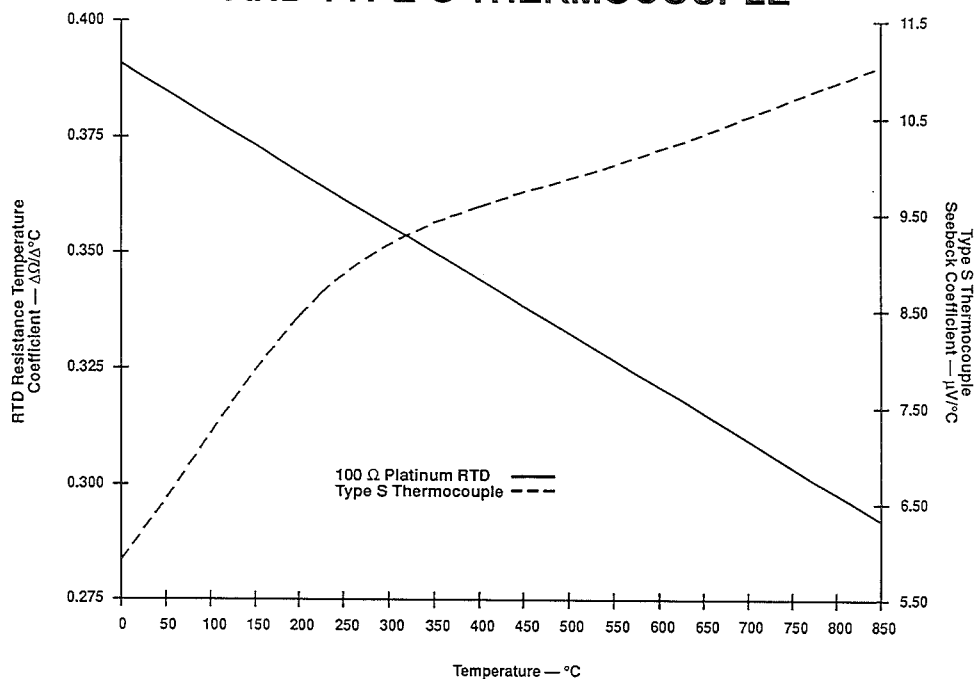
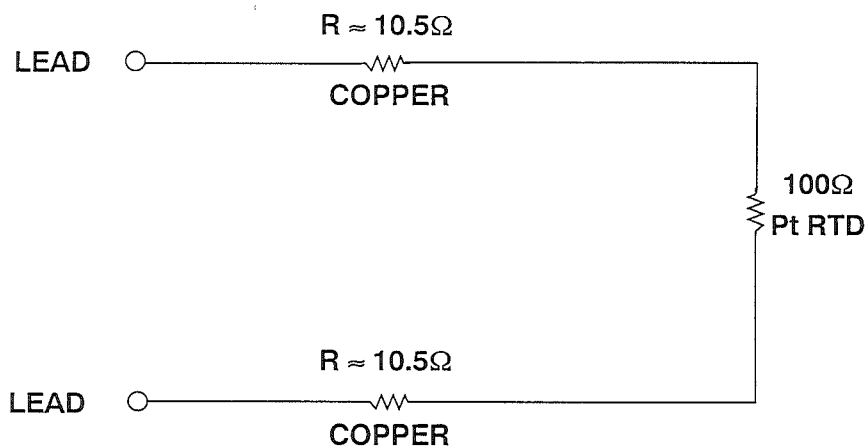


Figure 9.45

Another effect that can produce measurement error is voltage drop in RTD lead wires. This is especially critical with low-value 2-wire RTDs because the temperature coefficient and the absolute value of the RTD resistance are both small. If the RTD is located a long distance from the signal conditioning circuitry, then the lead resistance can be ohms or tens of ohms, and a small amount of lead resistance can contribute a significant error to the temperature measurement. To illustrate this point, let us assume that a 100Ω plati-

num RTD with 30-gauge copper leads is located about 100 feet from a controller's display console. The resistance of 30-gauge copper wire is 0.105Ω/ft, and the two leads of the RTD will contribute a total 21Ω to the network which is shown in Figure 9.46. This additional resistance will produce a 55°C error in the measurement! The leads' temperature coefficient can contribute an additional, and possibly significant, error to the measurement. To eliminate the effect of the lead resistance, a 4-wire technique is used.

## A 100Ω PLATINUM RTD WITH 100 FEET OF 30-GAUGE LEAD WIRES



RESISTANCE TC OF COPPER  $\approx 0.4\%/^{\circ}\text{C}$  @  $20^{\circ}\text{C}$

Figure 9.46

## FOUR-WIRE OR KELVIN CONNECTION TO RTD

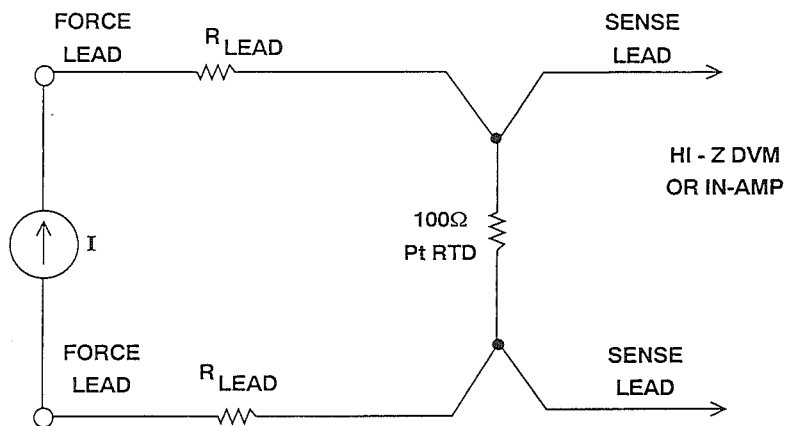


Figure 9.47



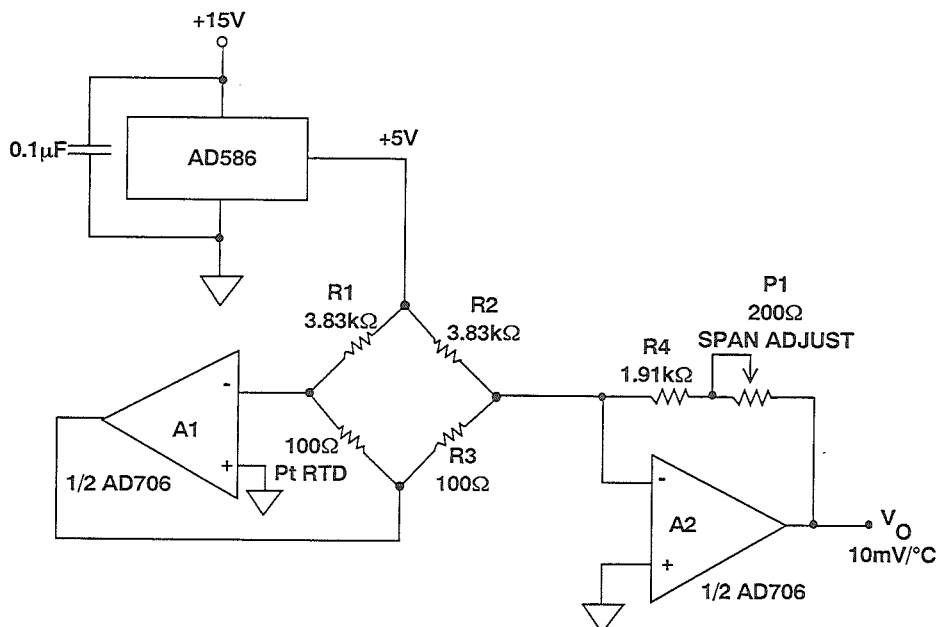
In Figure 9.47, a 4-wire, or Kelvin, connection is made to the RTD. A constant current is applied through the FORCE leads of the RTD and the voltage across the RTD itself is measured remotely via the SENSE leads. The measuring device can be a DVM or an instrumentation amplifier, and high accuracy can be achieved provided that the measuring device exhibits high input impedance and/or low input bias current. Since the SENSE leads do not carry appreciable current, this technique is insensitive to lead wire length. Sources of errors are the stability of the constant current source and the input impedance and/or bias currents in the amplifier or DVM.

Bridge circuits used in RTD signal conditioning effectively linearize trans-

ducer outputs. They do not compensate for a major source of bridge-instrumentation error: an operational amplifier's  $V_{OS}$  drift. In many bridge designs, amplifier  $\Delta V_{OS}$  can see four times more gain than the sensor signal because of the bridge's voltage-divider effects.

Without sacrificing linearity, an amplifier's  $\Delta V_{OS}$  can be minimized by applying feedback to the bridge. A pair of op amps can be used to place all bridge elements under fixed bias or feedback control. Shown in Figure 9.48 is a circuit which uses an AD706 dual operational amplifier and a  $100\Omega$  Pt RTD to measure temperature from  $0^\circ\text{C}$  to  $100^\circ\text{C}$ .

### RTD BRIDGE AMPLIFIER



NOTE: ALL FIXED RESISTORS ARE 0.1% IMPERIAL ASTRONICS M015

Figure 9.48

A1 forces a null at one bridge node so that a constant current, defined by the AD586 and R1, flows through the RTD. Amplifier A2 is then used to establish a null at the other bridge node. Therefore, any variation of the RTD resistance generates a signal voltage at the output of A1 which is then converted to a signal current for A2 by R3. This signal current is then summed with the current generated by the reference's 5V output and R2, and the result scaled by R4 to provide a 10mV/°C output. Since the AD706 input bias current is typically 30pA, its error contributions can be neglected.

The circuit's response is dominated by the RTD, and the circuit has a low sensitivity to amplifier input offset voltage and drift. By placing the RTD in the feedback path of A1, A1's input offset voltage effects are effectively suppressed, and the circuit's response is very accurate. Although the output amplifier's  $V_{OS}$  appears at the output, it is not amplified by the same gain as in conventional approaches and introduces less than 0.002°C error at 0°C and <0.04°C error over a 20°C to 50°C range of amplifier temperature.

Calibration of the circuit involves one trim. Because of the AD706 low  $V_{OS}$  (10μV) and the use of precision wirewound resistors, the circuit error at 0°C is less than 0.1°C. Calibration is only required at the full-scale temperature of 100°C. The RTD is replaced by a precision decade resistance box which is set to 138.5Ω. P1 is adjusted such that  $V_O$  equals 1.00V. With this single calibration and 0.1% low-TCR resistors, the measurement error is better than ± 0.2 °C over a 20°C to 50°C ambient temperature range.

Although the servo loop controlled by A1 maintains a constant current in the RTD, this topology does not correct the

non-linearity of the RTD. For example, if this topology were used with the same RTD to measure the range of 0°C to 200°C, curvature of the RTD response will cause a measurement error of approximately 3°C at full scale.

Linearization of RTD outputs can be achieved using op-amps and a small amount of positive feedback. Figure 9.49 shows a single supply circuit to correct the nonlinear behavior of an RTD. The RTD operates in one leg of a full bridge circuit that is excited by a constant current source established by 1/2 of an OP-295 dual op amp. The bridge current is regulated by servoing the current flowing into resistor  $R_{SENSE}$  and comparing with a 200mV reference voltage derived from the REF-43.

The temperature-dependent resistance change is amplified by an instrumentation amplifier, the AMP-04. Scaling is such that for 0°C the amplifier output is 0V, and at 400°C the amplifier output is +4.00V.

The RTD has an inherent non-linearity in its resistance-versus-temperature function. If uncorrected, the sensor nonlinearity would produce a 20°C error over the 400°C temperature range. This nonlinearity can be corrected by providing a small amount of positive feedback to the reference voltage, which increases the bridge current at high temperatures. The amount of positive feedback is so small as not to cause a stability problem.

Calibration is an interactive three-step procedure. The FULL-SCALE and LINEARITY potentiometers are first set to the middle of their adjustment ranges. The first calibration is made with the zero adjust, and must be made at a voltage other than zero, since zero volts is the negative voltage limit of the

## PRECISION SINGLE SUPPLY RTD AMPLIFIER WITH LINEARIZATION

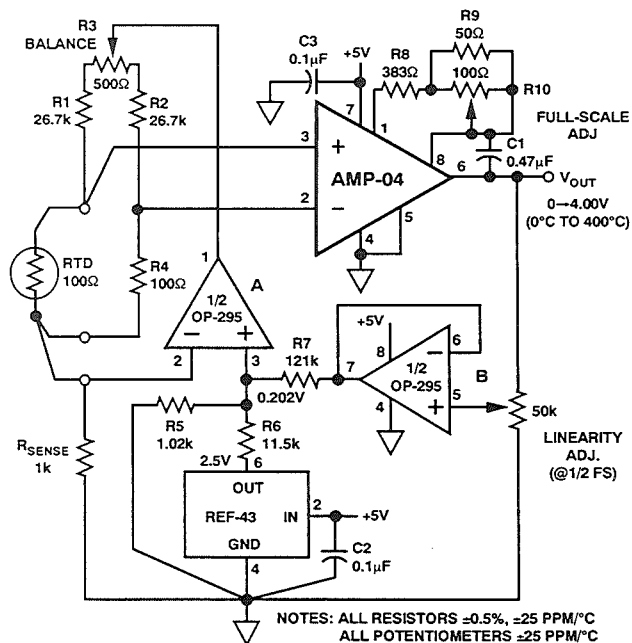


Figure 9.49

## FOUR-WIRE RTD APPLICATION USING THE 22-BIT AD7711 SIGNAL CONDITIONING ADC

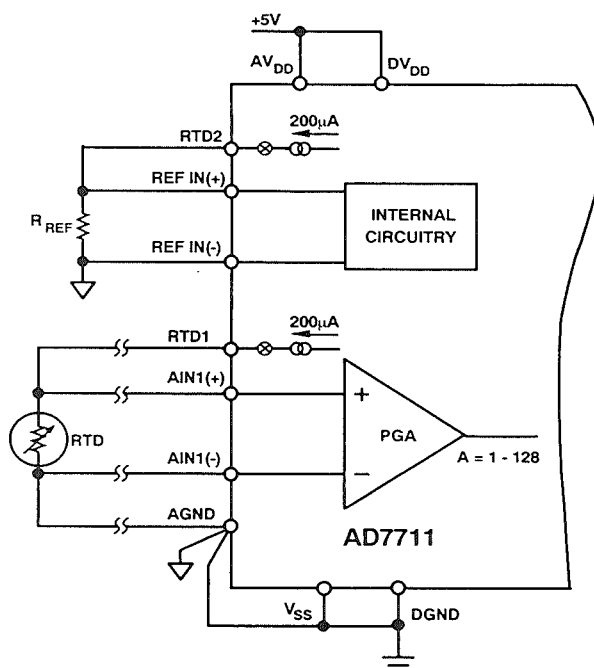


Figure 9.50

circuit. A convenient zero calibration point is  $+5^{\circ}\text{C}$ . Substitute a stable  $101.95\Omega$  resistor for the RTD and then adjust the ZERO ADJUST potentiometer for  $0.050\text{V}$  output.

Next substitute the full-scale ( $400^{\circ}\text{C}$ ) equivalent RTD resistance of  $247.04\Omega$ . Adjust FULL-SCALE ADJUST for  $4.000\text{V}$  output. Then substitute the resistance corresponding to half-scale ( $200^{\circ}\text{C}$ ), or  $175.84\Omega$  and adjust the LINEARITY ADJUST pot for a  $2.000\text{V}$  output. Since the FULL-SCALE and LINEARITY adjustments are interactive, it is necessary to repeat the FULL-SCALE and LINEARITY calibration routine once or twice until no further adjustment is necessary.

Once calibrated, the amplifier is accurate to better than  $\pm 0.5^{\circ}\text{C}$  over the  $0^{\circ}\text{C}$  to  $400^{\circ}\text{C}$  measurement range. If a higher supply voltage is available, the range can be increased.

Highly integrated signal conditioning ADCs, such as the AD7711, can be interfaced directly to RTDs as in Figure 9.50. The 22-bit AD7711 has two internal current sources of  $200\mu\text{A}$  each. In this four-wire configuration, there are no errors associated with lead resistance as no current flows in the measurement leads, which are connected to  $\text{AIN1}(+)$  and  $\text{AIN1}(-)$ . One of the current sources is used to provide the excitation current for the RTD. A  $100\Omega$  RTD will generate a  $20\text{mV}$  signal which can be handled directly by the analog input of the AD7711. The second RTD excitation current is used to generate

the reference voltage. This voltage is developed across  $R_{\text{REF}}$  and applied to the differential reference inputs. For a nominal reference voltage of  $+2.5\text{V}$ ,  $R_{\text{REF}}$  is  $12.5\text{k}\Omega$ . This scheme ensures that the analog input voltage remains ratiometric to the reference voltage. Any errors in the analog input voltage due to temperature drift of the RTD current source are compensated by the variation in the reference voltage. The typical matching between the two RTD current sources varies by less than  $3\text{ppm}/^{\circ}\text{C}$ .

Figure 9.51 shows a simplified block diagram of a complete *intelligent digitizing signal conditioner*, the AD1B60. The device consists of a signal conditioning front end followed by a charge balance ADC and a mask-programmed microcontroller with EEPROM memory. The primary application of the AD1B60 is a user-configurable digitizing signal conditioner for RTDs, thermocouples, and low- and high-level voltage signals. (For a detailed description of the AD1B60, see Section 7 of Reference 4). The AD1B60 provides the algorithms required for scaling and linearizing many types of thermocouples and RTDs. For sensors not included in the built-in routines, a customized linearization algorithm can be created for *any* sensor. Besides its multiplexer, PGA, ADC, and microcontroller, the AD1B60 also provides digitally-controlled current sources for RTD and thermistor excitation and open thermocouple detection, and an internal 5:1 attenuator for high-level input signals (Figure 9.52).

## AD1B60 INTELLIGENT, DIGITIZING SIGNAL CONDITIONER

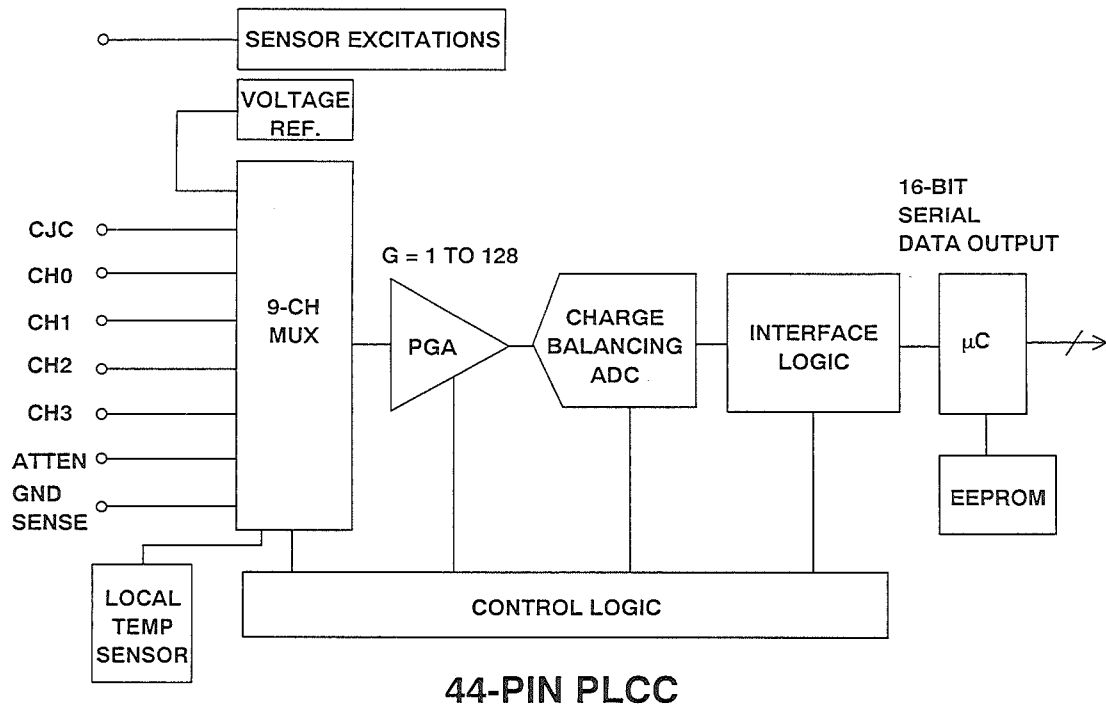


Figure 9.51

## AD1B60 BUILT-IN CONDITIONING CIRCUITS REDUCE OVERALL COMPONENTS COUNT

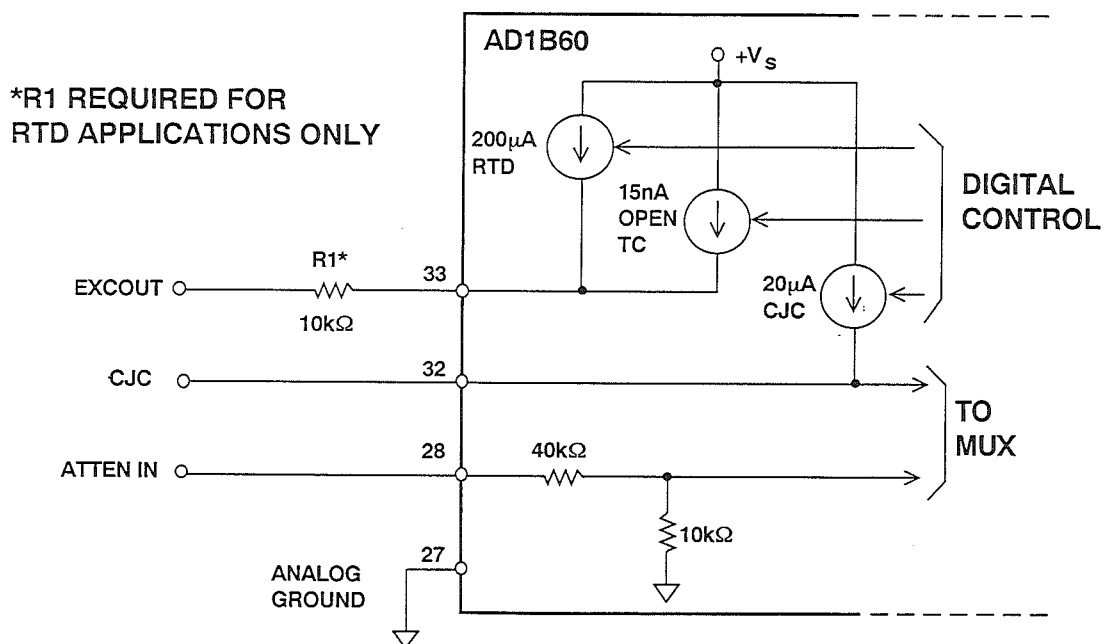


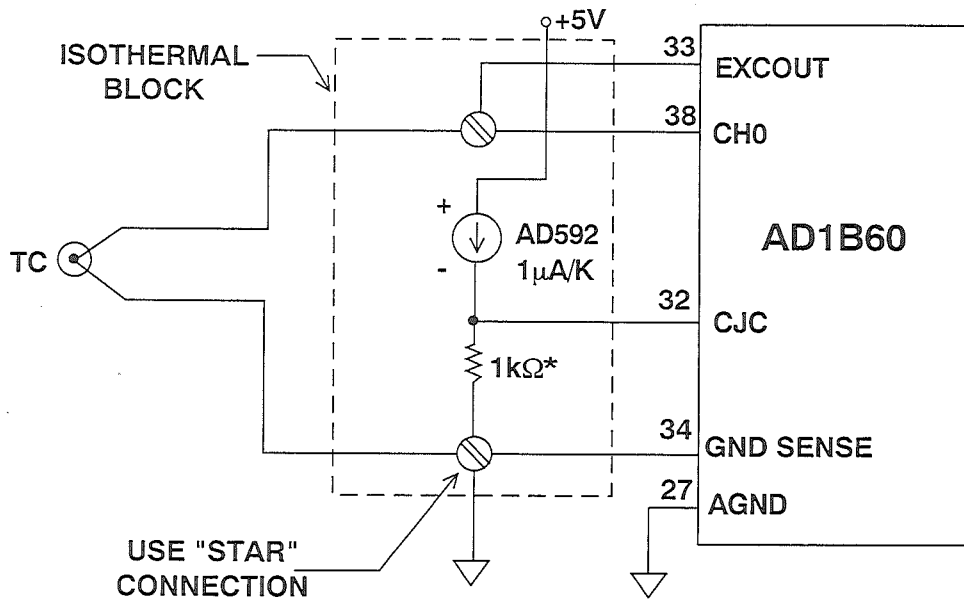
Figure 9.52

Figure 9.53 shows the AD1B60 thermocouple interface using an AD592 temperature sensor for cold junction compensation. The AD592 output current exhibits a temperature coefficient of  $1\mu\text{A/K}$  which develops a voltage across the precision  $1\text{k}\Omega$  resistor to provide the cold junction compensation.

The AD1B60 can accommodate both 3- and 4-wire RTD applications, as shown in Figure 9.54. For three-wire RTD applications, the internal current excitation is connected directly to the RTD FORCE (+) lead wire through a  $10\text{k}\Omega$  resistor. This external resistor need not be a precision type — it serves only to

reduce self-heating. Without this resistor, a gain error of approximately  $0.2^\circ\text{C}$  would be introduced. The RTD's FORCE (+) lead is directly connected to the AD1B60 CH0 input. Only in 3-wire applications is a "star" connection required to minimize additional errors generated by ground loops. The "star" connection is formed by the RTD's FORCE (-) lead wire and the AD1B60's GNDSENSE input connected to the analog ground. In four-wire applications the RTD FORCE(+) lead goes to the  $10\text{k}\Omega$  resistor, its SENSE(+) to CH1, and its SENSE(-) to CH3. There is no star connection, and FORCE(-) goes to GNDSENSE and AGND.

### USING THE AD592 TEMPERATURE SENSOR WITH THE AD1B60 FOR COLD-JUNCTION COMPENSATION



\*PRECISION RESISTOR: 0.01% OR BETTER  
TCR  $\leq 10\text{ppm}/^\circ\text{C}$

Figure 9.53

### 3- AND 4-WIRE RTD CONNECTIONS TO THE AD1B60

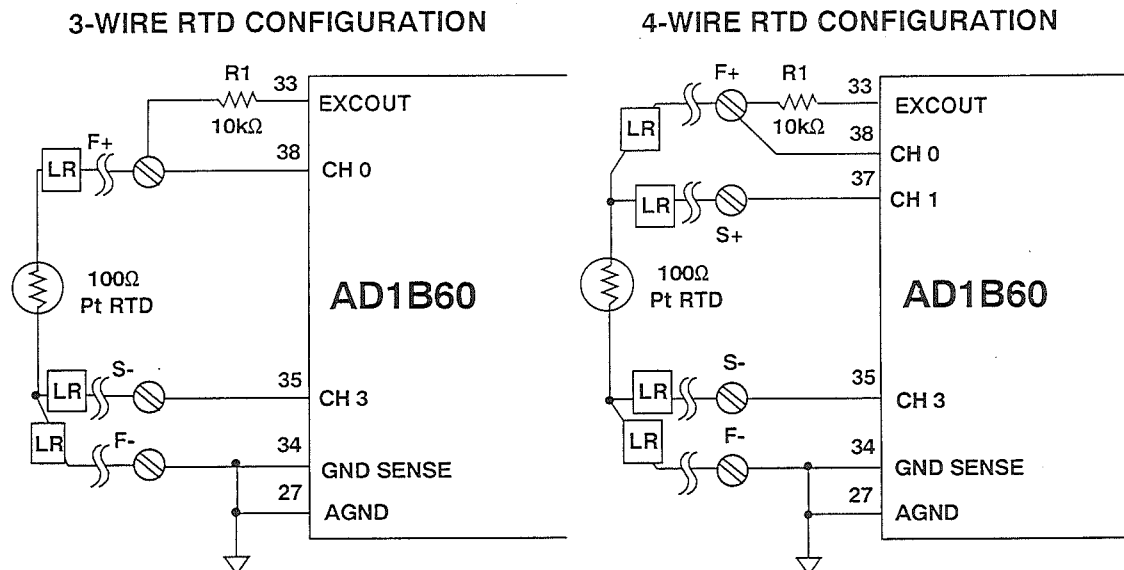


Figure 9.54

A summary of the performance of the AD1B60 (using the built-in lineariza-

tion algorithms) is given in Figure 9.55.

### THE AD1B60'S BUILT-IN ALGORITHMS LINEARIZE THERMOCOUPLE AND RTD OUTPUTS

Thermocouple Type	Temperature Range	Accuracy/Resolution (Typ)
J	$0^{\circ}\text{C} \leq T \leq 760^{\circ}\text{C}$	$\pm 0.25^{\circ}\text{C} / \pm 0.15^{\circ}\text{C}$
K	$0^{\circ}\text{C} \leq T \leq 1000^{\circ}\text{C}$	$\pm 0.55^{\circ}\text{C} / \pm 0.2^{\circ}\text{C}$
T	$-100^{\circ}\text{C} \leq T \leq 400^{\circ}\text{C}$	$\pm 0.25^{\circ}\text{C} / \pm 0.15^{\circ}\text{C}$
E	$0^{\circ}\text{C} \leq T \leq 1000^{\circ}\text{C}$	$\pm 0.2^{\circ}\text{C} / \pm 0.1^{\circ}\text{C}$
R	$500^{\circ}\text{C} \leq T \leq 1750^{\circ}\text{C}$	$\pm 1.00^{\circ}\text{C} / \pm 0.55^{\circ}\text{C}$
S	$500^{\circ}\text{C} \leq T \leq 1750^{\circ}\text{C}$	$\pm 1.15^{\circ}\text{C} / \pm 0.6^{\circ}\text{C}$
B	$500^{\circ}\text{C} \leq T \leq 1800^{\circ}\text{C}$	$\pm 1.15^{\circ}\text{C} / \pm 0.7^{\circ}\text{C}$

100Ω RTD Type	Temperature Range	Accuracy/Resolution (Typ)
$\alpha = 3.85 \text{ m}\Omega/\Omega/^{\circ}\text{C}$	$-200^{\circ}\text{C} \leq T \leq 800^{\circ}\text{C}$	$\pm 0.2^{\circ}\text{C} / \pm 0.15^{\circ}\text{C}$
$\alpha = 3.92 \text{ m}\Omega/\Omega/^{\circ}\text{C}$	$-200^{\circ}\text{C} \leq T \leq 800^{\circ}\text{C}$	$\pm 0.2^{\circ}\text{C} / \pm 0.15^{\circ}\text{C}$

Figure 9.55

## THERMISTOR SIGNAL CONDITIONING

Similar in function to the RTD, thermistors are low-cost temperature-sensitive resistors and are constructed of solid semiconductor materials which exhibit a positive or negative temperature coefficient. Although positive temperature coefficient devices are available, the most commonly used thermistors are those with a negative

temperature coefficient. Figure 9.56 shows the resistance-temperature characteristic of a commonly used NTC (Negative Temperature Coefficient) thermistor. The thermistor is highly non-linear and, of the three temperature sensors discussed, is the most sensitive.

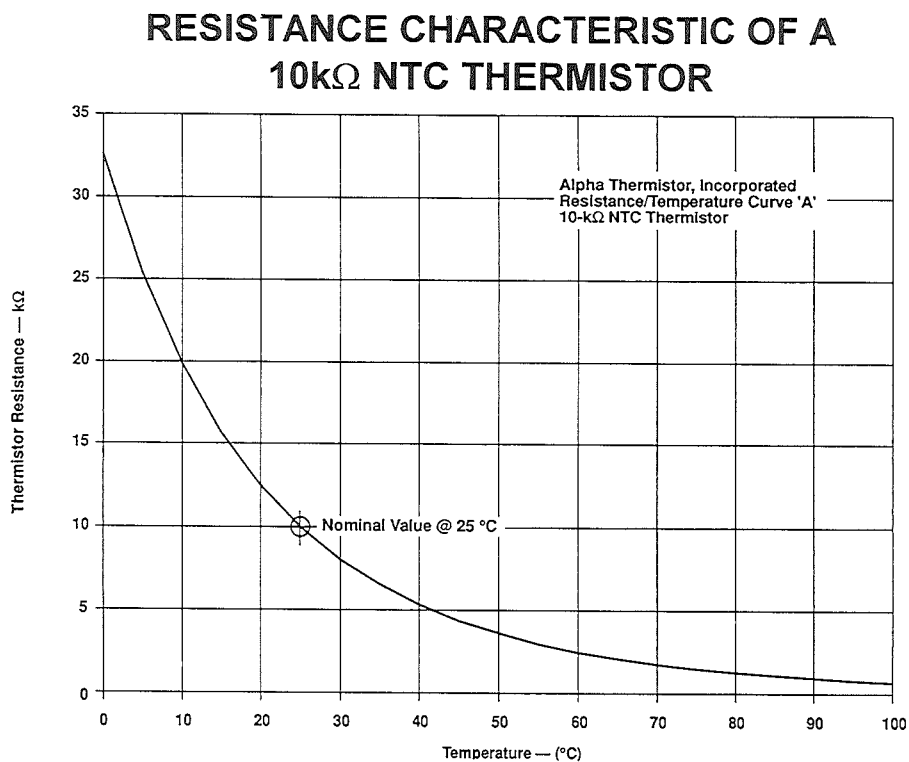


Figure 9.56

The thermistor's high sensitivity (typically,  $-44,000\text{ppm}/^{\circ}\text{C}$  at  $25^{\circ}\text{C}$ , as shown in Figure 9.57), allows it to detect minute variations in temperature which could not be observed with an RTD or thermocouple. This high sensitivity is a distinct advantage over the RTD in that 4-wire Kelvin connections to the thermistor are not needed to compensate for lead wire errors. To

illustrate this point, suppose a  $10\text{k}\Omega$  NTC thermistor, with a typical  $25^{\circ}\text{C}$  temperature coefficient of  $-44,000\text{ppm}/^{\circ}\text{C}$ , were substituted for the  $100\Omega$  Pt RTD in the example given earlier, then a total lead wire resistance of  $21\Omega$  would generate less than  $0.05^{\circ}\text{C}$  error in the measurement. This is roughly a factor of 500 improvement in error over an RTD.



## TEMPERATURE COEFFICIENT OF 10k $\Omega$ NTC THERMISTOR

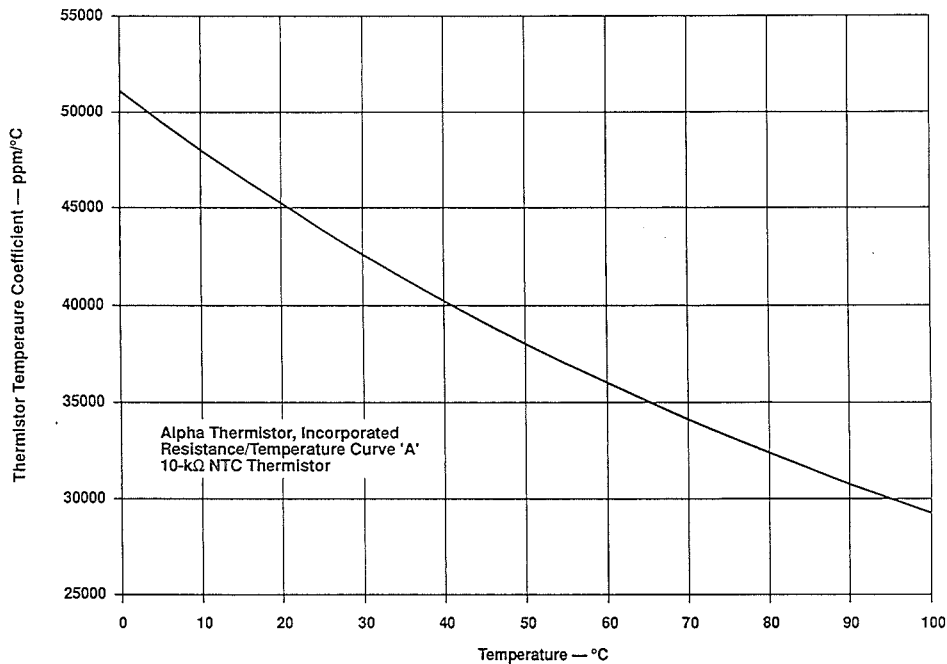


Figure 9.57

However, the thermistor's high sensitivity to temperature does not come without a price. As was shown in Figure 9.57, the temperature coefficient of thermistors does not decrease linearly with increasing temperature as it does with RTDs; therefore, linearization is required for all but the narrowest of temperature ranges. Thermistor applications are limited to a few hundred degrees at best because they are more susceptible to damage at high temperatures. Compared to thermocouples and RTDs, thermistors are fragile in construction and require careful mounting procedures to prevent crushing or bond separation. Although a thermistor's response time is short due to its small size, its small thermal mass makes it very sensitive to self-heating errors.

Thermistors are very inexpensive, highly sensitive temperature sensors.

However, we have shown that a thermistor's temperature coefficient varies from  $-44,000 \text{ ppm/}^\circ\text{C}$  at  $25^\circ\text{C}$  to  $-29,000 \text{ ppm/}^\circ\text{C}$  at  $100^\circ\text{C}$ . Not only is this non-linearity the largest source of error in a temperature measurement, it also limits useful applications to very narrow temperature ranges if linearization techniques are not used.

It is possible to use a thermistor over a wide temperature range only if the system designer can tolerate a lower sensitivity to achieve improved linearity. One approach to linearizing a thermistor is simply shunting it with a fixed resistor. Paralleling the thermistor with a fixed resistor increases the linearity significantly. As shown in Figure 9.58, the parallel combination exhibits a more linear variation with temperature compared to the thermistor itself. Also, the sensitivity of the

combination still is high compared to a thermocouple or RTD. The primary disadvantage to this technique is that

linearization can only be achieved within a narrow range.

### LINEARIZATION OF NTC THERMISTOR USING 5.17kΩ SHUNT RESISTOR

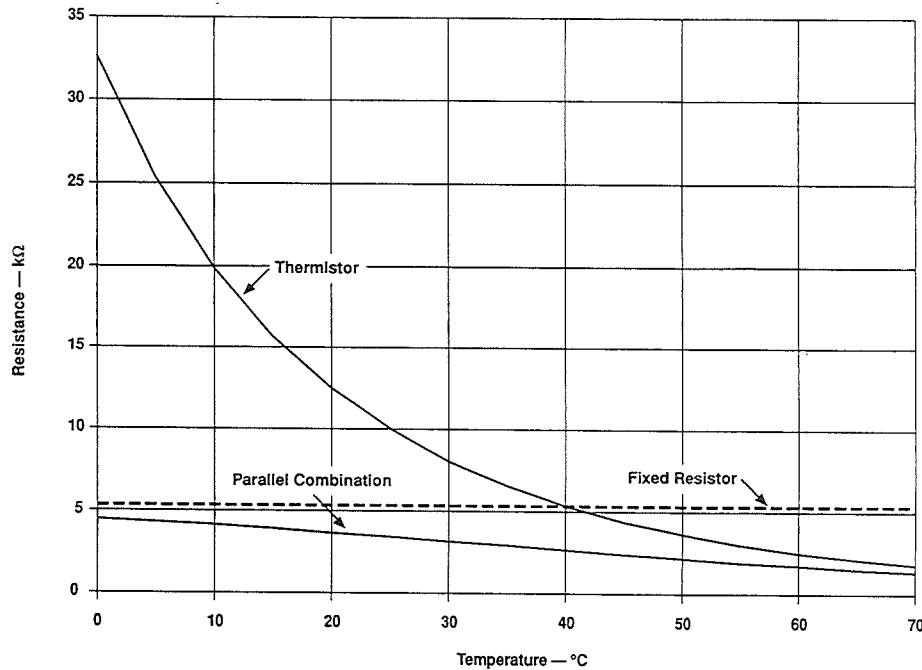


Figure 9.58

The value of the fixed resistor can be calculated from the following equation:

$$R = \frac{RT2 \cdot (RT1 + RT3) - 2 \cdot RT1 \cdot RT3}{RT1 + RT3 - 2 \cdot RT2}$$

where RT1 is the thermistor resistance at T1, the lowest temperature in the measurement range, RT3 is the thermistor resistance at T3, the highest temperature in the range, and RT2 is the thermistor resistance at T2, the midpoint,  $T2 = (T1 + T3)/2$ .

For a typical 10 kΩ NTC thermistor, RT1 = 32,650 Ω at 0°C, RT2 = 6,532 Ω at 35°C, and RT3 = 1,752 Ω at 70°C. This results in a value of 5.17kΩ for R. The accuracy needed in the signal conditioning circuitry depends on the linearity of the network. For the example given above, Figure 9.59 illustrates the response of the network and shows a non-linearity of - 2.3°C/ + 2.0°C.

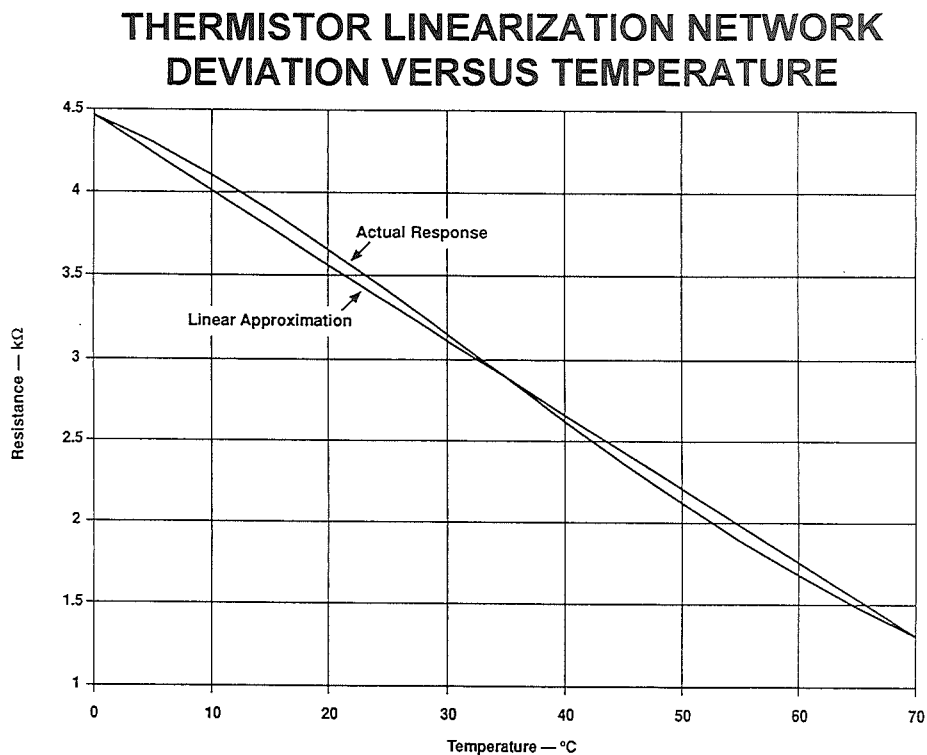
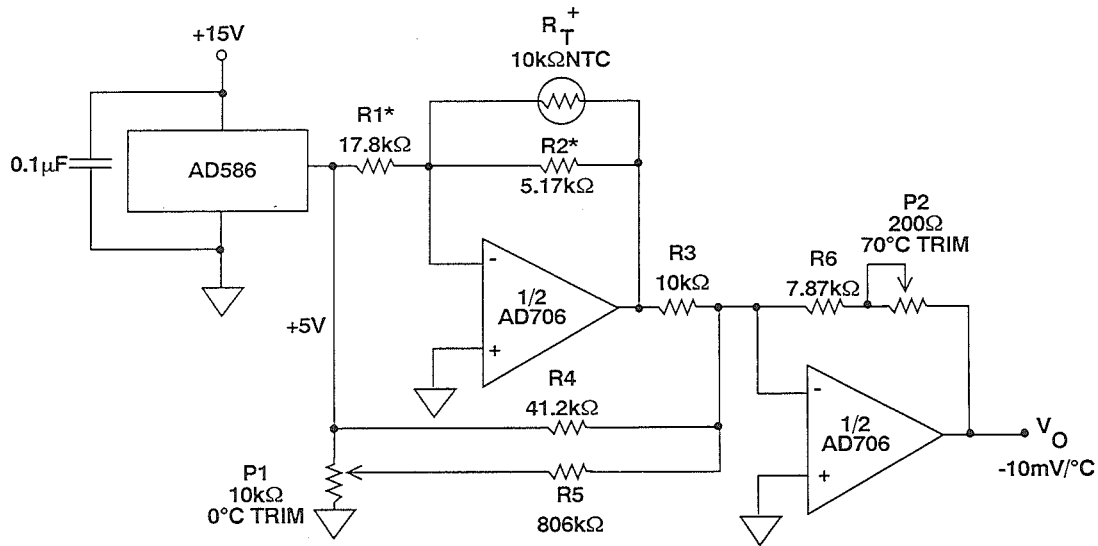


Figure 9.59

Figure 9.60 illustrates a linearized thermistor amplifier designed around the AD706 to measure temperatures over the range of 0°C to 70°C to an accuracy of  $\pm 0.2^\circ\text{C}$  using the network described above. The 10k $\Omega$  thermistor and R2 form the feedback network of an inverting amplifier whose gain increases with temperature. High absolute accuracy in R2 is required to

maintain the linearity of the network to better than  $-2.3^\circ\text{C}/+2^\circ\text{C}$ . Better linearity can be achieved over a narrower measurement temperature range, but R2 should then be recalculated. In many cases, the thermistor is placed some distance from the signal conditioning circuit. In this case, a 0.1 $\mu\text{F}$  capacitor placed across R2 will help to suppress noise.

## LINEARIZED THERMISTOR AMPLIFIER



NOTES: + = ALPHA THERMISTOR 13A1002-C3  
 \* = 0.1% IMPERIAL ASTRONICS M015  
 ALL RESISTORS ARE 1%, 25ppm/°C EXCEPT  
 R5 = 1%, 100ppm/°C

Figure 9.60

R1 and the AD586 provide a constant current of  $281\mu\text{A}$  to the network such that the thermistor's self-heating error is kept below  $0.1^\circ\text{C}$ . Any variation in R1 changes the current through the thermistor network, so absolute accuracy in R1 is important. The second AD706 scales the output of the first amplifier to provide a  $-10\text{mV}/^\circ\text{C}$  output. R4 and the reference generate an offset current such that the output of the second amplifier is 0V at  $0^\circ\text{C}$ .

A calibration procedure is required for this circuit to trim resistor errors and the AD706's  $V_{\text{OS}}$ . A precision decade box temporarily replaces the thermistor. For  $0^\circ\text{C}$  trim, the decade box is set to  $32.650\text{k}\Omega$ , and P1 is adjusted until the

circuit output reads 0V. To trim the circuit at full-scale ( $70^\circ\text{C}$ ), the decade box is set to  $1.752\text{k}\Omega$  and P2 is adjusted until the circuit reads  $-0.70\text{V}$ .

Since the AD706 exhibits very low input bias currents, measurement errors due to them can be neglected in this application. The high open-loop gain and low  $\Delta V_{\text{OS}}$  keep their error contribution below  $0.003^\circ\text{C}$  over a  $25^\circ\text{C}$  change in ambient temperature. To help reduce component costs,  $50\text{ppm}/^\circ\text{C}$  resistors can be substituted for R3, R4, and R6. With this modification, the circuit's accuracy is still better than  $\pm 0.3^\circ\text{C}$  over an ambient temperature range of  $20^\circ\text{C}$  to  $50^\circ\text{C}$ .

## PHOTODIODE TRANSDUCERS

Photodiodes generate a small current which is proportional to the level of illumination. They have many applica-

tions ranging from precision light meters to high-speed fiber optic receivers.

## PHOTODIODE APPLICATIONS

- Optical: Light Meters, Auto-Focus, Flash Controls
- Medical: CAT Scanners (X-Ray Detection), Blood Particle Analyzers
- Automotive: Headlight Dimmers, Twilight Detectors
- Communications: Fiber Optic Receivers
- Industrial: Bar Code Scanners, Position Sensors, Laser Printers

**Figure 9.61**

The equivalent circuit for a photodiode is shown in Figure 9.62. One of the standard methods for specifying the sensitivity of a photodiode is to state its short circuit photocurrent ( $I_{SC}$ ) at a given light level from a well defined light source. The most commonly used source is an incandescent tungsten lamp running at a color temperature of 2850K. At 100 fc (foot-candles) illumination (approximately the light level on an overcast day), the short circuit photocurrent is usually in the picoamps to hundreds of microamps range for small area (less than  $1\text{mm}^2$ ) diodes.

The short circuit photocurrent has a very linear relationship to illumination

over 6 to 9 decades of light intensity, and is therefore often used as a measure of absolute light levels. The open circuit forward voltage across the photodiode varies logarithmically with light level, but because of its large temperature coefficient, the diode voltage is seldom used as an accurate measure of light intensity.

The shunt resistance is of order of  $1000\text{M}\Omega$  at room temperature, and decreases by a factor of 2 for every  $10^\circ\text{C}$  rise in temperature. Diode capacitance is a function of junction area and the diode bias voltage. A value of  $50\text{pF}$  at zero bias is typical for small area diodes.

## PHOTODIODE EQUIVALENT CIRCUIT

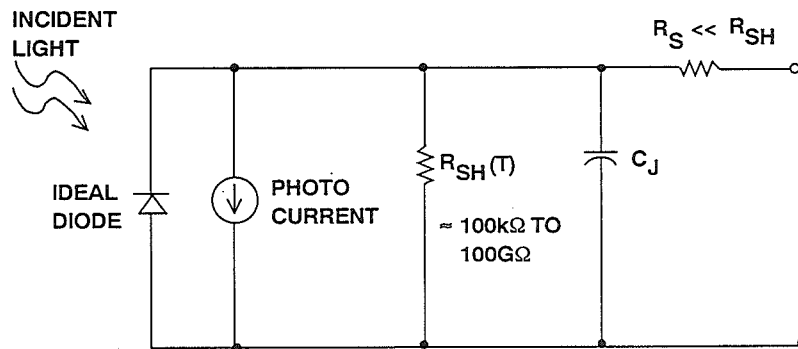
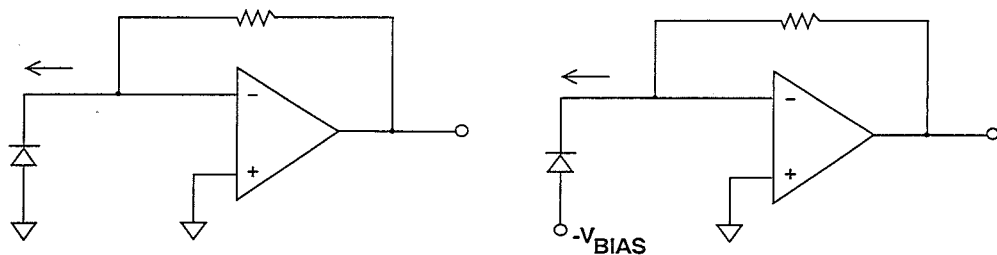


Figure 9.62

## PHOTODIODE MODES OF OPERATION



### PHOTOVOLTAIC

- Zero Bias
- No Dark Current
- Precision Applications
- Low Noise (Johnson)

### PHOTOCONDUCTIVE

- Reverse Bias
- Dark Current Exists
- High Speed Applications
- Higher Noise (Johnson + Shot)

Figure 9.63

Photodiodes may be operated with zero bias (*photovoltaic* mode) or reverse bias (*photoconductive* mode) as shown in Figure 9.63. The most precise linear operation is obtained in the photovoltaic mode, while higher switching speeds are realizable when the diode is operated in the photoconductive mode.

Under reverse bias conditions, a small leakage current called *dark current* will flow even when there is no illumination. There is no dark current in the photovoltaic mode. In the photovoltaic mode,

the diode noise is basically the thermal noise of the shunt resistance. In the photoconductive mode, shot noise is an additional source of noise. Photodiodes are usually optimized during design for use in either the photovoltaic mode or the photoconductive mode, but not both.

Figure 9.64 shows the photosensitivity for a small photodiode (Silicon Detector Part Number SD-020-12-001). The specifications of the diode are summarized in Figure 9.65.

### SHORT CIRCUIT CURRENT VERSUS LIGHT INTENSITY FOR PHOTODIODE (PHOTOVOLTAIC MODE)

ENVIRONMENT	ILLUMINATION ( $f_c$ )	SHORT CIRCUIT CURRENT
Direct Sunlight	1000	30mA
Overcast Day	100	3mA
Twilight	1	0.03mA
Full Moonlit Night	0.1	3000pA
Clear Night / No Moon	0.001	30pA

Figure 9.64

## PHOTODIODE SPECIFICATIONS

### Silicon Detector Part Number SD-020-12-12-001

- Area:  $0.2\text{mm}^2$
- Capacitance: 50pF
- Shunt Resistance at 25°C: 1000 megohms
- Maximum Linear Output Current: 40mA
- Response Time: 12ns
- Photosensitivity:  $0.03\mu\text{A} / \text{fc}$

Figure 9.65

## PHOTODIODE PREAMP CIRCUIT CONSIDERATIONS

A convenient way to convert the photodiode current into a usable voltage is to use an op amp as a current-to-voltage converter as shown in Figure 9.66. The diode bias is maintained at zero volts by the virtual ground of the op amp, and the short circuit current is converted into a voltage. If we wish to operate at maximum sensitivity, we must be able to detect a diode current of 30pA. This implies that the feedback resistor must be very large. For example,  $1000\text{M}\Omega$  will yield a voltage of 30mV for this

current. Larger resistor values are impractical, so we shall use  $1000\text{M}\Omega$  for the most sensitive range. This will give an output voltage range from 10mV for 10pA of diode current to 10V for 10nA, a range of 60dB. For higher values of light intensity, the gain of the circuit must be reduced by using a smaller feedback resistor. With the maximum sensitivity, we should easily be able to distinguish between the light intensity on a clear moonless night (0.001fc) and that of a full moon (0.1fc)!



## SIMPLIFIED OP-AMP CURRENT-TO-VOLTAGE CONVERTER

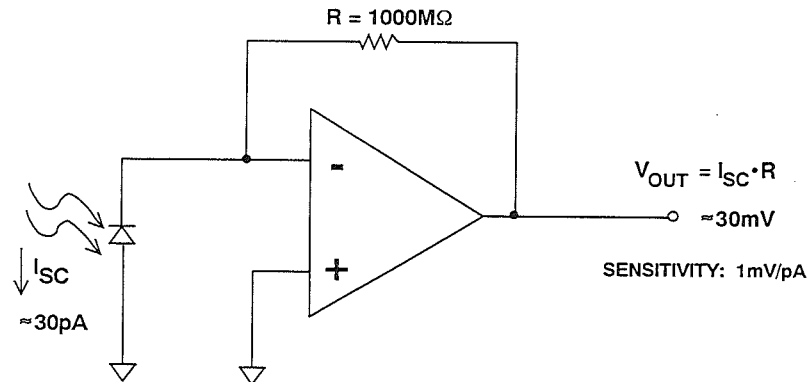


Figure 9.66

Notice that we have chosen to obtain as much gain as possible from one stage, rather than cascading two stages. This is in order to maximize the signal-to-noise ratio (SNR). If we halve the feedback resistor value, the signal level decreases by a factor of 2, while the noise due to the feedback resistor (Noise

Voltage =  $\sqrt{4kTR \cdot \text{Bandwidth}}$ ) decreases by  $\sqrt{2}$ , which reduces the SNR by 3dB, assuming the closed loop bandwidth remains constant. A detailed analysis (Reference 3, Section 3) shows that resistors are one of the largest contributors to the overall output noise.

## PRECAUTIONS FOR PICOAMPERE CIRCUITS

Since the diode current is measured in picoamperes, extreme attention must be given to potential leakage paths in the actual circuit. Two parallel conductor stripes on a high-quality well-cleaned epoxy-glass PC board 0.05 inches apart running parallel for 1 inch have a leakage resistance of approximately  $10^{11}$  ohms at  $+125^{\circ}\text{C}$  (Reference 9, p.293). If there is 15 volts between these runs, there will be a current flow of 150pA.

The critical leakage paths for the photodiode circuit are enclosed by the dotted lines in Figure 9.67. The feedback resistor should be of thin-film on ceramic, or glass with glass insulation. The compensation capacitor across the

feedback resistor should have a polypropylene or polystyrene dielectric. All connections to the summing junction should be kept short. If a cable is used to connect the photodiode to the preamp, it should be kept as short as possible and have Teflon insulation.

Guard rings (on both sides of the PC board) should be used around the inverting input pin of the op amp as shown in Figure 9.68. The case ground of the op amp (usually Pin 8) should also be connected to the grounded guard ring. Maintaining the guard ring at the same potential as the inverting input minimizes leakage current due to PC board resistance.

### LEAKAGE CURRENT PATHS

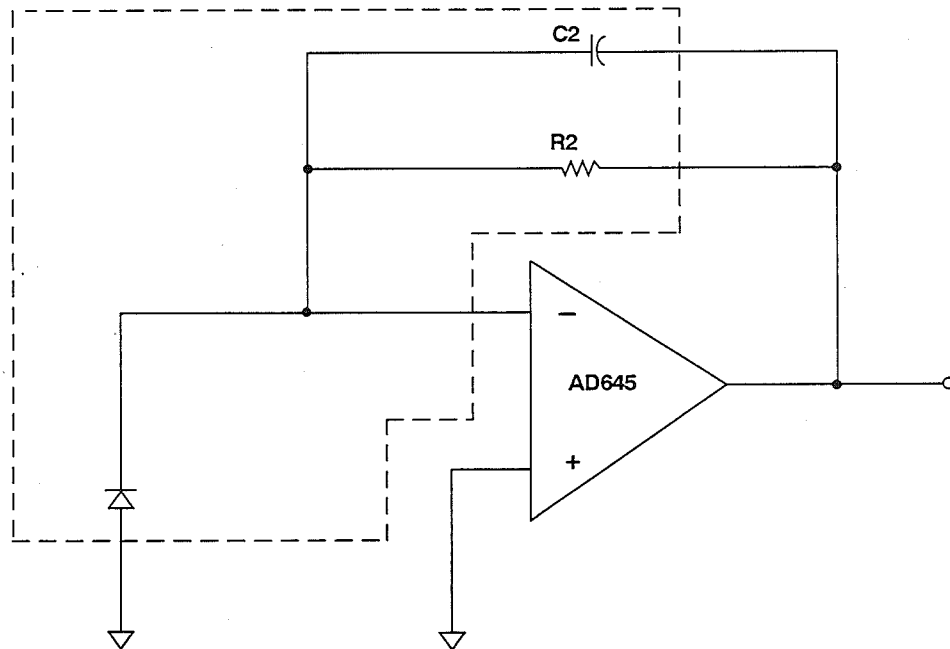


Figure 9.67

## PC BOARD LAYOUT FOR GUARDING TO-99 PACKAGE

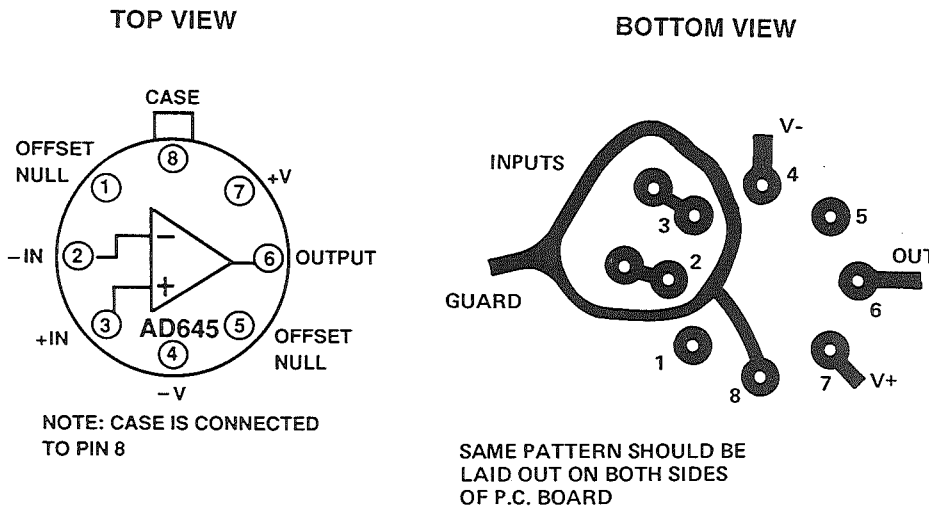


Figure 9.68

Ideally, all connections to the summing input of the op amp should be made to a virgin Teflon standoff insulator ("Virgin" Teflon is a solid piece of new Teflon material which has been machined to shape and has not been welded together from powder or grains). If mechanical and manufacturing considerations allow, the inverting input pin of the op amp should be soldered directly to the Teflon standoff (see Figure 9.69) rather than going through a hole in the PC board. The PC board itself must be

cleaned carefully and then sealed against humidity and dirt using a high quality conformal coating material.

In addition to minimizing leakage currents, the entire circuit should be well shielded with a grounded metal shield to prevent stray signal pickup. Details regarding proper grounding, shielding, and noise reduction techniques are given in References 13 and 14 at the end of this section and in Section 11.

## A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PCB TRACK

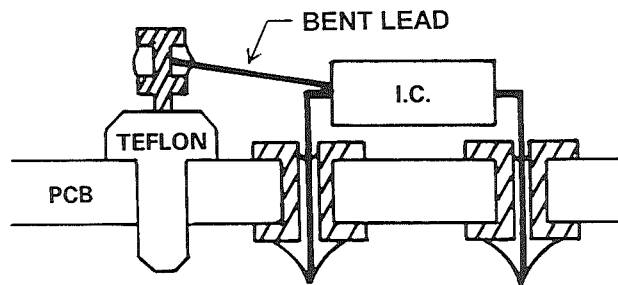


Figure 9.69

### AMPLIFIER SELECTION

If we wish to measure accurately photodiode currents of tens of picoamps, the bias current of the op amp should be no more than a few picoamps. This narrows the choice considerably. The industry-standard OP-07 is an ultra-low  $V_{OS}$  ( $10\mu V$ ) bipolar op amp, but its bias current is  $4nA$  ( $4000pA$ !). Even super-beta bipolar op amps with bias current compensation (such as the OP-97) have bias currents of  $100\mu A$  at room temperature. For this reason, an FET-input electrometer-grade op amp such as the AD549 is required for the photodiode preamp. The bias current of the AD549 is *guaranteed* less than  $60fA$  at  $T_A$  of  $25^\circ C$  (less than one electron every  $3\mu s$ ) but, as with all FET-input op amps, the bias current doubles with every  $10^\circ C$  increase of temperature, so by  $T_A = 125^\circ C$ ,  $I_b$  will be as much as  $60pA$ .

There are many applications for photodiodes which require less sensitivity to illumination but more bandwidth (see Figure 9.70). The equivalent circuit shown in Figure 9.71 is useful in making the proper tradeoffs. The photodiode is operated in the photoconductive mode (reversed biased) in order to minimize the junction capacitance  $C_D$ . Because of the reverse bias, a small amount of *dark current* flows when there is no illumination. The op amp should be chosen for low bias current, high gain-bandwidth product ( $f_u$ ), and low input capacitance  $C_{IN}$ . Notice that the total op amp input capacitance,  $C_1$ , is equal to the diode capacitance  $C_D$  plus the input capacitance of the op amp  $C_{IN}$ . The feedback capacitor  $C_2$  is required in order to compensate for the op-amp input capacitance. It should be as small

as possible (to provide the maximum signal bandwidth) and yet large enough to give adequate phase margin. It is usually optimized in the circuit for best pulse response. The equations are

summarized in Figure 9.72 and are derived in Reference 3, Section 3. Finally, the effects of bias current and noise should be evaluated.

## APPLICATIONS OF WIDE BANDWIDTH PHOTODIODE CIRCUITS

- Ring Laser Gyro Systems
- Bar Code Readers
- Fast Scanners
- Document Scanners
- Fax Machines
- Fiber Optic Receivers

Figure 9.70

## HIGH BANDWIDTH PHOTODIODE PREAMP EQUIVALENT CIRCUIT

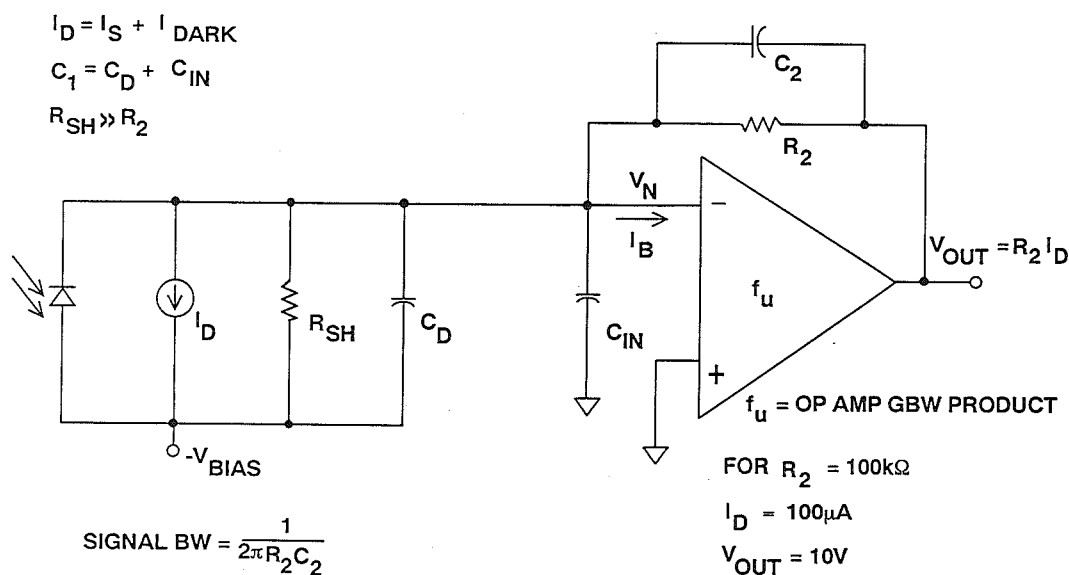


Figure 9.71

**CONDITIONS FOR MAXIMALLY FLAT SIGNAL FREQUENCY  
RESPONSE WITH APPROXIMATELY  
65° PHASE MARGIN AND  
5% STEP FUNCTION OVERSHOOT**

- $C_2 \approx 2 \sqrt{\frac{C_1}{2\pi R_2 f_u}}$ , and
- Signal Bandwidth  $\approx \frac{1}{2} \sqrt{\frac{f_u}{2\pi R_2 C_1}}$ .

Figure 9.72

**GENERALIZED OP AMP SELECTION FLOW CHART  
FOR HIGH SPEED PHOTODIODE PREAMP**

- SIGNAL BW  $\sim \sqrt{\frac{f_u}{R_2 C_1}}$ ,  $f_u$  = Op Amp Unity Gain Bandwidth  
 $C_1$  = Input Capacitance =  $C_d + C_{in}$ .
- Minimize Value of  $R_2$  Based on Gain Requirements
- Try and make op amp input capacitance,  $C_{in} \leq C_d$
- Maximize  $f_u/C_{in}$ , Minimize Voltage and Current Noise
- Calculate  $C_2$  and Signal Bandwidth
- Examine Bias Current and Noise Effects on Circuit

Figure 9.73

Figure 9.74 shows a photodiode preamp circuit with a bandwidth just above 1MHz. The op-amp chosen is the AD843 FET-input type (gain-bandwidth product 34MHz, 6pF input capacitance). Using the circuit parameters  $C_1 = C_D + C_{IN} = 4 + 6 = 10\text{pF}$ ,  $f_u = 34\text{MHz}$ ,  $R_2 = 100\text{k}\Omega$ , we find that  $C_2 = 1.4\text{pF}$  using

the equations in Figure 9.72. In practice,  $C_2$  should be a 2pF low leakage variable capacitor so that the circuit may be optimized for the best compromise between frequency and pulse response. The 100k $\Omega$  resistors are made up of three 33.2k $\Omega$  film resistors in series to minimize stray capacitance.

### 1 MHz PHOTODIODE PREAMP USING AD843 OP AMP

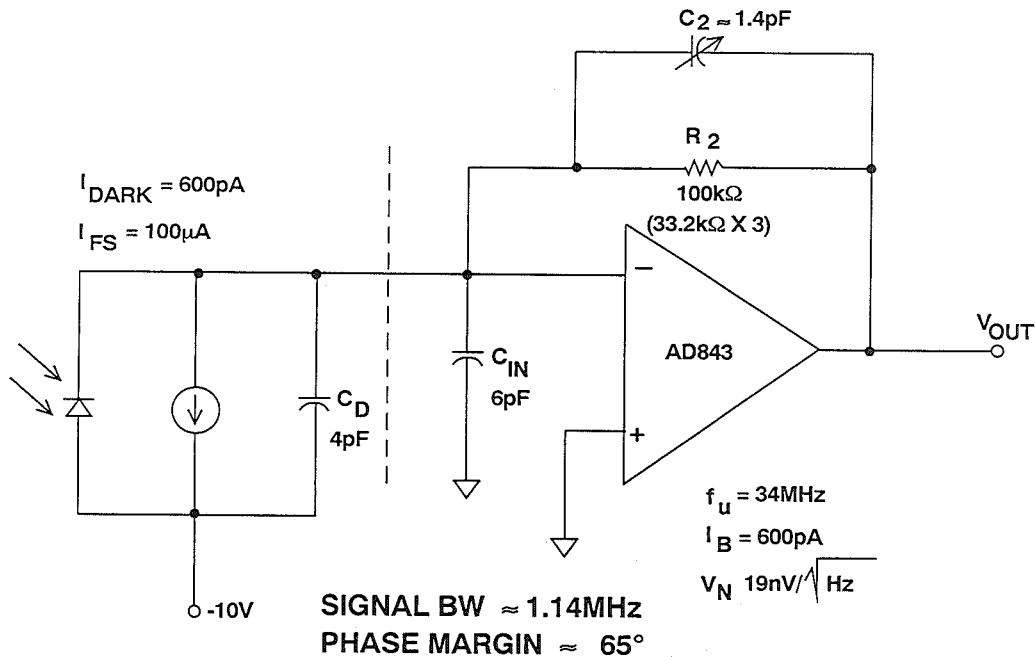


Figure 9.74

The noise analysis of the circuit is somewhat tedious and is given in Reference 2, Section 3. The total output noise of approximately 346 $\mu\text{V}$  rms is domi-

nated by the input voltage noise integrated over the region of high frequency peaking which is typical of second-order circuits.

## HIGH SPEED FIBER OPTIC RECEIVERS

When the primary function of the photodiode preamp is to amplify digital data from a fiber optic link, even more tradeoffs become possible to achieve higher speeds. In a fiber optic data transmission system, such as the one shown in Figure 9.75, the primary purpose of the preamp is to amplify the photodiode current to a voltage level which is sufficient to drive the input of a threshold comparator. In these applications, the data is coded in such a manner that the average duty cycle of the data is always 50% regardless of the actual bit pattern. (A Manchester

coding scheme is one way to accomplish this.) Since the average duty cycle of the data stream is always 50%, ac coupling is possible, and the need for wideband precision op amps is eliminated. The preamp does not have to be a traditional dc-coupled op amp with feedback, and may be a low noise open loop GaAs "gain block". The photodiode, preamp, and the comparator are often fabricated on the same substrate in a hybrid package in order to minimize parasitics. Data transmission rates of much greater than 100MHz are possible using this approach.

## HIGH SPEED FIBER OPTIC DATA RECOVERY

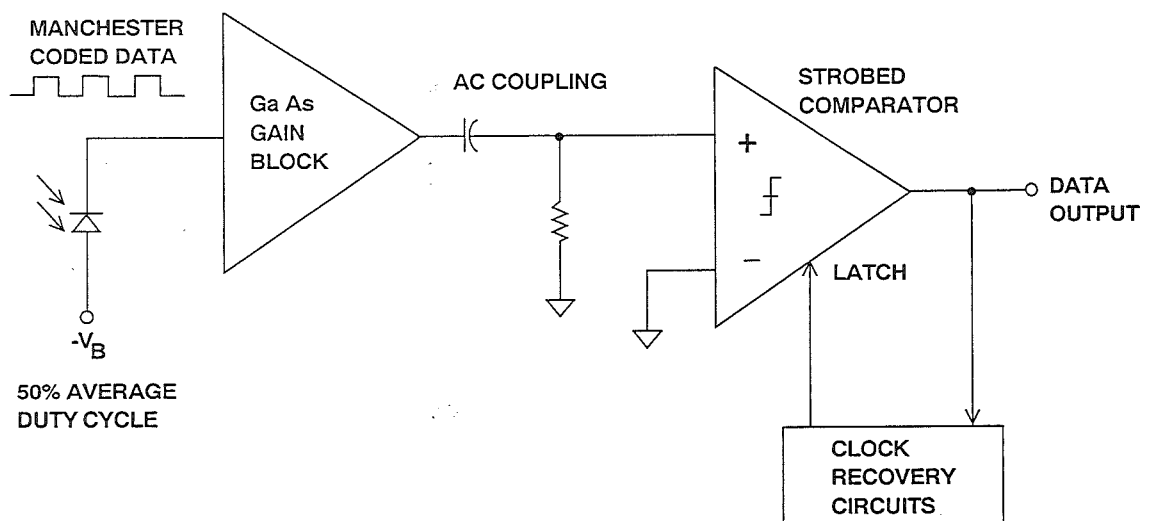


Figure 9.75

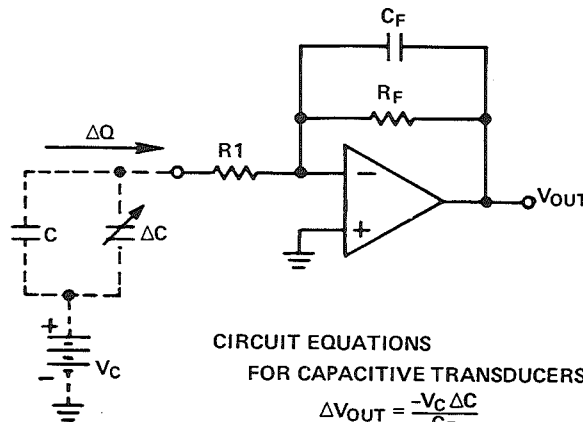


# HIGH-IMPEDANCE CHARGE OUTPUT TRANSDUCERS

High impedance transducers such as hydrophones and some accelerometers require an amplifier which converts a transfer of charge into a change of voltage. Because of the high dc output impedance of these devices, appropriate buffers are required. The basic circuit of an inverting charge sensitive amplifier is shown in Figure 9.76. There are two

types of charge transducers: capacitive and charge-emitting. In a capacitive transducer, the voltage across the capacitor ( $V_c$ ) is held constant. The change in capacitance,  $\Delta C$ , produces a change in charge,  $\Delta Q = \Delta C V_c$ . This charge is transferred to the op amp output as a voltage,  $\Delta V_{out} = -\Delta Q / C_f = -\Delta C V_c / C_f$ .

## CHARGE-SENSITIVE AMPLIFIER



### CIRCUIT EQUATIONS

FOR CAPACITIVE TRANSDUCERS

$$\Delta V_{OUT} = \frac{-V_c \Delta C}{C_f}$$

FOR CHARGE-EMITTING TRANSDUCERS

$$\Delta V_{OUT} = \frac{-\Delta Q}{C_f}$$

LOWER CUTOFF FREQUENCY (-3dB)

$$f_{o1} = \frac{1}{2\pi R_F C_f}$$

UPPER CUTOFF FREQUENCY (-3dB)

$$f_{o2} = \frac{1}{2\pi R_1 C}$$

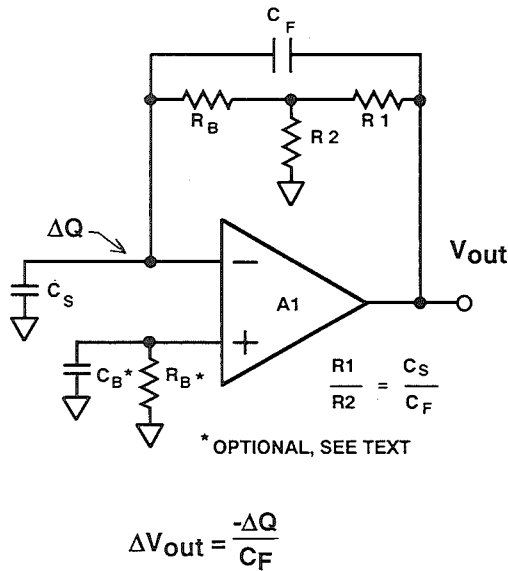
Figure 9.76

Charge-emitting transducers produce an output charge,  $\Delta Q$ , and their output capacitance remains constant. This charge would normally produce an open-circuit output voltage at the transducer output equal to  $\Delta Q / C$ . However, since the voltage across the transducer is held constant by the virtual ground of the op amp ( $R_1$  is usually small), the charge is transferred to capacitor  $C_f$ , producing an output voltage  $\Delta V_{out} = -\Delta Q / C_f$ .

Figure 9.77 shows two ways to buffer and amplify the output of a charge output transducer. Both require using an amplifier which has a very high input impedance, such as the AD745. The AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones.

# CHARGE AMPLIFIER CONFIGURATIONS

## CHARGE OUTPUT MODE



## VOLTAGE OUTPUT MODE

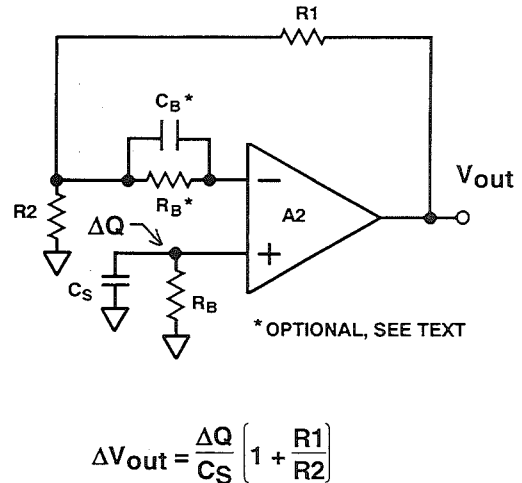


Figure 9.77

The first circuit in Figure 9.77 uses the op amp in the inverting mode. Amplification depends on the principle of conservation of charge at the inverting input of amplifier A1. The charge on capacitor  $C_S$  is transferred to capacitor  $C_F$ , yielding an output voltage of  $\Delta Q/C_F$ . The amplifier's input voltage noise will appear at the output amplified by the ac noise gain of the circuit,  $1 + C_S/C_F$ .

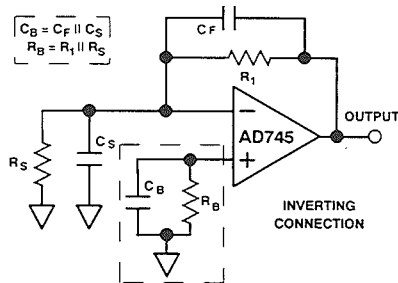
The second circuit shown in Figure 9.77 is simply a high impedance follower with gain. Here the noise gain  $(1 + R1/R2)$  is the same as the gain from the transducer to the output. Resistor  $R_B$ , in both circuits, is required as a dc bias current return.

To maximize dc performance over temperature, the source resistances should be balanced on each input of the amplifier. This is represented by the optional resistor  $R_{B^*}$  shown in Figure 9.77. For best noise performance, the

source capacitance should also be balanced with the capacitor  $C_B$ . In general, it is good practice to balance the source *impedances* (both resistive and reactive) as seen by the inputs of a precision low noise BiFET amplifiers such as the AD743/AD745. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing the input capacitance will minimize ac response errors due to the amplifier's non-linear common mode input capacitance, and, as shown in Figure 9.78, noise performance will be optimized. Figure 9.78 shows the required external components for both inverting and noninverting configurations. For values of  $C_B$  greater than 300pF, there is a diminishing impact on noise, and  $C_B$  can then be simply a large mylar bypass capacitor of 0.01μF or greater.

# BALANCING SOURCE IMPEDANCES MINIMIZES EFFECTS OF BIAS CURRENTS AND REDUCES INPUT NOISE

## CHARGE OUTPUT MODE



## VOLTAGE OUTPUT MODE

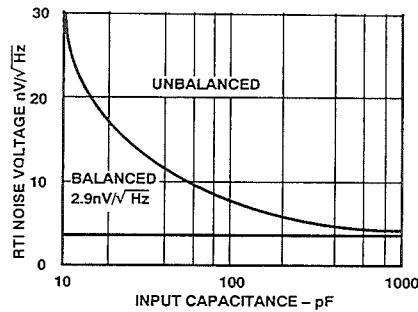
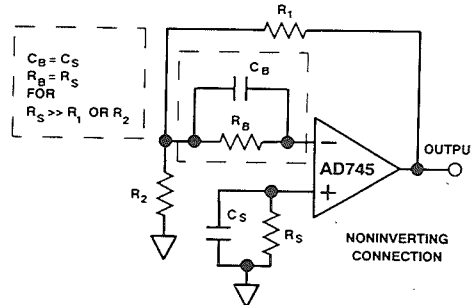
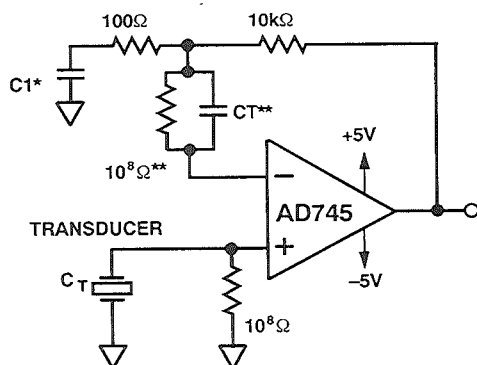


Figure 9.78

Figure 9.79 shows a piezoelectric transducer amplifier connected in the voltage-output mode. Reducing the power supplies to  $\pm 5\text{V}$  reduces the effects of bias current in two ways: first, by lowering the total power dissipation and, second, by reducing the basic gate-to-junction leakage current. The addition of a clip-on heat sink will further limit the internal junction temperature rise.

Without the ac coupling capacitor  $C_1$ , the amplifier will operate over a range of  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ . If the optional ac coupling capacitor  $C_1$  is used, the circuit will operate over the entire  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$  temperature range, but dc information is lost.

## A GAIN OF 100 PIEZOELECTRIC TRANSDUCER AMPLIFIER



\*OPTIONAL DC BLOCKING CAPACITOR

\*\*OPTIONAL, SEE TEXT

- $\pm 5V$  Power Supplies Reduce  $I_b$  for  $0^\circ C$  to  $+85^\circ C$  Operation
- C1 Allows  $-55^\circ C$  to  $+125^\circ C$  Operation

Figure 9.79

## HYDROPHONES

Interfacing the outputs of highly capacitive transducers such as hydrophones, some accelerometers, and condenser microphones to the outside world presents many problems. Previously designers had to use costly hybrid amplifiers consisting of discrete low-noise JFETs in front of conventional op amps to achieve the low levels of voltage and current noise required by these applications. The AD743 and AD745 monolithic amplifiers allow designers to achieve new levels of system integration and performance.

In sonar applications, a piezo-ceramic cylinder is commonly used as the active element in the hydrophone as is shown in Figure 9.80. A typical cylinder has a nominal capacitance of 6,000pF with a series resistance of  $10\Omega$ . The output impedance is typically  $10^8\Omega$  or  $100M\Omega$ .

Since the hydrophone signals are inherently ac in nature, noise is the overriding concern among sonar system designers. The noise floor of the hydrophone and the hydrophone preamplifier together limit the sensitivity of the system and therefore the overall usefulness of the hydrophone. Typical hydrophone bandwidths are in the range 1kHz to 10kHz. The AD743 and AD745 op amps, with their low noise figures of  $2.9nV/\sqrt{Hz}$  and high input impedance of  $10^{10}\Omega$  (or  $10G\Omega$ ) are ideal for use as hydrophone amplifiers.

The AD743 and AD745 are companion amplifiers with different levels of internal compensation. The AD743 is internally compensated for unity gain. The AD745, stable for noise gains of 5 or greater, has a much higher bandwidth and slew rate. This makes the AD745

useful as a high-gain preamplifier where it provides both high gain and wide bandwidth. The AD743 and AD745 have extremely low levels of distortion: less than 0.0003% and 0.0002% (at 1kHz), respectively.

Hydrophone amplifiers are usually connected in the voltage-out mode

rather than charge-out mode. Both modes are illustrated in Figure 9.80. The circuits shown in Figure 9.81 can be used to amplify the output of a typical hydrophone connected in the voltage-out mode.

## HYDROPHONE AMPLIFIERS

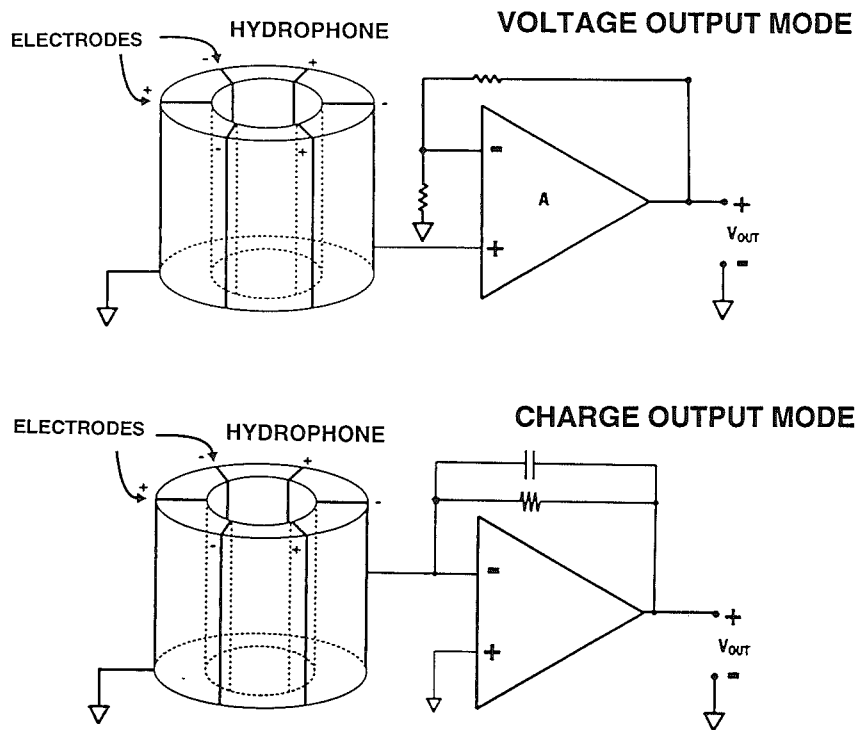


Figure 9.80

## HYDROPHONE AMPLIFIER CONFIGURATIONS

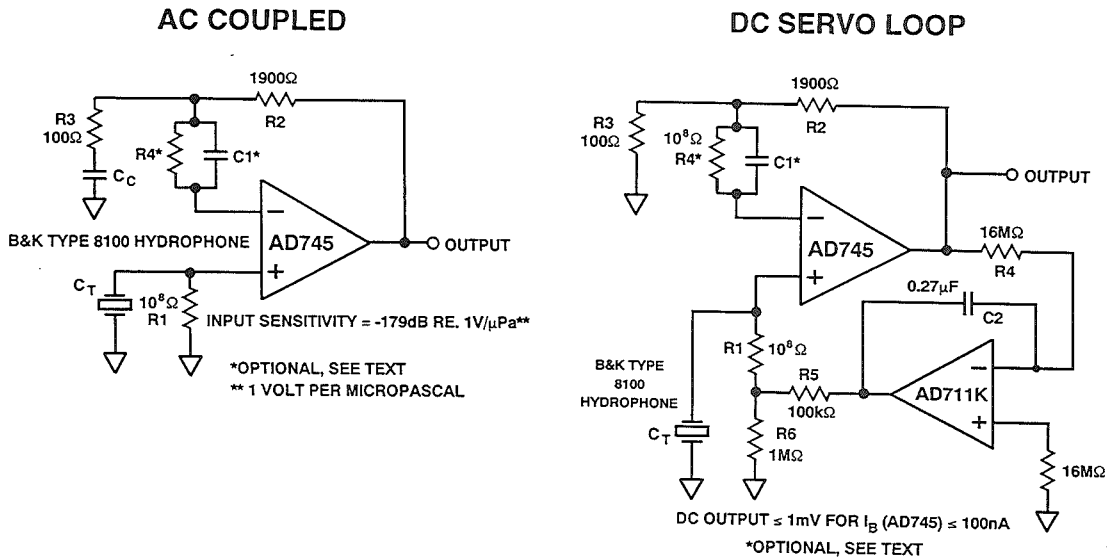


Figure 9.81

If the optional ac coupling capacitor,  $C_c$ , is used, the circuit on the left-hand side of Figure 9.81 will have a low frequency cutoff ( $F_L$ ) :

$$F_L = \frac{1}{2\pi C_c 100\Omega}$$

which is determined by the time constant  $R_3 C_c$ . With the ac coupling capacitor, the gain at dc is 1, and the gain above the low frequency cutoff will be a maximum of  $(1 + R_2/R_3)$  or 26dB.

A second type of hydrophone amplifier circuit is shown in the right-hand diagram in Figure 9.81. It uses a DC servo loop to force the dc output to 0V, within the input offset limits of the AD711 op amp, thereby maintaining full dynamic range. Power supply

voltages should be reduced and heatsinking used to keep the input bias current of the AD745 below 100nA over the full military temperature range. For a smooth low frequency response, the time constant of  $R_4$  and  $C_1$  should be at least 10 times larger than that of  $R_1$  and  $C_T$ .

The transducer shown has a source capacitance of 7500pF. For smaller transducer capacitances ( $\leq 300$ pF), lowest noise can be achieved by adding a parallel RC network ( $R_4 = R_1$ ,  $C_T = C_1$ ) in series with the inverting input of the AD745. As has been previously described, balancing the source impedances (both resistive and reactive) is good practice.

# ACCELEROMETER AMPLIFIERS

Two of the most common charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output measured in picocoulombs (pC) per g, where g is the Earth's gravitational constant (9.81m/s<sup>2</sup>). Figure 9.82 shows two ways to configure the AD745 as a low noise

charge amplifier for use with piezoelectric accelerometers. The output voltage,  $\Delta V_{out}$ , of these circuits will be determined by the value of capacitor, C1, and the transducer charge output,  $\Delta Q$ , or

$$\Delta V_{out} = \frac{\Delta Q}{C1}$$

## HIGH PERFORMANCE ACCELEROMETER AMPLIFIERS

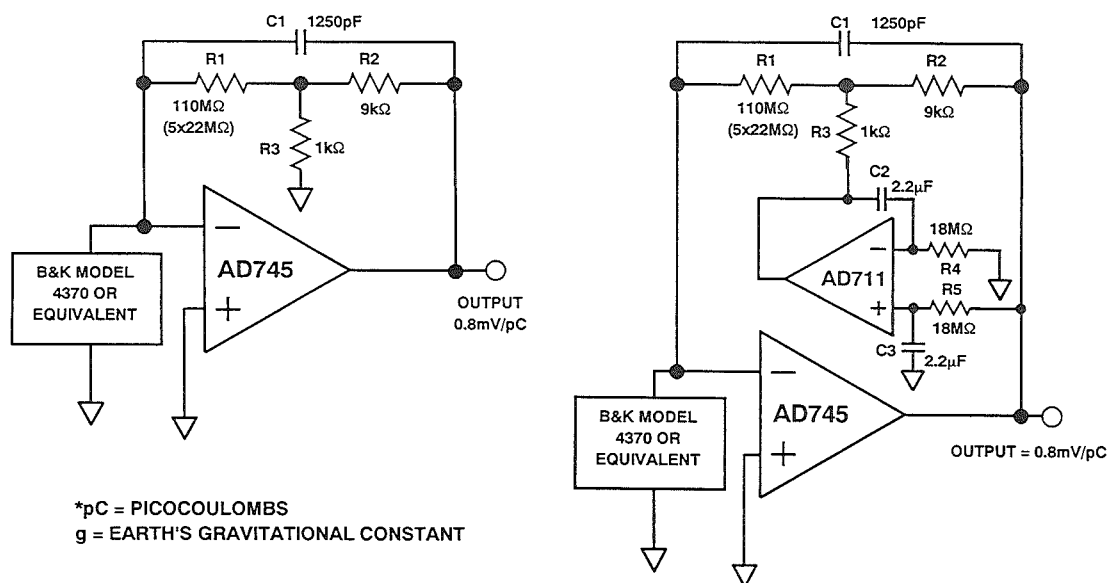


Figure 9.82

The ratio of capacitor C1 to the internal capacitance  $C_T$  of the transducer determines the ac noise gain of the circuit,  $1 + C_T/C1$ . The amplifier's voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a "T" network is used, the effective value is  $R1(1+R2/R3)$ .

The addition of the dc servo loop shown in Figure 9.82 can be used to assure a dc output less than 10mV without the need for a large compensating resistor when dealing with bias currents as large as 100nA. For low frequency performance, the time constant of the servo loop ( $R4C2 = R5C3$ ) should be:

$$\text{Time Constant} = R4C2 = R5C3 \geq 10R1 \left( 1 + \frac{R2}{R3} \right) C1$$

## MONOLITHIC ACCELEROMETERS

The ADXL50 is a complete acceleration measurement system on a single monolithic IC. It contains a polysilicon surface-micro-machined sensor and signal conditioning circuitry. The ADXL50 is capable of measuring both positive and negative acceleration to a maximum level of  $\pm 50g$ .

Figure 9.83 is a simplified view of the acceleration sensor at rest. The differential capacitor sensor consists of independent fixed plates and a movable "floating" central plate which deflects in response to acceleration. The two capacitors are connected in series, forming a capacitive divider with a common movable central plate. A force balance

technique counters any deflection due to acceleration and servos the sensor back to its 0g position.

Figure 9.84 shows the sensor responding to acceleration. When this occurs, the common central plate or "beam" moves closer to one of the fixed plates while moving further from the other. The sensor's fixed capacitor plates are driven differentially by a 1MHz square wave: the two square wave amplitudes are equal but are  $180^\circ$  out of phase. When at rest, the values of the two capacitors are the same, and therefore the voltage output at their electrical center (i.e., at the center plate) is zero.

### SIMPLIFIED DIAGRAM OF THE ADXL50 SENSOR AT REST

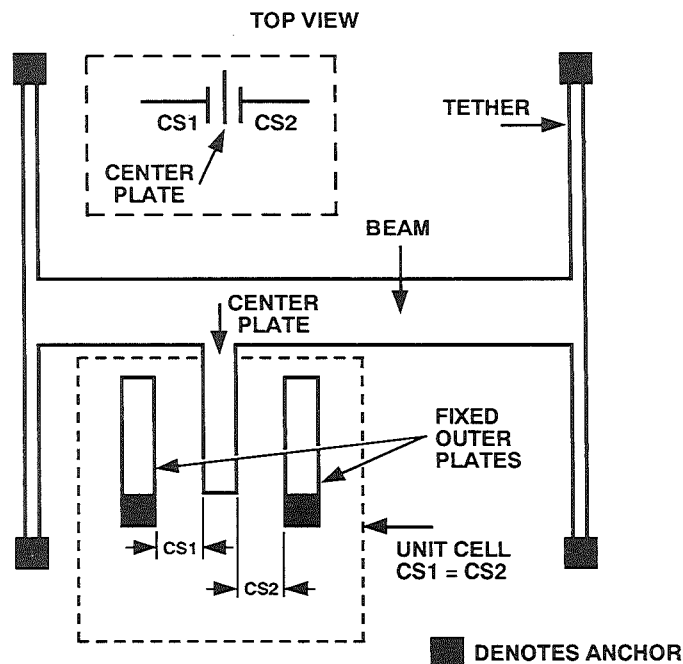


Figure 9.83



## THE ADXL50 SENSOR MOMENTARILY RESPONDING TO AN EXTERNALLY APPLIED ACCELERATION

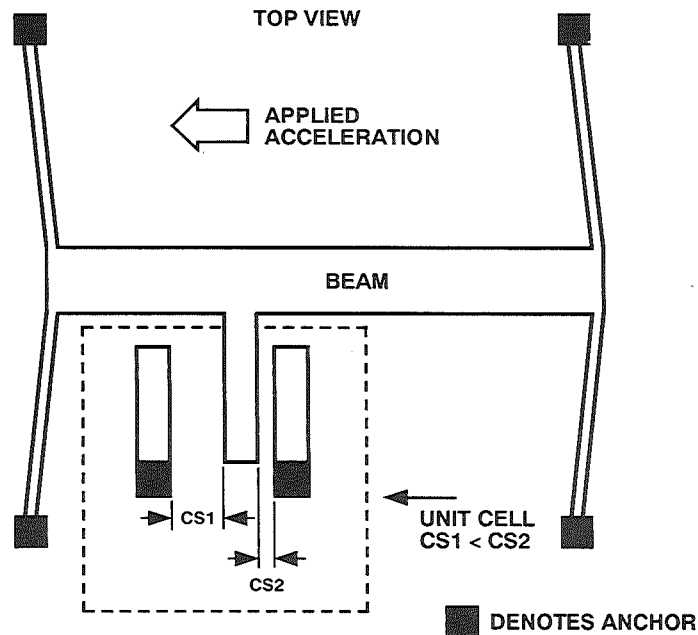


Figure 9.84

When the sensor begins to move, a mismatch in the capacitance produces an output signal at the central plate. The output amplitude will increase with the acceleration experienced by the sensor. The direction of beam motion affects the phase of the signal - synchronous demodulation is used to extract this information.

Figure 9.85 shows a simplified block diagram of the ADXL50. The voltage output from the central plate of the sensor is buffered and then applied to a

synchronous demodulator which is also supplied with a 1MHz clock from the same oscillator which drives the fixed plates of the sensor. The demodulator will rectify any voltage which is synchronous with its clock signal. If the applied voltage is in sync and in phase with the clock, a positive output will result. If the applied voltage is in sync but 180° out of phase with the clock, then the demodulator's output will be negative. All other signals will be rejected. The bandwidth of the demodulator is set by an external capacitor C1.

## ADXL50 ACCELEROMETER BLOCK DIAGRAM

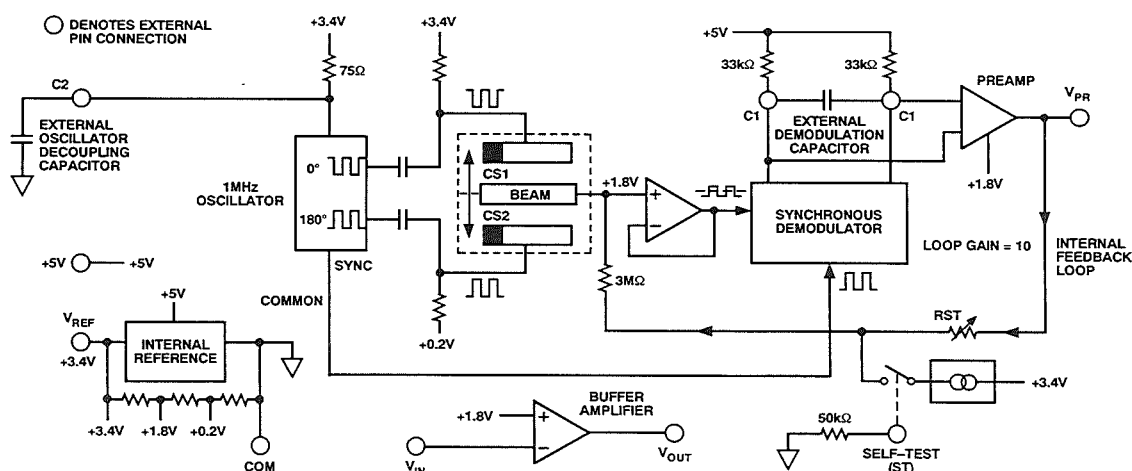


Figure 9.85

The output of the synchronous demodulator drives the preamp - an instrumentation amplifier which is referenced to +1.8V. The output of the preamp is fed back to the sensor through a 3MΩ isolation resistor and creates an electrostatic force which holds the sensor's center plate in the center position. The correction voltage is a direct measure of the applied acceleration and appears at the V<sub>PR</sub> pin.

The loop bandwidth corresponds to the time required to apply feedback to the sensor and is set by external capacitor C1. The loop response is fast enough to follow changes in acceleration up to and exceeding 1kHz. The ADXL50's ability to maintain a flat response over this

bandwidth keeps the sensor virtually motionless. This eliminates any nonlinearity or aging effects in the sensor beam's mechanical support spring, which is a problem with open-loop sensors.

The output of the preamp is 1.8V at zero acceleration with an output range of  $\pm 0.95V$  for a  $\pm 50g$  input, i.e., 19mV/g. An uncommitted buffer amplifier has been included on-chip to enhance the user's ability to offset the zero signal level and to amplify and filter the signal. The sensitivity may be increased up to  $\pm 10g$  (200mV/g) by using the internal buffer amplifier with the proper external gain-setting resistors.

# CHARGE COUPLED DEVICES (CCDs)

Charge coupled devices (CCDs) contains a large number of small photocells called photosites or pixels which are arranged either in a single row (linear arrays) or in a matrix (area arrays). CCD area arrays are commonly used in video applications, while linear arrays are used in facsimile machines, graphics scanners, and pattern recognition equipment.

The linear CCD array consists of a row of image sensor elements (photosites, or pixels) which are illuminated by light from the object or document. During one exposure period each photosite acquires an amount of charge which is

proportional to its illumination. These photosite charge packets are subsequently switched simultaneously via transfer gates to an analog shift register. The charge packets on this shift register are clocked serially to a charge detector (storage capacitor) and buffer amplifier (source follower) which convert them into a string of photo-dependent output voltage levels (see Figure 9.86). While the charge packets from one exposure are being clocked out to the charge detector, another exposure is underway. The analog shift register typically operates at frequencies between 1 and 10MHz.

## LINEAR CCD ARRAY

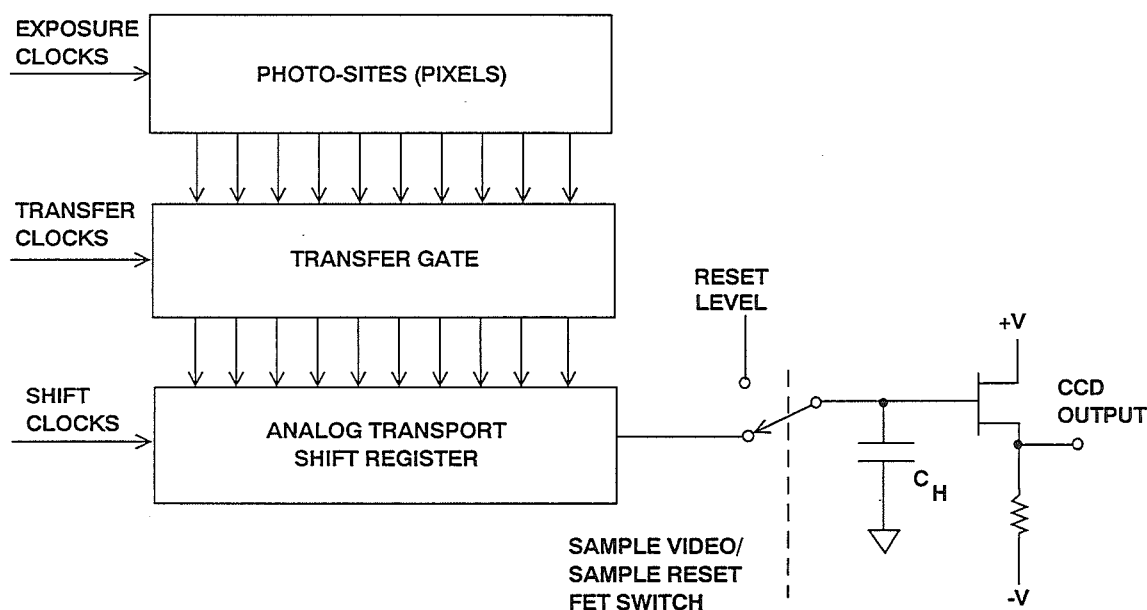


Figure 9.86

The charge detector readout cycle begins with a reset pulse which causes a FET switch to set the output storage capacitor to a known voltage. The switching FET's capacitive feedthrough causes a reset glitch at the output as shown in Figure 9.87. The switch is then opened, isolating the capacitor, and the charge from the last pixel is dumped onto the capacitor causing a

voltage change. The difference between the reset voltage and the final voltage (video level) shown in Figure 9.87 represents the amount of charge in the pixel. CCD charges may be as low as 10 electrons, and a typical CCD output sensitivity is  $0.6\mu\text{V}/\text{electron}$ . Most CCDs have a saturation output voltage of about 1V (see Reference 16).

### CCD OUTPUT WAVEFORM

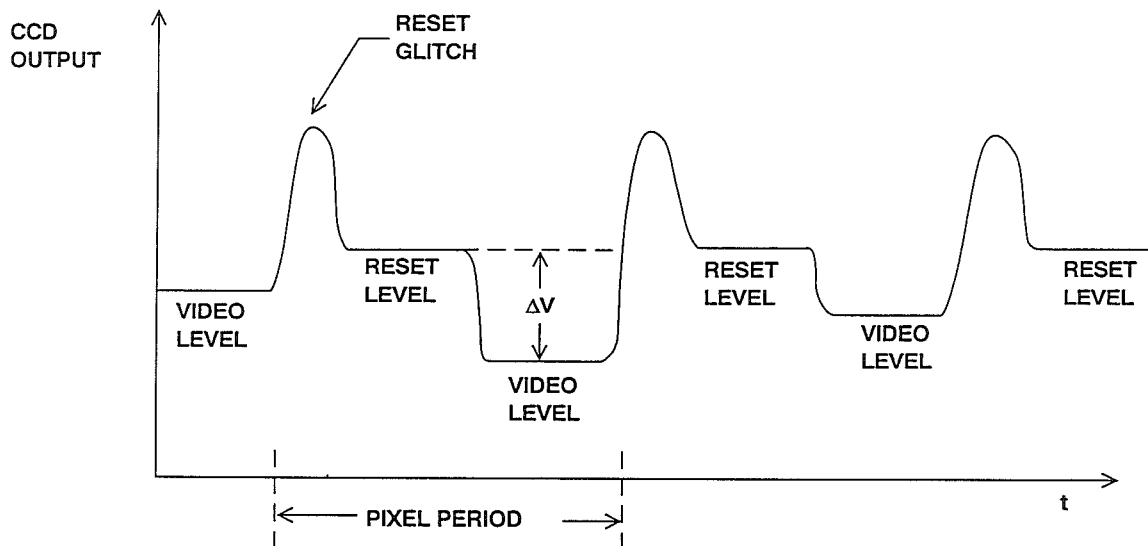


Figure 9.87

Since CCDs are generally fabricated on MOS processes, they have limited capability to perform on-chip signal conditioning. Therefore the CCD output is generally processed by external conditioning circuits.

CCD output voltages are small and quite often buried in noise. The largest source of noise is the thermal noise in

the resistance of the FET reset switch. This noise may have a typical value of 100 to 300 electrons rms (approximately 60 to 180mV rms). This noise occurs as a *sample-to-sample* variation in the CCD output level and is common to both the reset level and the video level for a given pixel period. A technique called *correlated double sampling* (CDS) is often used to reduce the effect

of this noise. Figure 9.88 shows two circuit implementations of the CDS scheme. In the top circuit, the CCD output drives both SHAs. At the end of the reset interval, SHA1 holds the reset voltage level. At the end of the video interval, SHA2 holds the video level. The SHA outputs are applied to a difference amplifier which subtracts one from the other. In this scheme, there is only a short interval during which both SHA outputs are stable, and their difference represents  $\Delta V$ , so the difference amplifier must settle quickly.

Another arrangement is shown in the bottom half of Figure 9.88, which uses

three SHAs and allows either for faster operation or more time for the difference amplifier to settle. In this circuit, SHA1 holds the reset level so that it occurs simultaneously with the video level at the input to SHA2 and SHA3. When the video clock is applied simultaneously to SHA2 and SHA3, the input to SHA2 is the reset level, and the input to SHA3 the video level. This arrangement allows the entire pixel period (less the acquisition time of SHA2 and SHA3) for the difference amplifier to settle.

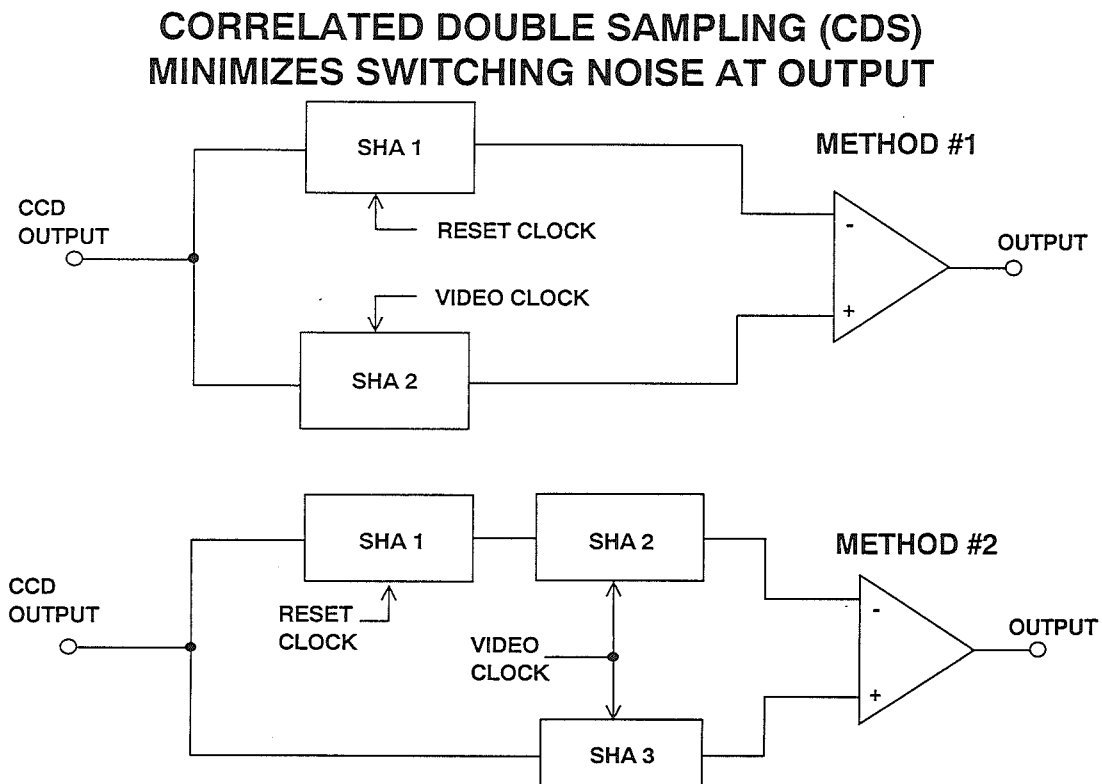


Figure 9.88

## HALL EFFECT MAGNETIC SENSORS

If a current flows in a conductor (or semiconductor) and there is present a magnetic field perpendicular to the current flow, then the combination of current and magnetic field will generate a voltage perpendicular to both. This

phenomenon is called the *Hall Effect*, and the voltage,  $V_H$ , is known as the *Hall Voltage*.  $V_H$  is a function of the current density, the magnetic field, and the charge density and carrier mobility of the conductor.

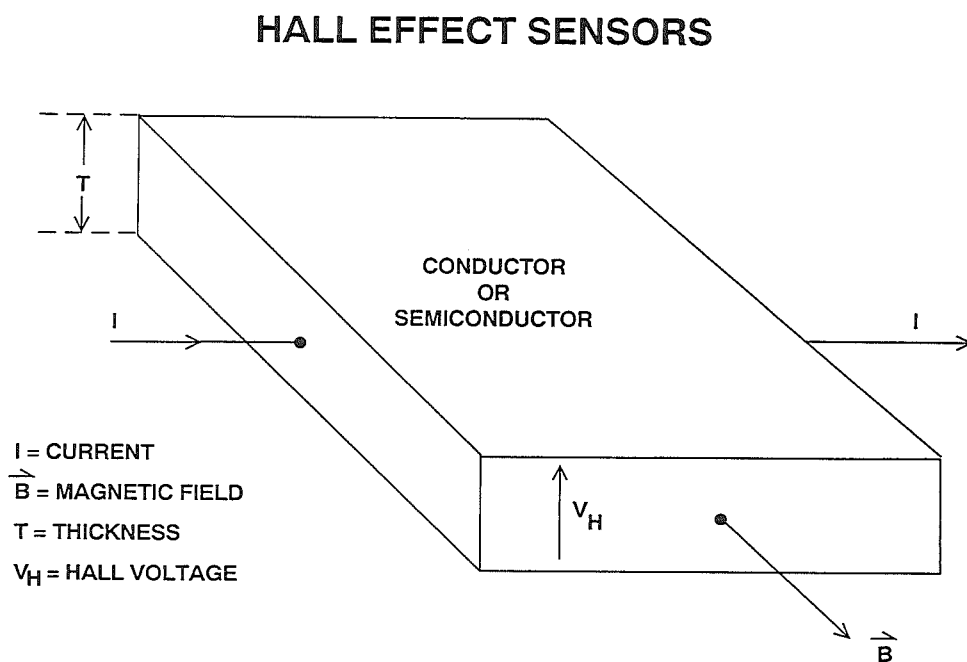


Figure 9.89

The Hall effect may be used to measure magnetic fields (and hence in contact-free current measurement), but its commonest application is in motion sensors where a fixed Hall sensor and a small magnet attached to a moving part can replace a cam and contacts with a great improvement in reliability. (Cams wear and contacts arc or become fouled, but magnets and Hall sensors are contact free and do neither.) Since  $V_H$  is proportional to magnetic field and not to rate of change of magnetic field like an inductive sensor, the Hall Effect provides a more reliable low speed sensor than an inductive pickup.

Although several materials can be used for Hall effect sensors, silicon has the

advantage that signal-conditioning circuits can be integrated on the same chip. The AD22150 integrates a Hall effect sensor with a gain stage and a comparator as shown in Figure 9.90. The part is designed to detect rotation speed in automotive applications. The AD22150 responds to small changes in field (operate and release points at  $-12$  and  $+17$  Gauss, respectively). The comparator has built-in hysteresis, and the device operates up to 50kHz. A typical application is shown in Figure 9.91. The changing magnetic field caused by the rotating target wheel and the biasing magnet produces a square wave output from the AD22150.

### AD22150 MONOLITHIC HALL EFFECT SENSOR WITH SIGNAL CONDITIONING

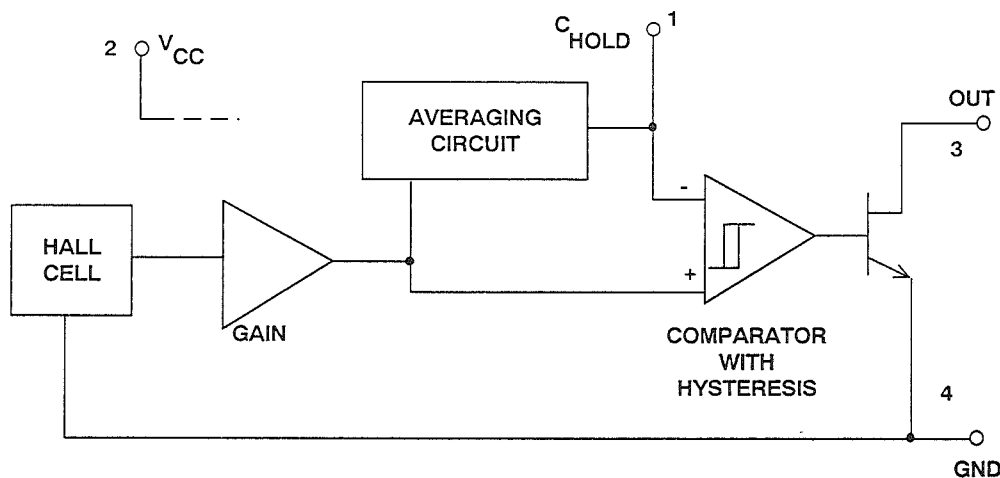


Figure 9.90

## TYPICAL APPLICATION OF A HALL EFFECT SENSOR

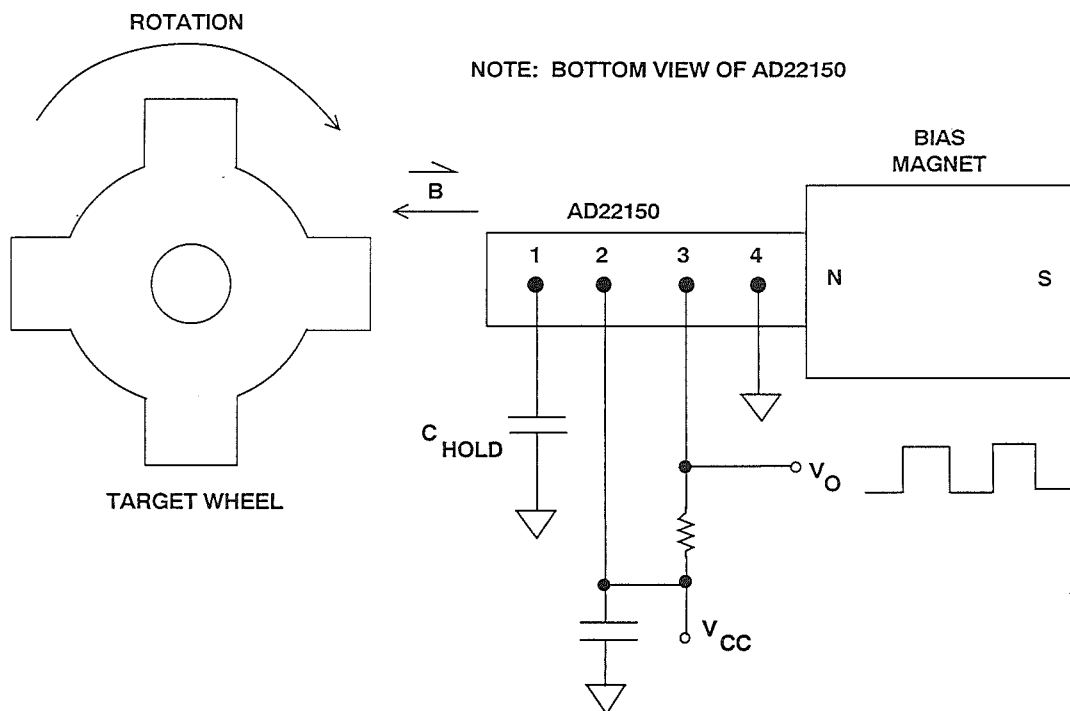


Figure 9.91



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## SECTION 10

### PASSIVE AND ACTIVE ANALOG FILTERING

- Introduction to Filter Design and Implementation
- Antialiasing Filter Design Example
- A Programmable State Variable Filter
- A Seven-Pole FDNR 20kHz Antialiasing Filter
- A 2MHz Biquad Bandpass Filter Using a 30MHz Quad Op Amp
- Practical Problems in Filter Implementation:  
Passive Components, Active Components
- A 12MHz Sallen-Key Filter using a Current Feedback Amplifier
- Switched Capacitor Filters



## SECTION 10

# PASSIVE AND ACTIVE ANALOG FILTERING

*Hank Zumbahlen, Walt Kester*

## INTRODUCTION TO FILTER DESIGN AND IMPLEMENTATION

Filtering is an important part of analog signal processing. Filtering can be used to reduce unwanted signals, limit bandwidth, help recover wanted signals, minimize aliasing in sampled data systems, and smooth the output of DACs. There are five classes of filters. *Lowpass* filters pass all frequencies below the cutoff frequency and block all frequencies above the cutoff frequency. *Highpass* filters are the inverse of the lowpass filters. They block the low

frequencies and pass those above the cutoff frequency. *Bandpass* filters pass those frequencies between the lower cutoff and upper cutoff frequencies and reject all others. *Bandstop* filters are the inverse of bandpass filters. They reject frequencies between the cutoff frequencies and pass all others. *Allpass* filters pass all frequencies equally but introduce a predictable phase delay to the signal.

## CLASSES OF PASSIVE AND ACTIVE FILTERS

- Lowpass
- Highpass
- Bandpass
- Bandstop
- Allpass

Traditional filters were passive, that is designed with no active elements. Active components were too costly and had very poor performance. Inductors, capacitors, and resistors were used to synthesize the filter. This approach has several limitations because inductors become physically large for low frequency filters and have poor characteristics at high frequencies. There is a

great deal of interaction between the different sections of the filter. Impedance levels must be precisely controlled. Close component tolerances are difficult to manufacture and maintain. Despite these limitations passive filters are still dominant at high frequencies, primarily due to dynamic performance limitations of op amps.

## **PASSIVE FILTERS**

- **Designed with Inductors, Capacitors, Resistors**
- **Large Inductors Required for Low Frequency Filters**
- **Interaction Between Filter Stages**
- **Component Tolerances Difficult to Manufacture and Maintain**
- **Still the Only Solution at High Frequencies Due to Active Component Limitations**

**Figure 10.2**

Active filters answer some of the limitations of the passive filter by offering isolation between stages and eliminating the need for inductors. Their use at

high frequencies is limited by the dynamic performance of the active elements.

## ACTIVE FILTERS

- Eliminate Need for Inductors
- Good Interstage Isolation
- High Frequency Use Limited by Op Amp Dynamic Performance

Figure 10.3

A filter can be specified in terms of five parameters as shown in Figure 10.4. The *cutoff frequency*  $F_c$  is the frequency at which the filter response leaves the error band (or the -3dB point for a Butterworth filter). The *stopband frequency*  $F_s$  is the frequency at which the minimum attenuation in the

stopband is reached. The *passband ripple*  $A_{\max}$  is the variation (error band) in the passband response. The *minimum passband attenuation*  $A_{\min}$  defines the signal attenuation within the stopband. The *order*  $M$  of the filter is the number of poles in the transfer function.

## KEY FILTER DESIGN PARAMETERS

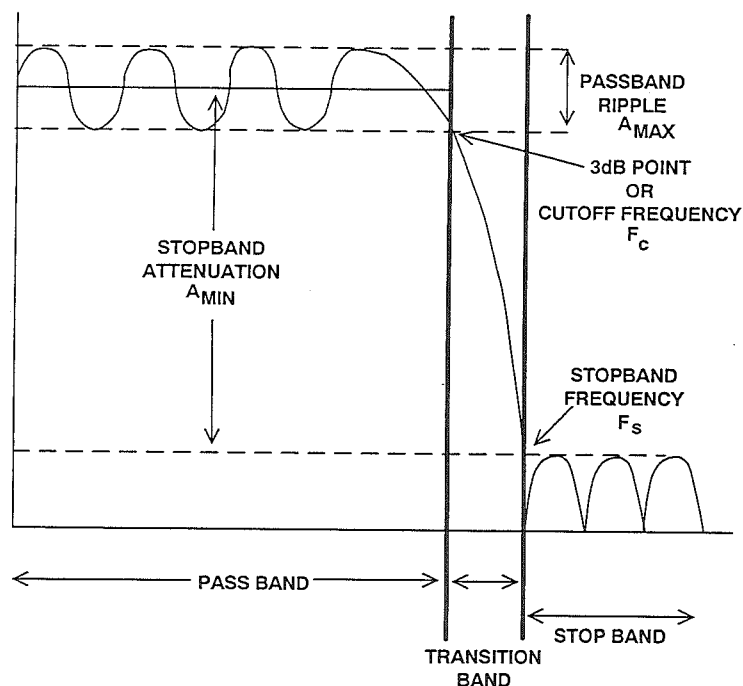


Figure 10.4

## FILTER SPECIFICATIONS

- Cutoff Frequency,  $F_c$
- Stopband Frequency,  $F_s$
- Passband Ripple,  $A_{max}$
- Stopband Attenuation,  $A_{min}$
- Filter Order,  $M$

Figure 10.5

Typically, one or more of the above parameters will be variable. For instance, if you were to design an antialiasing filter for an ADC, you will know the cutoff frequency, the stopband frequency, and the minimum attenuation. You can then go to a chart or computer program to determine the other parameters.

There are many transfer functions that may satisfy the requirements of a particular filter. The *Butterworth* filter is the best compromise between attenuation and phase response. It has no ripples in the passband or the stopband and is called the *maximally flat filter* because of this. The Butterworth filter achieves its flatness at the expense of a relatively wide transition region from passband to stopband.

The *Chebyshev* filter has a smaller transition region than the same-order Butterworth filter, but it has ripples in

either its passband or stopband. This filter gets its name because the Chebyshev filter minimizes the height of the maximum ripple—this is the Chebyshev criterion.

The Butterworth filter and the Chebyshev filter are all-pole designs. By this we mean that the zeros of the transfer function are at one of the two extremes of the frequency range (0 or  $\infty$ ). For a lowpass filter, the zeros are at  $f = \infty$ . We can add finite frequency transfer function zeros as well as poles to get an *Elliptical Filter*. This filter has a shorter transition region than the Chebyshev filter because it allows ripple in both the stopband and passband. The Elliptical filter also has degraded phase (time domain) response.

These are by no means all possible transfer functions, but they do represent the most common.

## POPULAR FILTER DESIGNS

- **Butterworth:** All Pole, No Ripples in Passband or Stopband, Maximally Flat Response
- **Chebyshev:** All Pole, Ripple in Passband, Shorter Transition Region than Butterworth for Given Number of Poles
- **Elliptical:** Ripple in Both Passband and Stopband, Shorter Transition Region than Chebyshev, Degraded Phase Response, Poles and Zeros

Figure 10.6



Once the order of the filter and the specifications of filter have been determined, the design charts (see Reference 1) or computer programs are consulted, and the linear and quadratic factors of poles for the transfer function are determined. All filters, regardless of order, are made up of one- or two-pole sections. The single pole section is defined by its cutoff frequency, which is the -3dB point. The pole pair in a two-pole filter section is defined by its resonant frequency ( $F_0$ ) and  $Q$ , which indicates the peaking of the section. Sometimes alpha ( $\alpha$ ) is used instead of  $Q$  ( $Q=1/\alpha$ ).

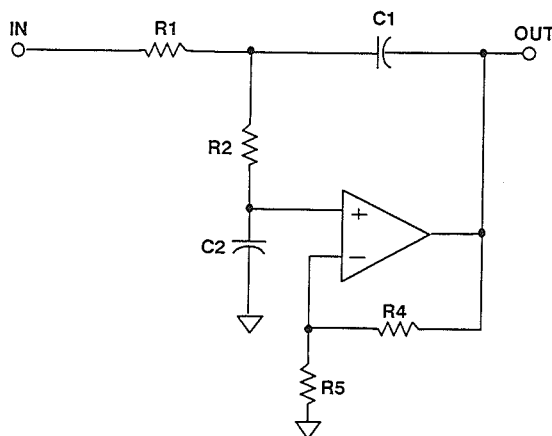
When the values of  $F_0$  and  $Q$  are defined, the configuration for the realization of the filter is then chosen: Butterworth, Chebyshev, or Elliptical.

For passive filters, these values, along with the filter characteristic impedance, determine the inductor, capacitor, and resistor values.

For active filters, it is necessary to decide which of the realizations to use. The three most common are the *Sallen-Key* (voltage controlled voltage source), *multiple feedback*, and *state variable*. Each realization has its own advantages and disadvantages.

The Sallen-Key configuration shown in Figure 10.7 is the least dependent on the performance of the op amp, and the signal phase is maintained. For this filter, the ratio of the largest resistor value to the smallest resistor value and the ratio of the largest capacitor value to the smallest capacitor value is low. The frequency term and  $Q$  terms are somewhat independent, but they are very sensitive to the gain parameter. The Sallen-Key is very  $Q$ -sensitive to element values for high  $Q$  sections. The design equations are given in Figure 10.7.

## VOLTAGE CONTROLLED VOLTAGE SOURCE (SALLEN-KEY) REALIZATION



$H$  = Circuit Gain Below Cutoff

$\alpha$  = Damping Ratio =  $1/Q$

$F_0$  = Cutoff Frequency

Choose  $C1$

$$K = 2\pi F_0 C1$$

$$M = \frac{\alpha^2}{4} + H - 1$$

$$C2 = M C1$$

$$R1 = \frac{2}{K\alpha}$$

$$R2 = \frac{\alpha}{2MK}$$

Choose  $R5$

$$R4 = R5(H - 1)$$

For  $H = 1$ ,  $R4 = 0$ ,  $R5 = \text{Open}$

Figure 10.7

The multiple feedback filter shown in Figure 10.8 uses an op amp in the inverting configuration. The dependence on the op amp parameters is greater than in the Sallen-Key realization. It is hard to generate high  $Q$  sections due to the limitations of the open loop gain of the op amp. The maximum to minimum component value ratios are higher than in the Sallen-Key realization. The design equations are also given in Figure 10.8.

The state-variable realization shown in Figure 10.9 offers the most precise implementation, at the expense of many more circuit elements. All parameters can be adjusted independently, and lowpass, highpass, and bandpass outputs are available simultaneously. The gain of the filter is also independently variable. Since all parameters of the state variable filter can be adjusted independently, component spread is minimized. Also, variations due to temperature and component tolerances are minimized. The design equations for the state variable filter are given in Figure 10.9.

Another active filter technique that has recently become more popular is the *Frequency Dependent Negative Resistor* (FDNR), which is a subset of the *General Impedance Converter* (GIC). In the FDNR the passive realization goes through a transformation by  $1/s$ . Therefore, inductors, whose impedance is  $sL$ , transform into a resistor of value  $L$ . Similarly, a resistor of value  $R$  becomes a capacitor of value  $R/s$ . A capacitor of impedance  $1/sC$  transforms into a frequency dependent variable resistor, which is given the designation  $D$ . Its

impedance is  $1/s^2C$ . The transformations to the FDNR configuration and the GIC implementation of the  $D$  element are given in Figure 10.10.

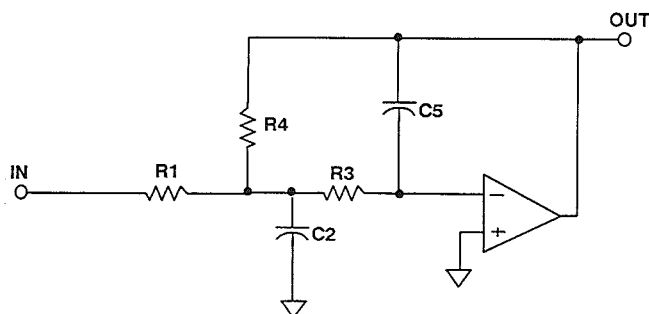
The advantage of the FDNR filter is that there are no op amps in the signal path which can add noise. It is also relatively insensitive to component variation. The advantages of the FDNR come at the expense of an increase in the number of components required.

For all of the realizations discussed above, the tabulated filter values are in terms of the lowpass function normalized to a frequency of 1 radian/second with an impedance level of  $1\Omega$ . To realize the final design, the filter values are scaled by the appropriate frequency and impedance.

Similarly, the lowpass prototype is converted to a highpass filter by scaling by  $1/s$  in the transfer function. In practice, this amounts to capacitors becoming inductors with a value  $1/C$ , and inductors becoming capacitors with a value of  $1/L$  for passive designs. For active designs, resistors become capacitors with a value of  $1/R$ , and capacitors become resistors with a value of  $1/C$ .

Transformation to the bandpass response is a little more complicated. If the corner frequencies of the bandpass are widely separated (by more than 2 octaves), the filter is made up of separate lowpass and highpass sections. In the case of a narrowband bandpass filter, the design is much more complicated, and is usually done using a computer program or design tables.

## MULTIPLE FEEDBACK REALIZATION



$F_O$  = Cutoff Frequency

$\alpha$  = Damping Ratio =  $1/Q$

$H$  = Absolute Value of Circuit Gain

Choose  $C_5$

$$K = 2\pi F_O C_1$$

$$C_2 = \frac{4C_5}{\alpha^2} (H + 1)$$

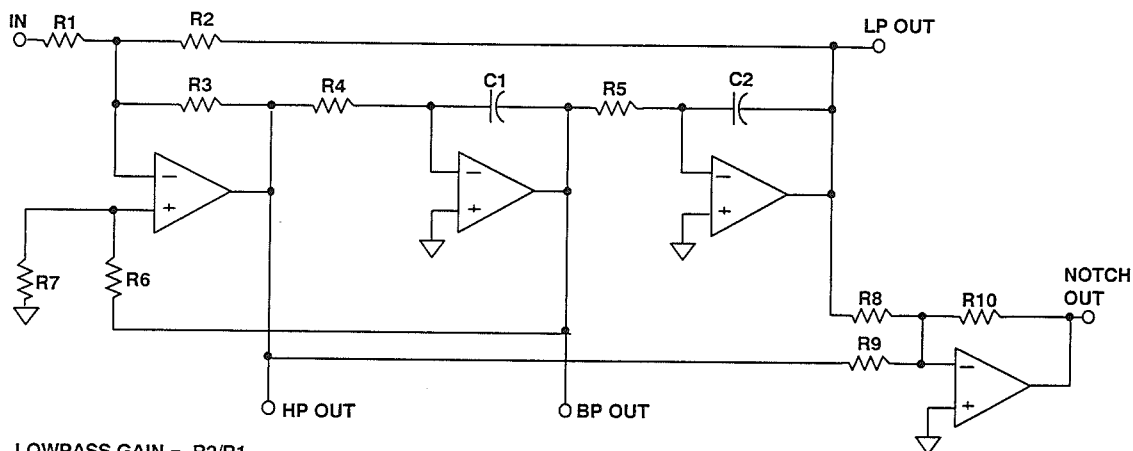
$$R_1 = \frac{\alpha}{2HK}$$

$$R_3 = \frac{\alpha}{2K(H + 1)}$$

$$R_4 = HR_1$$

Figure 10.8

## STATE VARIABLE REALIZATION



LOWPASS GAIN =  $-R_2/R_1$   
HIGHPASS GAIN =  $-R_3/R_1$

$$\text{BANDPASS GAIN} = \frac{R_6 + R_7}{R_1 R_7 \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} \right)}$$

$$F_O = \frac{1}{2\pi} \sqrt{\frac{R_3}{R_2 \cdot R_4 \cdot R_5 \cdot C_1 \cdot C_2}}$$

$$Q = \frac{1}{\alpha} = \frac{R_6 + R_7}{R_7} \left( \frac{1}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}} \right) \sqrt{\frac{R_4 \cdot C_1}{R_2 \cdot R_3 \cdot R_5 \cdot C_2}}$$

FOR NOTCH FREQUENCY =  $F_Z$

$$\text{FOR } F_O = F_Z, \frac{R_2 \cdot R_9}{R_3 \cdot R_8} = 1$$

$$\text{FOR } F_O > F_Z, \frac{R_2 \cdot R_9}{R_3 \cdot R_8} < 1$$

$$\text{FOR } F_O < F_Z, \frac{R_2 \cdot R_9}{R_3 \cdot R_8} > 1$$

$$\frac{F_Z^2}{F_O^2} = \frac{R_2 \cdot R_9}{R_3 \cdot R_8}$$

Figure 10.9

## FREQUENCY DEPENDENT NEGATIVE RESISTOR (FDNR) 1/S IMPEDANCE TRANSFORMATION

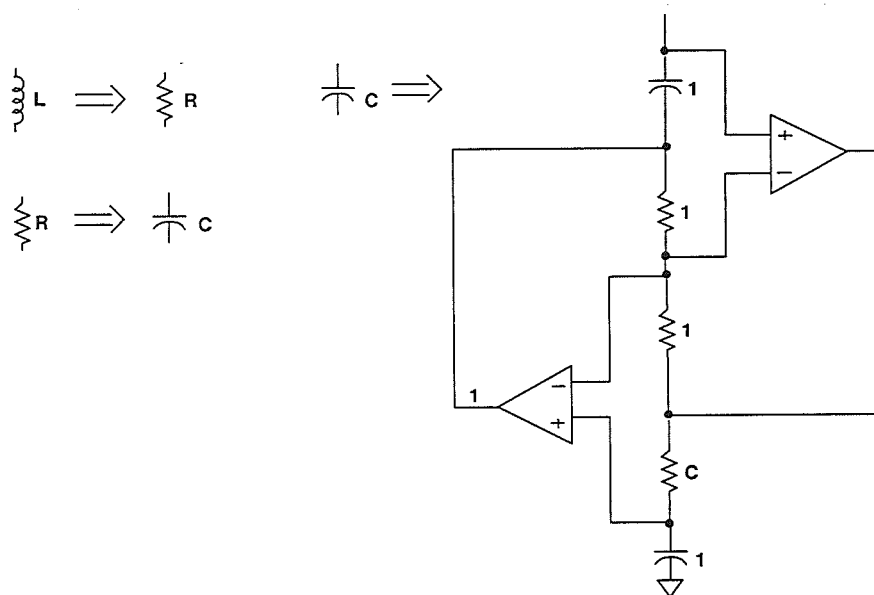


Figure 10.10

## SOME ACTIVE FILTER REALIZATIONS

- Sallen-Key: Good Phase Response, Least Dependent on Op Amp Performance, Sensitive to Element Values for High Q Sections
- Multiple Feedback: Less Sensitive to Element Values, High Q Sections Difficult due to Op Amp Open Loop Gain Limitations
- State-Variable: Most Precise, More Components, All Parameters Independently Adjustable
- Frequency Dependent Negative Resistance (FDNR): Op Amps not in Signal Path, More Components, Relatively Insensitive to Component Variations

Figure 10.11

## ANTIALIASING FILTER DESIGN EXAMPLE

We will now design passive and active antialiasing filters based upon the same specifications. The active filter will be designed in four ways: Sallen-Key, multiple feedback, state variable, and Frequency Dependent Negative Resistance (FDNR). We choose the

Butterworth filter in order to give the best compromise between attenuation and phase response.

The specifications for the filter are given in Figure 10.12.

### ANTIALIASING FILTER SPECIFICATIONS

- Cutoff Frequency  $F_C = 8\text{kHz}$
- Stopband Attenuation  $F_S$  at  $50\text{kHz} = 70\text{dB}$
- Best Balance Between Attenuation and Phase Response  
Choose Butterworth Design
- From Design Charts, for  $f = 6.25$  ( $50\text{kHz}/8\text{kHz}$ ),  $M = 5$

Figure 10.12

Consulting the design charts (Reference 1, p. 82), we see that for 70dB of attenuation at a frequency of 10.25 ( $50\text{kHz}/8\text{kHz}$ ), a fifth order filter is required.

We now consult the tuning tables (Reference 1, p. 341) and find:

### ALPHA AND $F_0$ VALUES FROM TUNING TABLES

Stage	Alpha	$F_0$
1	---	1.000
2	1.618	1.000
3	0.618	1.000

Figure 10.13

The first stage is a real pole, thus the lack of an alpha value. It should be noted that this is not necessarily the order of implementation in hardware. In general, you would typically put the real pole last and put the second order sections in order of decreasing alpha (increasing  $Q$ ).

For the passive design, we will choose the zero input impedance configuration. From the design table (Reference 1, p. 313), we find the following normalized values for the filter:

## **NORMALIZED PASSIVE FILTER VALUES FROM TABLES**

<b>L1 = 1.5451</b>	<b>C2 = 1.6944</b>
<b>L3 = 1.3820</b>	<b>C4 = 0.8944</b>
<b>L5 = 0.3090</b>	

**Figure 10.14**

These values are for a 1 rad/second filter with a 1  $\Omega$  termination. To scale the filter we divide all reactive elements by the desired cutoff frequency, 8kHz (50265 rad/sec). We also need to scale the impedance. For this example, we choose a value of 1000  $\Omega$ . To scale the impedance, we multiply all resistor and inductor values and divide all capacitor values by the impedance scaling factor. After scaling, the circuit looks like Figure 10.15.

For the Sallen-Key active filter, we use the design table shown in Figure 10.7. The values for C1 in each section are chosen to give reasonable resistor values. The implementation is shown in Figure 10.16. For the Sallen-Key realization to work correctly, it is assumed to have a zero-impedance driver, and a return path for dc. Both of these criteria are approximately met when you use an op amp to drive the filter.

## EXAMPLE FILTER-PASSIVE IMPLEMENTATION

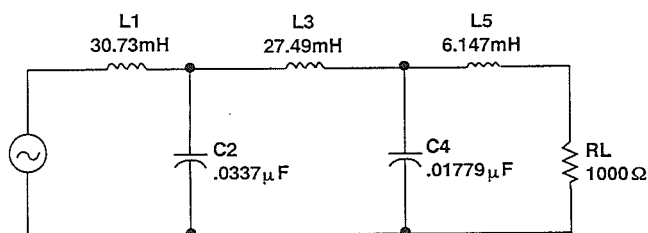


Figure 10.15

## EXAMPLE FILTER-SALLEN-KEY IMPLEMENTATION

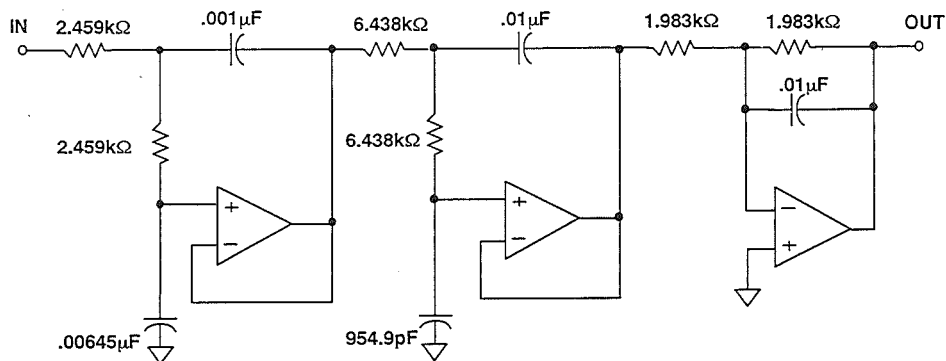


Figure 10.16



Figure 10.17 shows a multiple feedback realization of our filter. It was designed using the equations in Figure 10.8.

The state variable filter is shown in Figure 10.18, and the Frequency Dependent Negative Resistance (FDNR)

realization is shown in Figure 10.19. In the conversion process from passive to FDNR, the D element is normalized for a capacitance of 1F. We then scale the filter to a more reasonable value ( $0.01\mu\text{F}$  in this case).

### EXAMPLE FILTER- MULTIPLE FEEDBACK IMPLEMENTATION

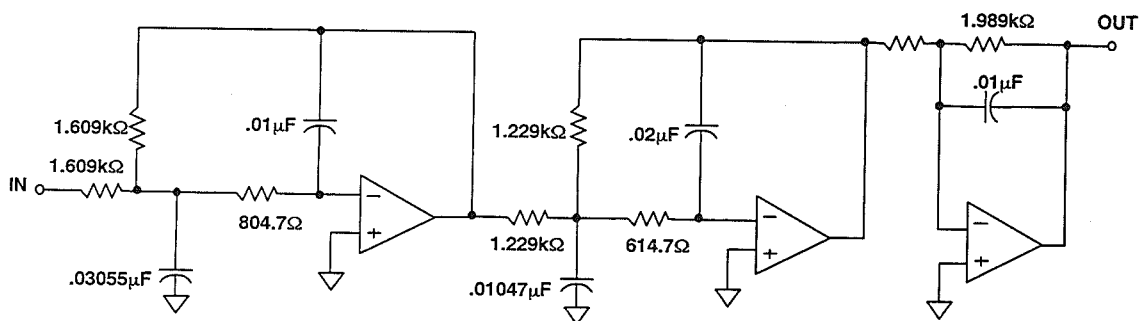


Figure 10.17

## EXAMPLE FILTER- STATE VARIABLE IMPLEMENTATION

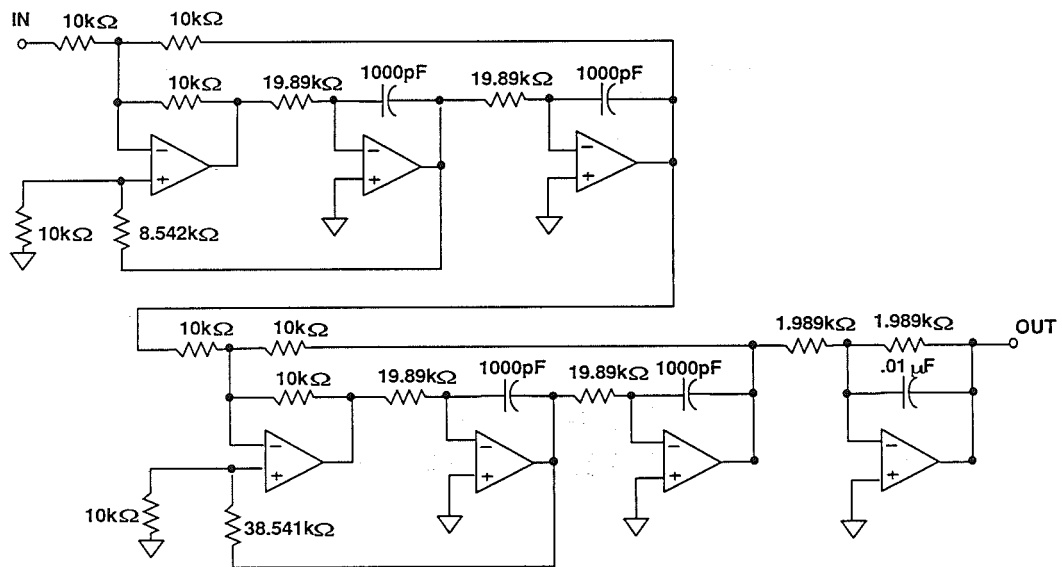


Figure 10.18

## EXAMPLE FILTER- FDNR IMPLEMENTATION

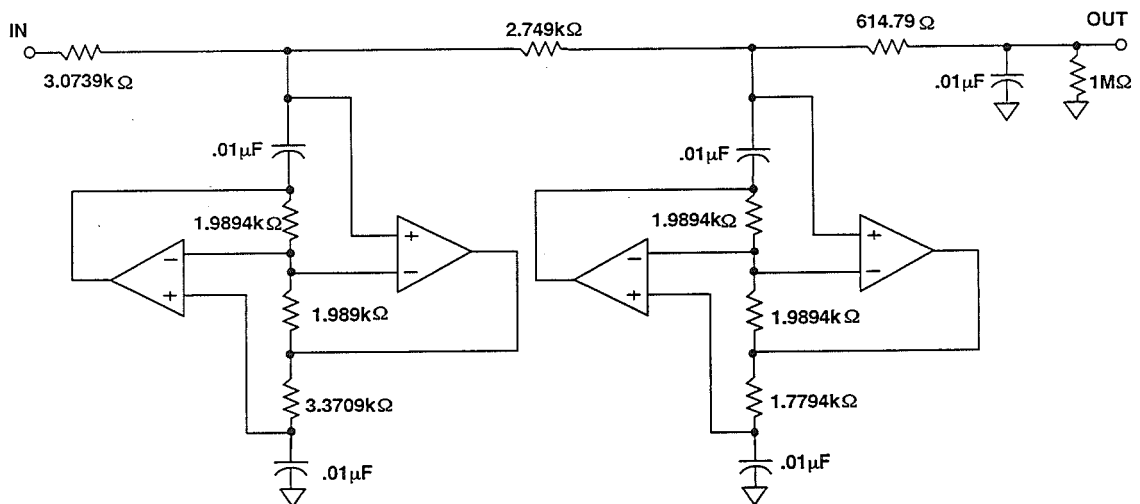


Figure 10.19

In all of the filters above, the values shown are the exact calculated values. These exact values are rarely obtainable. We must therefore either substitute the nearest standard value, or use series/parallel combinations. Any variation from the ideal values will cause a shift in the filter response characteristic, but often the effects are minimal. The computer can be used to evaluate these variations on the overall performance and determine if they are acceptable.

In active filter applications using op amps, the dc accuracy of the amplifier is often critical to optimal filter perfor-

mance. The amplifier's offset voltage will be passed by the filter and may be amplified to produce excessive output offset. For low frequency applications requiring large value resistors, bias currents flowing through these resistors will also generate an output offset voltage.

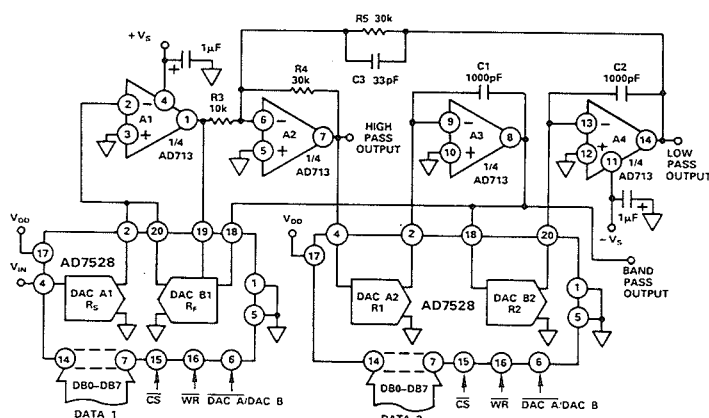
In addition, at higher frequencies, an op amp's dynamics must be carefully considered. Here, slewrate, bandwidth, and open loop gain play a major role in op amp selection. The slewrate must be fast as well as symmetrical to minimize distortion.

## A PROGRAMMABLE STATE VARIABLE FILTER

A programmable state variable filter using DACs is shown in Figure 10.20. DACs A1 and B1 control the gain and Q of the filter characteristic, while DACs A2 and B2 must accurately track for the simple expression for  $f_c$  to be true. This is readily accomplished using two AD7528 DACs and one AD713 quad op amp.

Capacitor C3 compensates for the effects of op amp and gain-bandwidth limitations. This filter provides lowpass, highpass, and bandpass outputs, and is ideally suited for applications where digital control of filter parameters is required. The programmable range for component values shown is  $f_c = 0$  to 15kHz, and  $Q = 0.3$  to 4.5.

## A PROGRAMMABLE STATE VARIABLE FILTER CIRCUIT



### CIRCUIT EQUATIONS

$$C_1 = C_2, R_1 = R_2, R_4 = R_5$$

$$f_c = \frac{1}{2\pi R_1 C_1}$$

$$Q = \frac{R_3}{R_4} \cdot \frac{R_F}{R_{FBB1}}$$

$$A_0 = -\frac{R_F}{R_S}$$

### NOTE:

DAC equivalent resistance equals  
 $\frac{256 \times (\text{DAC Ladder resistance})}{\text{DAC Digital Code}}$

Figure 10.20

## SEVEN-POLE FDNR 20kHz ANTIALIASING FILTER

Figure 10.21 shows a 7-pole antialiasing filter for a 2x oversampling (88.2kSPS) digital audio application. This filter has less than 0.05dB pass-band ripple and  $19.8 \pm 0.3\mu\text{s}$  delay, dc-

20kHz. The filter will handle a 5V rms signal ( $V_s = \pm 15\text{V}$ ) with no overload at any internal nodes. The frequency response of the filter is shown in Figure 10.22.

### 20KHZ FDNR AUDIO ANTIALIASING FILTER

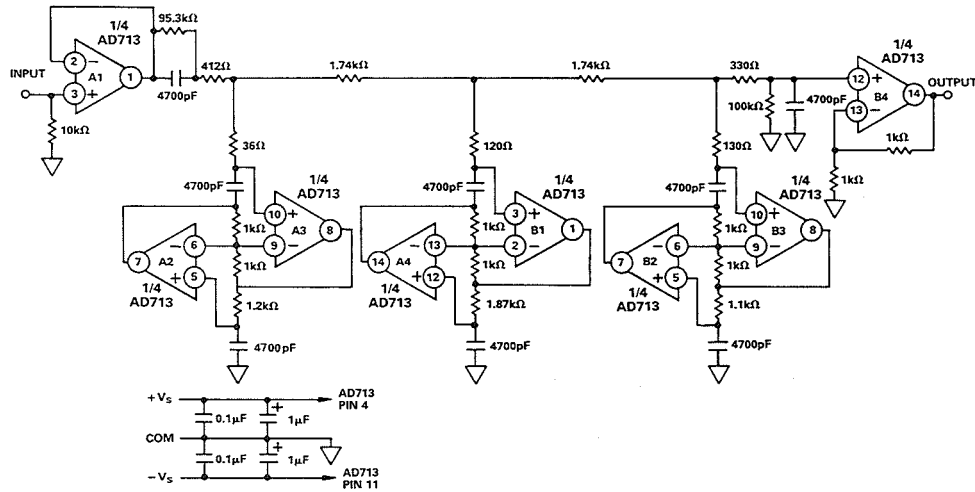


Figure 10.21

### AUDIO ANTIALIASING FILTER RESPONSE

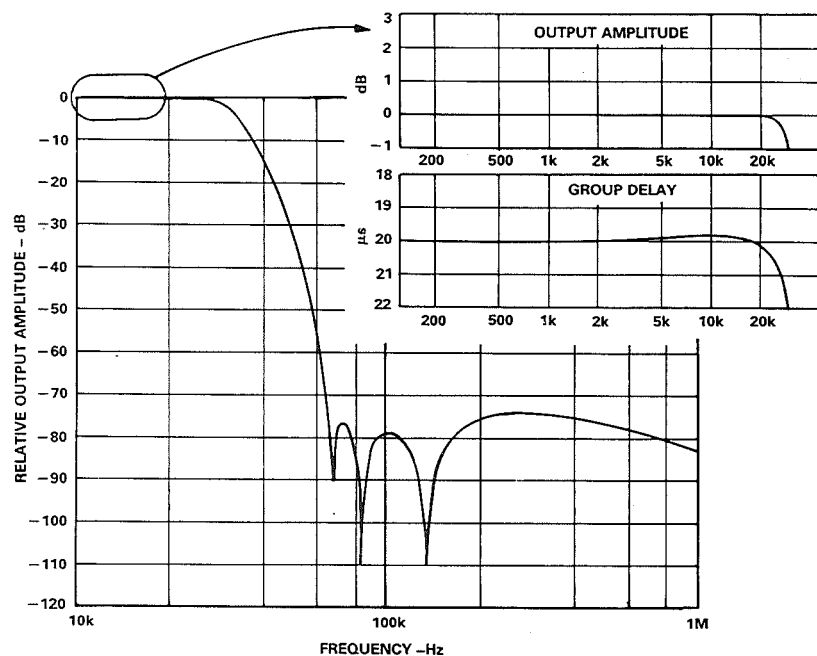


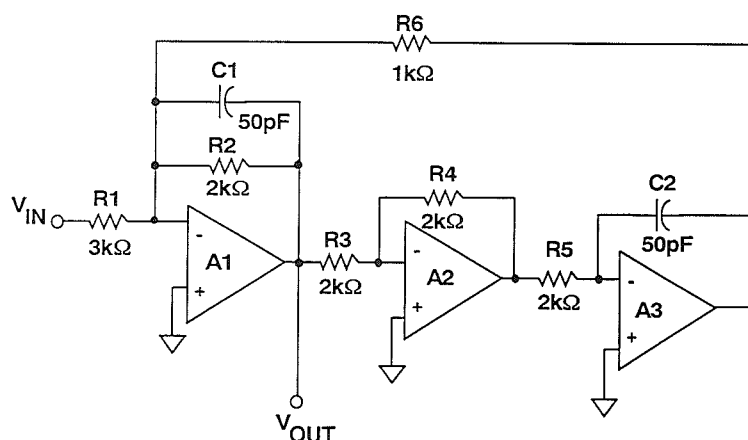
Figure 10.22

## 2 MHz BIQUAD BANDPASS FILTER USING A 30MHz QUAD AMPLIFIER

Figure 10.23 shows a circuit for a biquad bandpass filter with a 2MHz center frequency. This type of filter is often used in ultrasound receivers to detect a 2MHz signal, while rejecting all

others. The OP-467 is ideal for such an application because of its wide bandwidth and quad package. With four amplifiers, the OP-467 allows this circuit to be built using only one IC.

### A 2MHz BIQUAD BANDPASS FILTER USING A 30MHz QUAD AMPLIFIER



A1, A2, A3 ARE 1/4 OP-467

Figure 10.23

The 30MHz bandwidth is sufficient to accurately produce the 2MHz center frequency, as the measured response shows in Figure 10.24. Notice that the center frequency is exactly 2MHz, and the gain is unity. A lower speed amplifier would cause the center frequency to shift significantly. For example, using an op amp with a 10MHz gain-bandwidth product results in 20% shift in the center frequency to 1.6MHz, even though the same component values are

used. When the bandwidth is too close to the filter's center frequency, the amplifiers' internal phase shift causes excess phase shift at 2MHz, which alters the filter's response. In fact, if the chosen op amp has a bandwidth close to 2MHz, the combined phase shift of the three op amps will cause the loop to oscillate. The OP-467 has a high enough bandwidth such that it contributes only a small amount of phase shift at 2MHz.

### 2MHz BIQUAD BANDPASS FILTER FREQUENCY RESPONSE

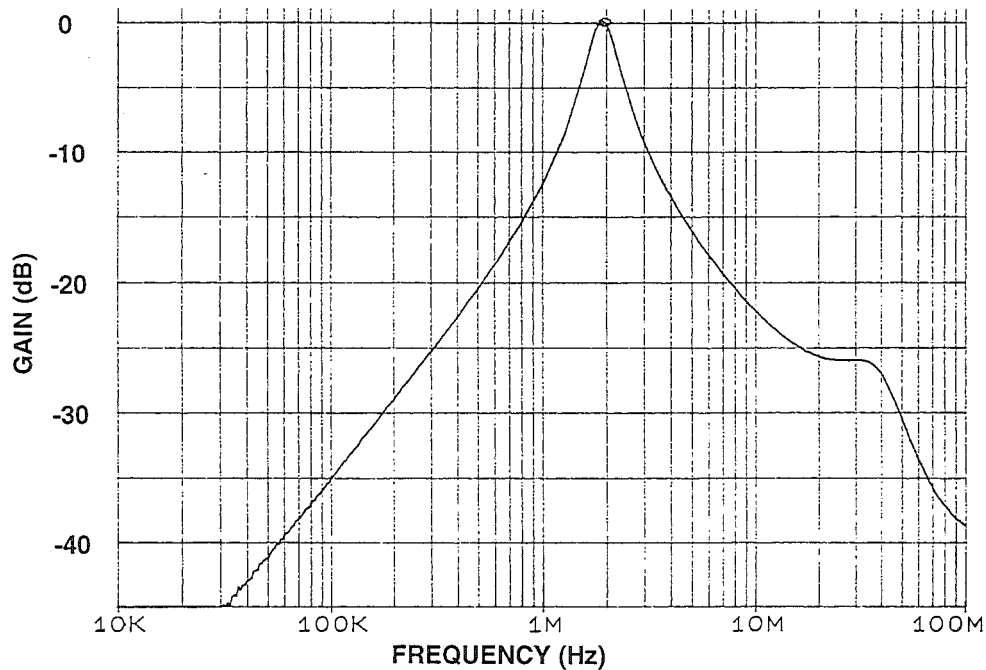


Figure 10.24

Careful consideration must be given to the layout of this circuit, as with any high speed circuit. As mentioned above, if the phase shift is too large at 2MHz, the filter's response will be altered, or worse, it will oscillate. Any parasitic capacitance will cause additional phase shift. Thus care must be taken to minimize this capacitance, especially on the inverting inputs to the amplifiers. The traces connected to this node should be kept short and the ground plane removed from this area.

The OP-467 allows the entire circuit to be built with only one package, which was not possible before. Additionally, the one additional op amp in the package can be used elsewhere in the circuit to provide gain or buffering. If the op amp is not used, then it should be configured as a voltage follower with the positive input grounded and no load on the output. This ensures that it will not oscillate.

## PRACTICAL PROBLEMS IN FILTER IMPLEMENTATION

In the introductory section we dealt with filters as mathematical functions. The filter designs were assumed to be implemented with “perfect” compo-

nents. It's only when the filter is built with real-world components that design tradeoffs must be made.

### PRACTICAL CONSIDERATIONS IN FILTER IMPLEMENTATION

- Higher Order Filters Require Accurate First and Second Order Sections: Q and Frequency Response
- Passive Component Inaccuracies, Parasitics, and Drift
- Active Component Frequency Response, Input and Output Impedance, and Distortion

Figure 10.25

In building a filter with an order greater than two, multiple second and/or first order sections are used. The frequencies and Qs of these sections must align precisely or the overall response of the filter will be affected. For example, the antialiasing filter design example previously discussed is a 5th order Butterworth filter, made up of a second order section with a frequency ( $F_0$ ) = 1

and a  $Q = 1.618$ , a second order section with a frequency ( $F_0$ ) = 1 and a  $Q = 0.618$ , and a first order section with a frequency ( $F_0$ ) = 1 (for a filter normalized to 1 rad/sec). If the Q or frequency response of any of the sections is off slightly, the overall response will deviate from the desired response. It may be close, but it won't be exact.

## PASSIVE COMPONENTS (RESISTORS, CAPACITORS, INDUCTORS)

Passive components are the first problem. When designing filters, values of components may be required that are not available commercially. Resistors, capacitors, and inductors come in standard values. While custom values can be ordered, the practical tolerance will still be  $\pm 1\%$  at best. An alternative is to build the required value out of a series and/or parallel combination of standard values. This increases the cost and size of the filter. Not only is the cost of components increased, but so are the manufacturing costs, both for loading

and for tuning the filter. Furthermore, its success will be still limited by the number of parts that are used, their tolerance, and their tracking.

A more practical way is to use a circuit analysis program to determine the response using standard values. The program can also evaluate the effects of component drift over temperature. The values of the sensitive components are adjusted using parallel combinations where needed, until the response is within the desired limits.

## RESISTOR CONSIDERATIONS

- Accuracy (Using Standard Values) and Temperature Coefficient
- Select Values Between  $100\Omega$  and  $1M\Omega$
- Use Metal Film if Possible
- Ratio Match for Minimum Error

Figure 10.26

In addition to the initial tolerance of the components, you must also evaluate the effects of temperature drift. The temperature coefficients of the various components may be different in both

magnitude and sign. Capacitors, especially, are difficult in that not only do they drift, but the temperature coefficient is also a function of temperature as shown in Figure 10.27.



## CAPACITANCE CHANGE VERSUS TEMPERATURE

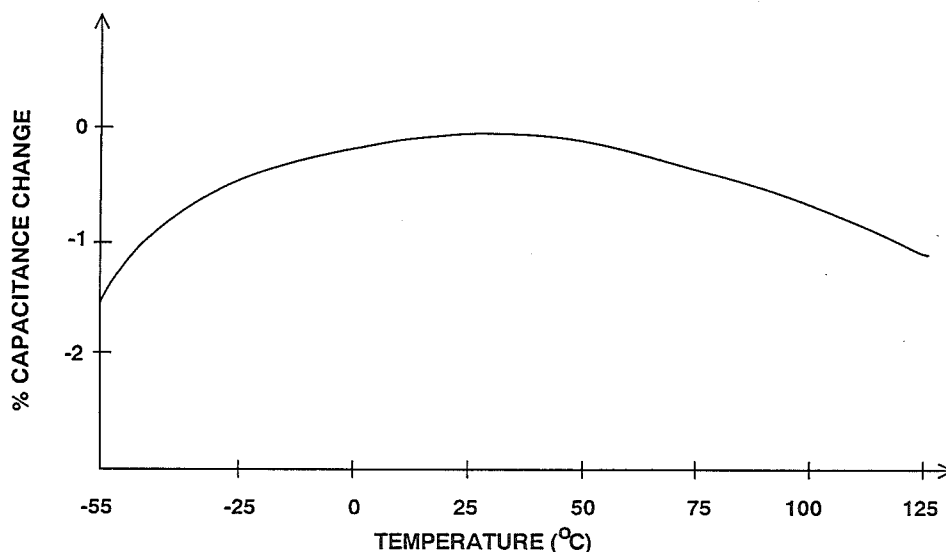


Figure 10.27

Capacitors also have temperature coefficients, with the lowest TC dielectrics being NPO (or COG) ceramic ( $\pm 30\text{ppm}/^\circ\text{C}$ ), and polystyrene

( $-120\text{ppm}/^\circ\text{C}$ ). Some capacitors, mainly the plastic film types, such as polystyrene and polypropylene, have a limited temperature range.

## CAPACITOR CONSIDERATIONS

- Accuracy (Using Standard Values) and Temperature Coefficient
- Parasitics: Inductance, Leakage, Dielectric Absorbtion
- Select Values Between  $10\text{pF}$  and  $10\mu\text{F}$
- Avoid Electrolytics
- Polystyrene or NPO Ceramics are Preferable for Lowest Linear TC

Figure 10.28

The frequency and  $Q$  of a filter are determined by the component values. Obviously, if the component value is drifting, the frequency and the  $Q$  of the filter will drift which, in turn, will cause the frequency response to vary. This is especially true in higher order filters. Higher order means that you will have higher  $Q$  sections. Higher  $Q$  sections means that component values are more critical, since the  $Q$  is typically set by the ratio of two components, usually capacitors.

While there is infinite choice of the values of the passive components for building filters, in practice there are physical limits. Capacitor values below 10pF and above 10 $\mu$ F are not practical. Electrolytic capacitors should be avoided in circuits requiring any sort of accuracy. Electrolytic capacitors are also very leaky, and if they are operated without a polarizing voltage, they become non-linear when the ac voltage reverse biases them. Even with a dc polarizing voltage, the ac signal can reduce the instantaneous voltage to 0 or below. Large values of film capacitors are physically very big.

Resistor values of less than 100 $\Omega$  should be avoided, as should values over 1M $\Omega$ . Very low resistance values (under 100 $\Omega$ ) require a great deal of drive current and dissipate a great deal of power. Both of these should be avoided. Very large values tend to be

more prone to parasitics. Noise also increases with the square root of the resistor value.

Parasitic capacitances due to circuit layout and other sources affect the performance of the circuit. They can form between two traces on a PC board (on the same side or opposite side of the board), between leads of adjacent components, and just about everything else you can (and in most cases can't) think of. These capacitances are usually small, so their effect is greater at high impedance nodes. Thus, they can be controlled most of the time by keeping the impedance of the circuits down. Remember that the effects of stray capacitance are frequency dependent, being worse at high frequencies because the impedance drops with increasing frequency.

Parasitics are not just associated with outside sources. They are also present in the components themselves.

A capacitor is more than just a capacitor in most instances. A real capacitor has inductance (from the leads and other sources) and resistance as shown in Figure 10.29. This resistance shows up in the specifications as leakage and poor power factor. Obviously, we would like capacitors with very low leakage and good power factor (see Figure 10.30). Resistors also have inductances.

## EQUIVALENT CIRCUITS OF A REAL CAPACITOR

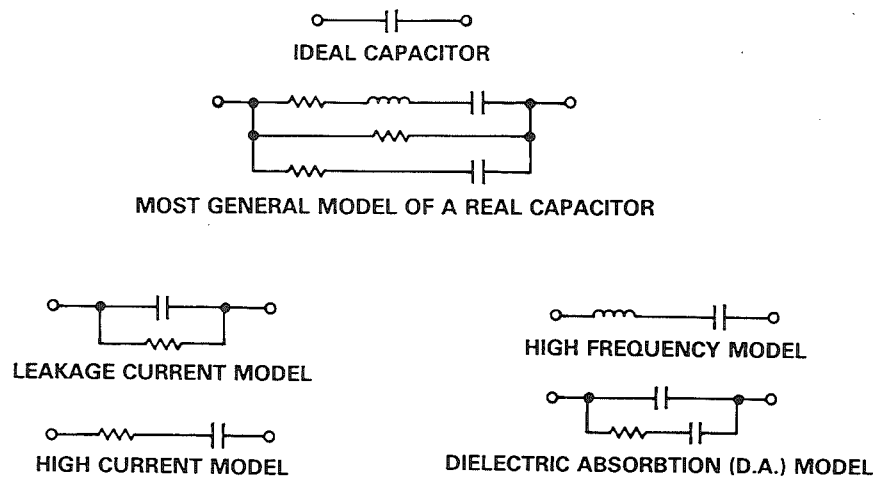


Figure 10.29

# CAPACITOR COMPARISON CHART

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	<0.1%	Small case size Inexpensive Good stability Wide Range of Values Many Vendors Low Inductance	DA generally low, but may not be specified Limited to small values ( $\leq 10\text{nF}$ )
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Damaged by Temperature $> +85^\circ\text{C}$ Large Case Size High Inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Damaged by Temperature $> +105^\circ\text{C}$ Large Case Size High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational above $+125^\circ\text{C}$ Wide Range of Values	Relatively Expensive Large High Inductance
MOS	0.01%	Good DA Small Operational above $+125^\circ\text{C}$ Low Inductance	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-bit Applications High Inductance
Polyester	0.3% to 0.5%	Moderate Stability Low Cost Wide Temperature Range Low Inductance (Stacked Film)	Large DA Limits to 8-bit Applications High Inductance
Monolithic Ceramic (High K)	$>0.2\%$	Low Inductance Wide Range of Values	Poor Stability Poor DA High Voltage Coefficient
Mica	$>0.003\%$	Low Loss at HF Low Inductance Very Stable Available in 1% Values or Better	Quite Large Low Values ( $<10\text{nF}$ ) Expensive
Aluminum Electrolytic	High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability Poor Accuracy Inductive
Tantalum Electrolytic	High	Small Size Large Values Medium Inductance	Quite High Leakage Usually Polarized Expensive Poor Stability Poor Accuracy

Figure 10.30

## RESISTOR COMPARISON CHART

TYPE		ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size Wide Range of Values	Poor Tolerance (5%) Poor Temperature Coefficient (1500 ppm/°C)
	Wirewound	Excellent Tolerance (0.01%) Excellent TC (1 ppm/°C) High Power	Reactance is a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100 ppm/°C) Moderate Cost Wide Range of Values Low Voltage Coefficient	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to < 1 ppm/°C) Low Reactance Low Voltage Coefficient	Low Power Very Expensive
	High Megohm	Very High Values ( $10^8$ to $10^{14}\Omega$ ) Only Choice for Some Circuits	High Voltage Coefficient (200 ppm/V) Fragile Glass Case (Needs Special Handling) Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimable Readily Available	Fair Matching (0.1%) Poor TC (>100 ppm/°C) Poor Tracking TC (10 ppm/°C)
	Thin Film	Good Matching (<0.01%) Good TC (<100 ppm/°C) Good Tracking TC (2 ppm/°C) Moderate Cost Laser-Trimable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Limited Values and Configurations

**Figure 10.31**

In general, it is best to use plastic film (preferably polystyrene) or mica capacitors and metal film resistors, both of moderate to low values in our filters.

One way to reduce component parasitics is to use surface mounted devices. Not having leads means that the lead

inductance is reduced. Also, being physically smaller allows more optimal placement. A disadvantage is that not all types of capacitors are available in surface mount. Ceramic capacitors are popular surface mount types, and of these, the NPO family have the best characteristics for filtering.

## **LIMITATIONS OF ACTIVE ELEMENTS (OP AMPS) IN FILTERS**

The active element of the filter will also have a pronounced effect on the response.

In developing the various topologies (Multiple Feedback, Sallen-Key, State Variable, etc.), the active element was always modeled as a "perfect" operational amplifier. That is to say it has:

- 1) infinite gain
- 2) infinite input impedance
- 3) zero output impedance

none of which vary with frequency. While amplifiers have improved a great deal over the years, this model has not yet been realized.

## **CONSIDERATIONS FOR OP AMPS**

- Finite Gain-Bandwidth
- Input Impedance
- Output Impedance
- Distortion
- Noise

Figure 10.32

The most important limitation of the amplifier has to do with its gain variation with frequency. All amplifiers are band limited. This is due mainly to the physical limitations of the devices with which the amplifier is constructed. Negative feedback theory tells us that the response of an amplifier must be first order ( $-6\text{dB}$  per octave) when the gain falls to unity in order to be stable. To accomplish this, a real pole is usually introduced in the amplifier so the gain rolls off to  $< 1$  by the time the phase shift reaches  $180^\circ$  (plus some phase margin, hopefully). This roll off is equivalent to that of a single pole filter. So in simplistic terms, the transfer function of the amplifier is added to the transfer function of the filter to give a composite function. How much the

frequency dependent nature of the op amp affects the filter is dependent on which topology is used.

The Sallen-Key configuration, for instance, is the least dependent on the frequency response of the amplifier. All that is required is for the amplifier response to be flat to just past the frequency where the attenuation of the filter is below the minimum attenuation required. This is because the amplifier is used as a gain block. Beyond cutoff, the attenuation of the filter is reduced by the rolloff of the gain of the op amp. This is because the output of the amplifier is phase shifted, which results in incomplete nulling when fed back to the input.

## **SALLEN KEY SENSITIVITY TO OP AMP**

- **Least Dependent on Op Amp Frequency Response.  
Op Amp Used As Gain Block**
- **Op Amp Flat to Slightly Beyond Filter Stopband  
Frequency**
- **Can Use Current Feedback Op Amps in Sallen Key  
Configuration**

**Figure 10.33**

The state variable configuration uses the op amps in two modes, as amplifiers and as integrators. As amplifiers, the constraint on frequency response is the same as for the Sallen-Key, that is flat out to the minimum attenuation frequency. As an integrator, however, more is required. A good rule of thumb is that the open loop gain of the amplifier must be greater than 10 times the closed loop gain. This should be taken as the absolute minimum requirement. What this means is that there must be 20dB loop gain, minimum. Therefore, an op amp with 10MHz unity gain bandwidth can be used to make a 1MHz integrator. What happens is that the effective  $Q$  of the circuit increases as loop gain decreases. This phenomenon is called  $Q$  enhancement. The mecha-

nism for  $Q$  enhancement is similar to that of slew rate limitation. Without sufficient loop gain, the op amp virtual ground is no longer at ground. In other words, the op amp is no longer behaving as a op amp. Because of this, the integrator no longer behaves like an integrator.

The multiple feedback configuration also places heavy constraints on the active element.  $Q$  enhancement is a problem in this topology as well. As the loop gain falls, the  $Q$  of the circuit increases, and the parameters of the filter change. The same rule of thumb as used for the integrator apply to the multiple feedback topology (loop gain should be at least 20dB).

## STATE VARIABLE SENSITIVITY TO OP AMP

- Op Amps Used as Amplifiers and Integrators
- Amplifiers: Flat to Beyond Stopband Frequency
- Integrators: 20dB Minimum Loop Gain (Open Loop Gain 10 Times Closed Loop Gain), or  $Q$  Enhancement Occurs
- 10MHz Unity-Gain Bandwidth Op Amp Can Make a 1MHz Integrator

Figure 10.34



## MULTIPLE FEEDBACK SENSITIVITY TO OP AMP

- Same Rule of Thumb as for Integrators: 20dB Minimum Loop Gain to Prevent Q Enhancement

Figure 10.35

In the FDNR realization, the requirements for the op amps are not as clear. To make the circuit work, we assume that the op amps will be able to force the input terminals to be the same voltage. This implies that the loop gain be a minimum of 20dB at the resonant frequency. Also it is generally consid-

ered to be advantageous to have the two op amps in each leg matched. This is easily accomplished using dual op amps. It is also a good idea to have low bias current devices for the op amps, so FET input op amps should be used, all other things being equal.

## FDNR SENSITIVITY TO OP AMP

- Loop Gain Should be 20dB Minimum at Resonant Frequency
- Match Op Amps in Each Leg (Use Duals)
- Use FET Input Op Amps for Low Bias Currents

Figure 10.36

In addition to the frequency dependent limitations of the op amp, several other of its parameters may be important to the filter designer.

One is input impedance. As we said, the filter topologies assume “perfect” amplifiers. This implies that the input impedance is infinite. This is required so that the input of the op amp does not load

the network around it. This means that we probably want to use FET amplifiers with high impedance circuits. There is also a small frequency dependent term to the input impedance, since the effective impedance is the real input impedance multiplied by the loop gain. This usually is not a major source of error, since the network impedance of a high frequency filter should be low.

## OTHER OP AMP CONSIDERATIONS IN FILTERS

- Input and Output Impedance
- Distortion at Low Loop Gains
- Noise
- Dynamic Range (Overload),  $Q \text{ times Gain} < \text{Loop Gain}$
- Current Feedback Op Amps May Only be Used in Sallen Key Configuration

Figure 10.37

Similarly, the op amp output impedance affects the response of the filter. The output impedance of the amplifier is divided by the loop gain, therefore the output impedance will rise with increasing frequency. This may have an effect with high frequency filters if the output impedance of the stage driving the filter becomes a significant portion of the network impedance.

The fall of loop gain with frequency can also affect the distortion of the op amp, since there is less loop gain available for correction. In the multiple feedback configuration the feedback loop is also frequency dependent, which may further reduce the feedback correction, resulting in increased distortion. This effect is counteracted somewhat by the reduction of distortion components in

the filter network (assuming a lowpass or bandpass filter).

All of the discussion so far is based on using classical voltage feedback op amps. Current feedback, or transimpedance, op amps offer improved high frequency response, but are unusable in any topology except the Sallen-Key. The problem is that capacitance in the feedback loop of a current feedback amplifier usually causes it to become unstable. Also, most current feedback amplifiers will only drive small capacitive loads. Therefore, it is difficult to build classical integrators using current feedback amplifiers. Some current feedback op amps have an external pin which may be used to configure them as a very good integrator, but this configuration does not lend

itself to classical active filter designs. Current feedback integrators are non-inverting, which is not acceptable in the state variable configuration. Also, the bandwidth of a current feedback amplifier is set by its feedback resistor, which would make the Multiple Feedback topology difficult to implement. Another limitation of the current feedback amplifier in the Multiple Feedback configuration is the low input impedance of the inverting terminal. This would result in loading of the filter network. Sallen-Key filters are possible with current feedback amplifiers, since the amplifier is used as a non-inverting gain block. New topologies which capitalize on the current feedback amplifiers superior high frequency performance and compensate for its limitations will have to be developed.

The last thing that you need to be aware of is exceeding the dynamic

range of the amplifier.  $Q$ s over 0.707 will cause peaking in the response of the filter (see Figure 10.38). For high  $Q$ s, this could cause overload of the input or output stages of the amplifier with a large input. Note that relatively small values of  $Q$  can cause significant peaking. The  $Q$  times the gain of the circuit must stay under the loop gain (plus some margin, again, 20dB is a good starting point). This holds for multiple amplifier topologies as well. Be aware of internal node levels, as well as input and output levels. As an amplifier overloads, its effective  $Q$  decreases, so the transfer function will appear to change even if the output appears undistorted. This shows up as the transfer function changing with increasing input level.

### EFFECT OF FILTER $Q$ ON GAIN PEAKING

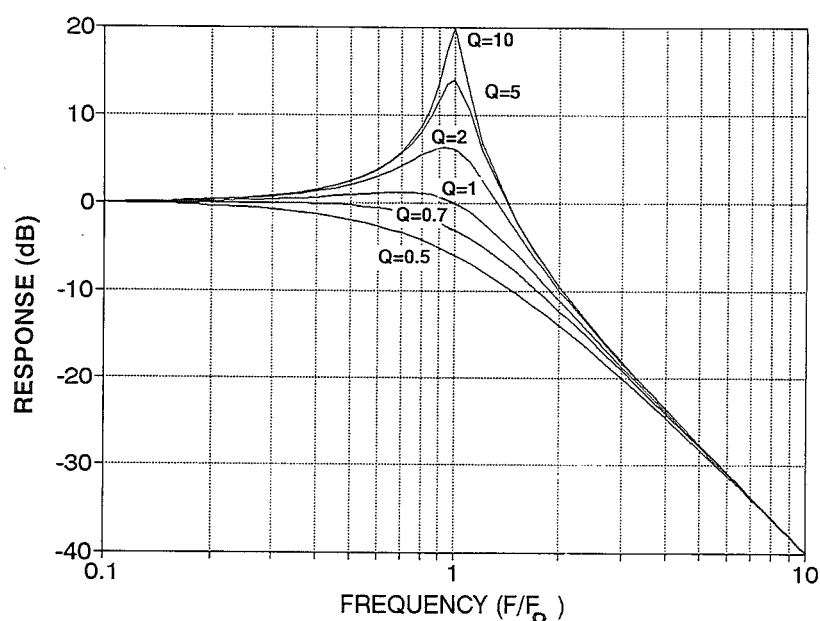


Figure 10.38

We have been dealing mostly with lowpass filters in our discussions, but the same principles are valid for highpass, bandpass, and band reject as well. In general, things like  $Q$  enhancement and limited gain/bandwidth will not affect highpass filters, since the resonant frequency will probably be low in relation to the cutoff frequency of the op amp. Remember, though, that the

highpass filter will have a low pass section, by default, at the cutoff frequency of the amplifier. Bandpass and band reject (notch) filters will be affected, especially since both tend to have high values of  $Q$ . The general effect of the op amp's frequency response on the filter  $Q$  is shown in Figure 10.39.

### Q ENHANCEMENT

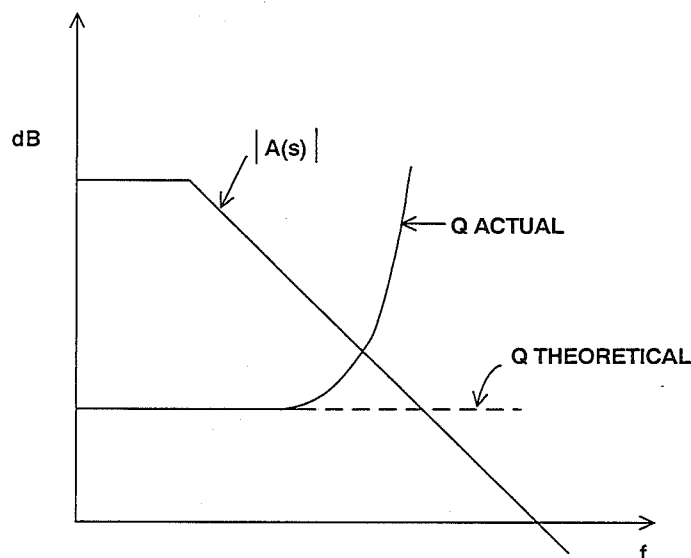


Figure 10.39

As an example of the  $Q$  enhancement phenomenon, consider the Spice simulation of a 10kHz bandpass Multiple Feedback filter with  $Q = 10$  and gain = 1, using a good high frequency amplifier (the AD847) as the active device. The circuit diagram is shown in Figure 10.40. The open loop gain of the AD847 is greater than 70dB at 10kHz as shown in Figure 10.41. This is well over the 20dB minimum, so the filter works as designed as shown in Figure 10.42. We now replace the AD847 with an OP-

90. The OP-90 is a dc precision amplifier and so has a limited bandwidth. In fact, its open loop gain is less than 10dB at 10kHz (see Figure 10.41). This is not to imply that the AD847 is in all cases better than the OP-90. It is a case of misapplying the OP-90. From the output for the OP-90, also shown in Figure 10.42, we see that the magnitude of the output has been reduced, and the center frequency has shifted downward.

## 10kHz MULTIPLE FEEDBACK BANDPASS FILTER

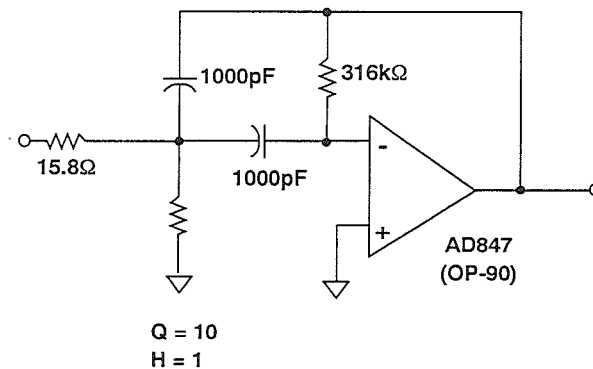


Figure 10.40

## OPEN LOOP GAIN OF AD847 AND OP-90 OP AMPS

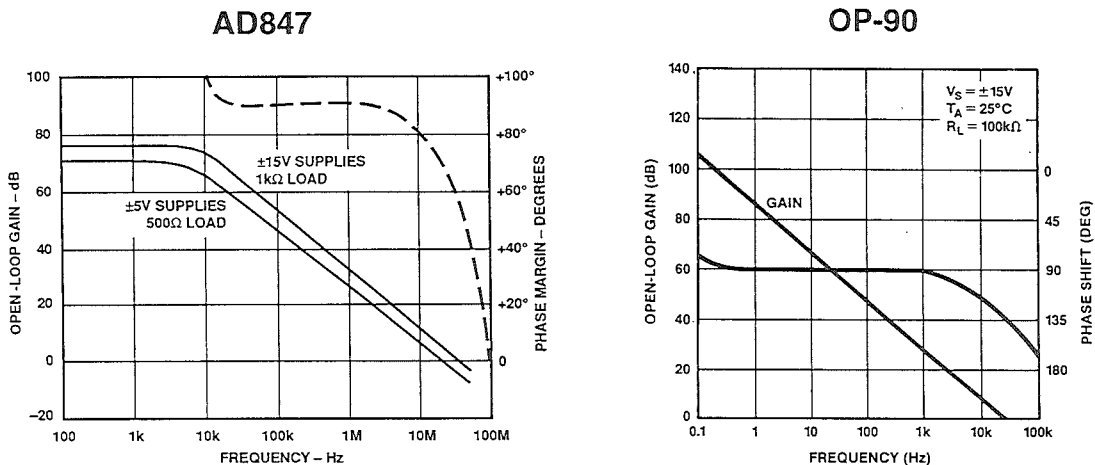


Figure 10.41

## FREQUENCY RESPONSE OF 10kHz BANDPASS FILTER USING AD847 AND OP-90 OP AMPS

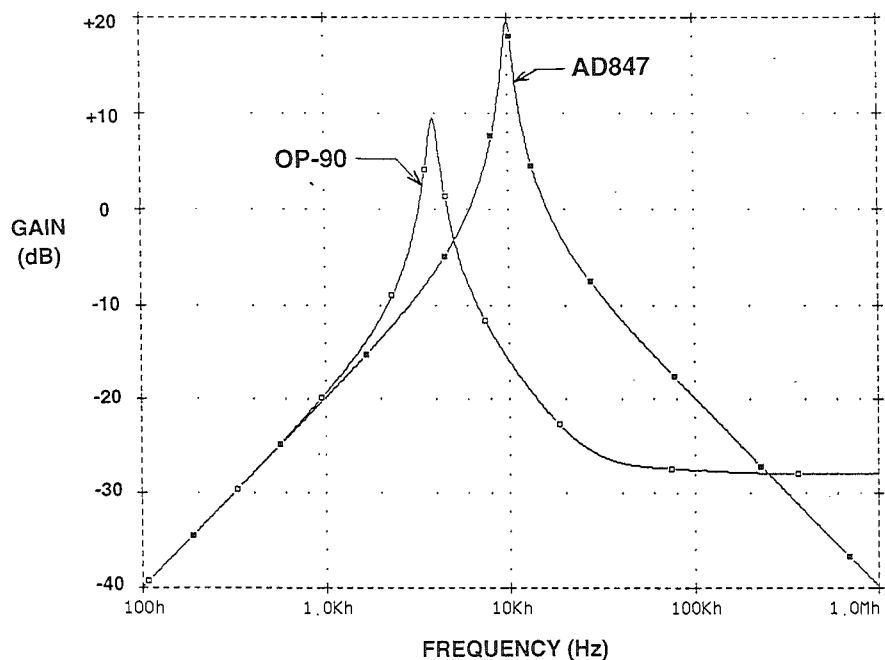


Figure 10.42

## A 12MHz Sallen-Key Filter Using a Current Feedback Amplifier

As a demonstration of a high frequency filter, we will design a 12MHz Sallen-Key filter using a transimpedance amplifier (the AD9617) as the active device (see Figure 10.43). Here we see that the corner frequency of the filter is slightly less than the design value of 12MHz (see Figure 10.44). Also note that the attenuation is only good to

about 100MHz. This is where the loop gain of the amplifier starts to decrease. Now, since the output of the amplifier is phase shifted relative to its input, there is incomplete nulling of the signal. Also, as the impedance of the filter network decreases, it reaches the point where it starts to bypass the amplifier.

### 12 MHz Sallen-Key Lowpass Filter with Butterworth Response Uses Current Feedback Amplifier

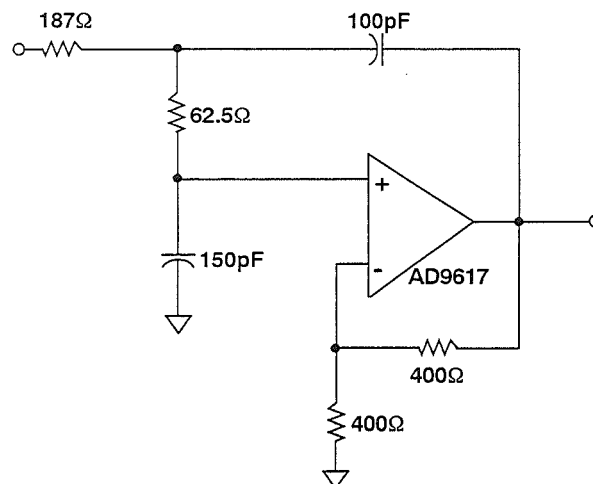


Figure 10.43



## FREQUENCY RESPONSE OF 12MHz SALLEN-KEY LOWPASS FILTER

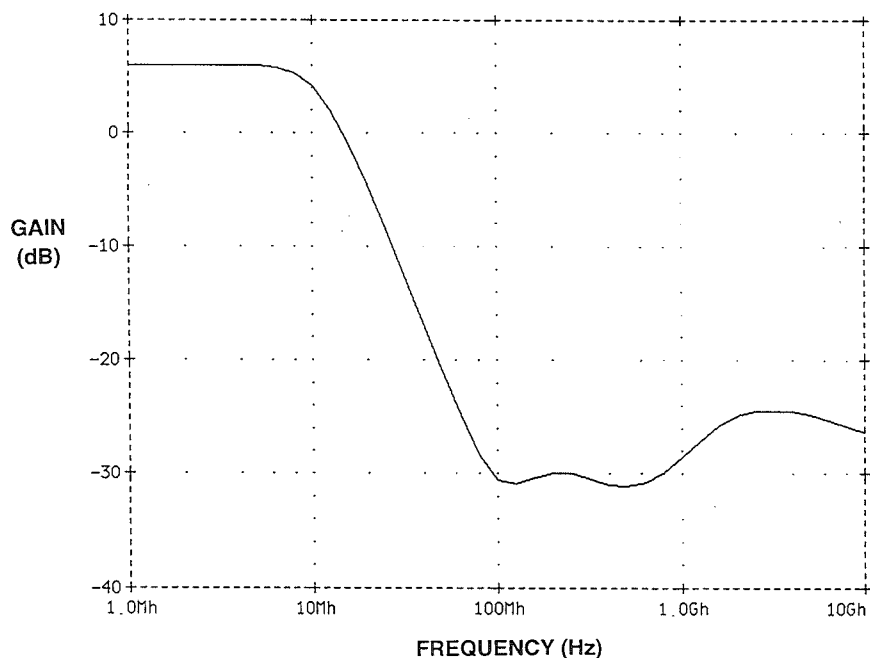


Figure 10.44

## SWITCHED CAPACITOR FILTERS

Signals were once filtered entirely in the continuous analog domain by configurations of passive components (typically inductors, resistors, and capacitors). Later, active filters, with op amps for buffering and gain, provided filter designers with additional flexibility and performance, but still operated continuously on analog signals. DSP led to stable and flexible discrete-time digital filters, where sampled analog signals are processed entirely by numerical calculations with filtering algorithms—some of which cannot be realized with continuous-time analog filters.

Switched-capacitor filters (SCFs) are an intermediate class, combining both continuous- and discrete-time aspects. They are usually implemented using CMOS switches and capacitors to simulate the behavior of resistors, therefore, many filter architectures can be realized entirely by a monolithic device without the need for external components. SCFs are particularly useful for voice and audio bandwidth signal applications in conjunction with DSP technology. Since SCFs are *sampling* devices, all the concepts of discrete time sampling apply to their use: Nyquist's theorem, aliasing, etc.

## SUMMARY OF FILTERING TECHNIQUES

- Crystals, SAWs
- Passive Components (R, L, and C)
- Active Filters (R, C, and Op-Amps)
- Switched Capacitor Filters (CMOS Switches and Capacitors Replace Resistors)
- Digital Filters (Numerical Realizations Which May Have No Analog Counterpart)

Figure 10.45

The fundamental concept of a switched capacitor acting as a resistor can best be understood from the concept of charge transfer as shown in Figure 10.46. If the capacitor is switched from  $V_1$  to  $V_2$ , an instantaneous charge transfer occurs,  $\Delta Q = C(V_1 - V_2)$ , either into or out of  $V_2$ . This assumes that  $C$  has no series resistance, and that  $V_1$  and  $V_2$  are ideal voltage sources. If the

switch is thrown back and forth at a clock frequency,  $f_s$  (having a period  $T$ ), then an average current,  $i$ , flows between  $V_1$  and  $V_2$  having a value  $i = \Delta Q/T = C\Delta V/T$ . The equivalent resistance, "R", that would give the same average current is given by :

$$\text{"R"} = \Delta V/i = T/C = 1/(Cf_s).$$

## SWITCHED CAPACITOR "RESISTOR"

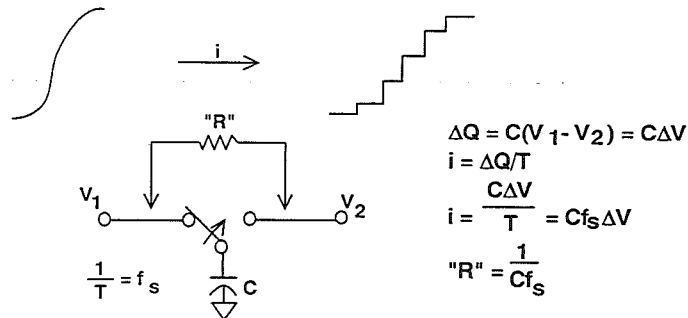


Figure 10.46

In an integrated circuit, the single-pole double-throw switch is implemented using CMOS switches driven by a non-overlapping two-phase clock as shown in Figure 10.47. A requirement for this

technique to work is that the switches have very low on resistance and very high off resistance. This is precisely what CMOS technology offers.

## CMOS IMPLEMENTATION OF SWITCHED CAPACITOR

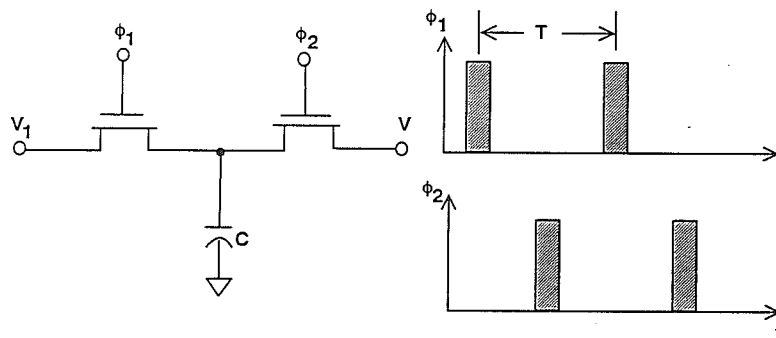


Figure 10.47

Using this SC resistor-equivalent, many conventional passive and active filter configurations can be realized. Figure 10.48 shows a single-pole passive RC filter and its SCF equivalent. The -3dB frequency of the RC filter is  $1/(2\pi R_1 C_1)$ . For the SCF version,

$$f_{3dB} = f_s C_1 / (2\pi C_2).$$

Note that for the SCF version, the bandwidth depends on the sampling

rate and the ratio of the capacitor values. A major assumption which must be made is that  $f_s \gg f_{3dB}$  (typically 50 to 100) to minimize the effects of time-sampling and charge-sharing. Using the SCF concept, critical frequencies are therefore determined by capacitor ratios and the sampling clock frequency, both of which can be made precise and drift free.

### SWITCHED CAPACITOR EQUIVALENT OF A PASSIVE RC NETWORK

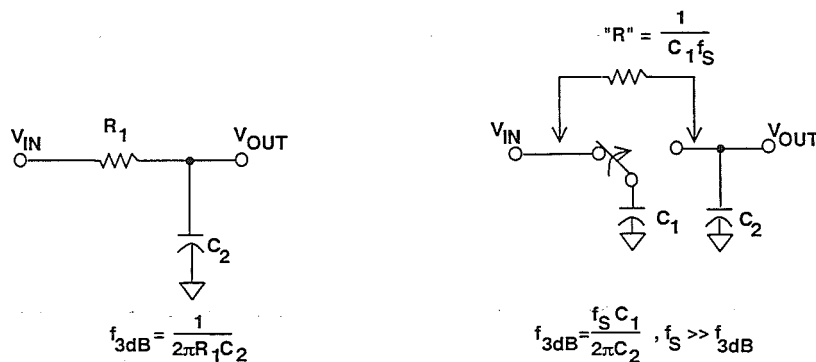


Figure 10.48

Audio and voiceband filtering with SC filters can greatly reduce passive component physical size. To implement audio filters, a resistance on the order of  $10M\Omega$  is required, if a monolithic capacitor of reasonable size ( $\sim 10pF$ ) is to be used. This value of resistance is

easily achieved by switching a  $1pF$  capacitor at a  $100kHz$  rate, requiring a silicon area of approximately  $0.01mm^2$ . If the  $10M\Omega$  resistor were implemented using polysilicon or diffusion, the area required would be at least 100 times larger.

## SWITCHED CAPACITOR FILTER ADVANTAGES

- Filter Bandwidths Proportional to Capacitance Ratios  
Not Absolute Values
- Filter Bandwidths Variable with Clock Frequency
- Defined Like Classic Analog Filters
- Low Values of Capacitance Required for Audio Frequencies:  
1pF Capacitor Switched at 100kSPS =  $10\text{M}\Omega$  "Resistance"
- SCFs Ideally Suited to DSP CMOS Processes

Figure 10.49

By using SC resistors in conjunction with other capacitors and op amps, it is possible to realize many of the circuit configurations used in conventional RC active filters. Unlike digital filters, SC

filters may be defined exactly like analog filters. A first-order continuous-time active lowpass RC filter and its SC counterpart are shown in Figure 10.50.

## FIRST ORDER ACTIVE LOWPASS RC FILTER AND SWITCHED CAPACITOR EQUIVALENT

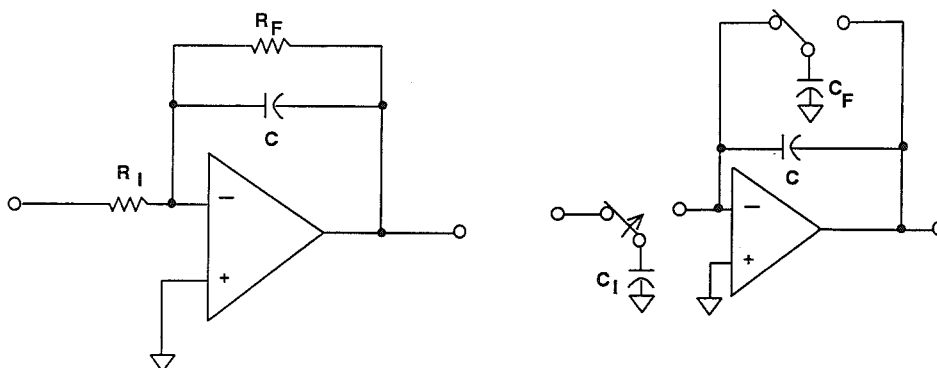


Figure 10.50

Since they sample analog signals, SC filters must usually be preceded by a continuous-time antialiasing prefilter to eliminate spectral components above the Nyquist frequency. Since the SC filter sampling rate is usually much higher than its passband, a single or double pole RC filter is usually sufficient for this purpose.

Differential amplifiers are often used in analog circuits to achieve good common mode rejection of unwanted signals

such as power line noise, etc. The same principles can be used in designing switched capacitor filters. Figure 10.51 shows an active differential integrator and its switched capacitor equivalent. In addition to providing good CMRR to noise, the differential configuration also provides common mode rejection to the transients caused by the operation of the switches. Switched capacitor integrators are often used in the modulator circuits of a Sigma-Delta ADCs as discussed in Sections 5 and 6.

### ACTIVE DIFFERENTIAL INTEGRATOR AND SWITCHED CAPACITOR EQUIVALENT

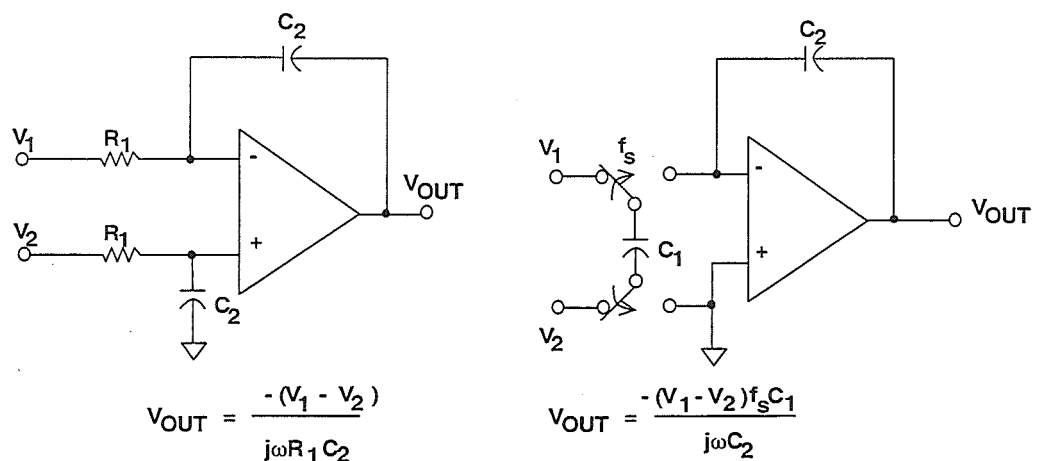


Figure 10.51

Switched capacitor filters are subject to several limitations and error sources. Their usefulness is limited to frequencies in the audio bandwidth, since sampling rates greater than a few hundred kilohertz cannot be readily achieved with current CMOS technology. The switched capacitors and op

amps introduce random noise, and leakage currents can produce offset errors. Clock feedthrough from the switches themselves can produce synchronous errors. Finally, since SCFs are sampling devices, large oversampling ratios are usually required in order to prevent errors due to aliasing.

### **SWITCHED CAPACITOR FILTER LIMITATIONS AND ERROR SOURCES**

- Limited to Lower Frequencies
- Noise, Offset, and Distortion
- Clock Feedthrough from Switches
- Must Obey the Laws of Nyquist (Requires Antialiasing Filter)

**Figure 10.52**

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## SECTION 11

### MIXED SIGNAL CIRCUIT TECHNIQUES

- Introduction
- Resistance:
  - Resistance of Conductors, Skin Effect, Voltage Drop in Signal Leads, Kelvin Feedback, Leakage in Insulators, Guard Rings, Electrostatic Damage, Parasitic Effects in Resistors, Inductance, Thermoelectric Effects, Stability and Matching, Voltage Variation of Resistance, Johnson Noise
- Capacitance:
  - Stray Capacitance, Faraday Shields, Noise, Parasitic Effects in Capacitors, Capacitor Leakage, Series/Loss Resistance, Inductance of Capacitors, Dielectric Absorption
- Inductance:
  - Stray Inductance, Mutual Inductance, Ringing, Parasitic Effects in Inductors, Quality Factor (Q)
- Grounding and Signal Routing:
  - Signal Return Currents, Ground Noise and Ground Loops, Star Grounds, Separate Analog and Digital Grounds, Ground Planes, Transmission Lines, System Grounds, Signal Routing
- Power Supplies:
  - Power Supply Noise, Switching-Mode Power Supplies

- **Electromagnetic Interference:**  
Radio Frequency Interference, Photoelectric Effects
- **Logic:**  
Fan-Out, Timing Variations, Sampling Clock Noise,  
Logic Noise
- **Problem Areas:**  
Limitations of Spice Modeling, Sockets,  
Prototyping High Performance Analog Circuitry

## SECTION 11

# MIXED SIGNAL CIRCUIT TECHNIQUES

*James Bryant*

### INTRODUCTION

There are considerably more problems involved in the successful design of Mixed Signal circuitry than mere circuit design. If we design an electronic circuit as a diagram, whether we use an old-fashioned pencil and paper or, as is the modern fashion, a computer and SPICE or some similar software, we are overlooking one of the most important factors in the design of successful hardware, namely that what we are designing is HARDware, and until it has been shown to work successfully in fact, rather than in simulation, our design is not complete.

This section of our book considers the problems which arise when reality reacts on a design which theory and modeling have shown to be satisfactory. What, in fact, has happened is that our model probably does not consider the effects of non-ideal components and of spurious or parasitic components resulting from the circuit layout which has been used. It is not, perhaps, too fanciful to describe this as the section of the book dealing with Murphy's Law.

### MURPHY'S LAW

IN ANY SET OF CIRCUMSTANCES  
THE WORST THING THAT CAN HAPPEN - WILL

- Any effect which you think can be disregarded, can't.
- Nature always sides with the hidden flaw.

Murphy's Law, though frequently expressed humorously, is not entirely a joke. It is a recognition of the complexity of physical systems and a warning against over-simplification and is

comparable with Einstein's warning that "Everything should be made as simple as possible — but no simpler" (Reference 1).

## IMPORTANT COROLLARIES TO MURPHY'S LAW

- After it has worked successfully for two weeks it will fail during the first public demonstration.
- Equipment blows to protect fuses.
- Interchangeable parts aren't.
- Fail-safes don't.

Figure 11.2

This section discusses the various physical effects which must be considered in the design of the hardware of mixed signal systems. Often such consideration will amount to a quick calculation to demonstrate that further consideration is not necessary, but

sometimes extensive analysis, or even actual experiments, will be necessary. However, the quick calculation must not be omitted, since problems are rarely obvious, and often unexpected. The effects which must be considered will include many basic laws of physics.

## BASIC LAWS INVOLVED IN THE DESIGN OF MIXED SIGNAL CIRCUITRY

- Ohm's Law
- Kirchoff's Law
- Faraday's Laws
- Lenz's Law

Figure 11.3

We therefore shall use as a section heading the major phenomenon considered in the section, but in the most general sense (for example, under "Resistance" we shall consider the non-ideal behavior of resistors, including noise, thermo- electric and inductive effects, which are not strictly issues of Ohm's Law).

When considering the effects of circuit conditions we are, of course, interested in their effects on the performance of the system as a whole. Failure to allow for this is at the root of many of the problems which this section considers. For example, a 16-bit system divides its full-scale (FS) range into 216, or 65536, which means that 1LSB in a 10V FS system is only  $153\mu\text{V}$ . If we assume that we can tolerate errors of no more than 0.5LSB, this calculation tells us that in a 16-bit system with 10V FS, we

must keep the total error to less than  $76\mu\text{V}$ , which is approximately equal to the thermoelectric voltage in a nichrome wirewound resistor with copper/nickel leads having about  $2^\circ\text{C}$  temperature difference between its ends.

Binary logic circuitry, on the other hand, has only two states, logic 0 and logic 1, and noise immunity of hundreds or thousands of millivolts. This is why circuit designers who have worked only with digital circuitry tend to overlook the sources of error which we are considering in this section of the seminar.

Figure 11.4 lists the sizes of 0.5LSB at various resolutions (the values are given for 10V fullscale, since this is a classical converter range, and where LSBs are given a mV value. A 10V FS is assumed, unless explicitly stated

otherwise - scaling to other values of FS is a trivial operation). Every analog designer should be familiar with this table, since not only does it allow the comparison of converters which are specified in different ways, but it also

indicates whether a design is reasonable or not - if noise or system errors amount to 1mV, there is little point in designing a system with more than 12-bits resolution.

## BIT SIZES FOR 10 V FULLSCALE CONVERTERS

RESOLUTION N	$2^N$	VOLTAGE (10V FS)	ppm FS	% FS	dB FS
2-bit	4	2.5 V	250,000	25	-12
4-bit	16	625 mV	62,500	6.25	-24
6-bit	64	156 mV	15,625	1.56	-36
8-bit	256	39.1 mV	3,906	0.39	-48
10-bit	1,024	9.77 mV (10 mV)	977	0.098	-60
12-bit	4,096	2.44 mV	244	0.024	-72
14-bit	16,384	610 $\mu$ V	61	0.0061	-84
16-bit	65,536	153 $\mu$ V	15	0.0015	-96
18-bit	262,144	38 $\mu$ V	4	0.0004	-108
20-bit	1,048,576	9.54 $\mu$ V (10 $\mu$ V)	1	0.0001	-120
22-bit	4,194,304	2.38 $\mu$ V	0.24	0.000024	-132
24-bit	16,777,216	596 nV*	0.06	0.000006	-144

\* 600nV is the Johnson Noise in a 10kHz BW of a 2.2k $\Omega$  Resistor @ 25°C

Remember: 10-bits and 10V FS yields an LSB of 10mV, 1000ppm, or 0.1%  
All other values may be calculated by powers of 2

Figure 11.4

# RESISTANCE

## Resistance of Conductors

Every engineer is familiar with resistors - little cylinders with wire ends - although perhaps fewer are aware of all their idiosyncrasies. Far too few engineers consider that all the wires and PC tracks with which their systems and circuits are assembled are also resistors.

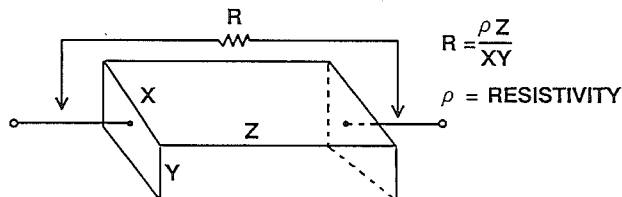
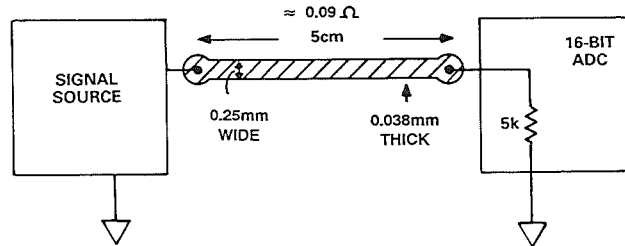
At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard (1 ounce) PCB foil is 0.038mm (0.0015"). The resistance of standard PCB copper is therefore 0.45milliohms/square, which implies a resistance for the 0.25mm track frequently used in

computer designed digital circuitry of 18 milliohms/cm, which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4% /°C around room temperature, which can be a further inconvenience.

As an illustration of the effect of PCB track resistance, consider a 16-bit ADC with a 5k ohm input resistance which has 5cm of 0.25mm PCB track between it and its signal source. This track has a resistance of approximately 0.09 ohms and introduces a gain error of 0.09 ohms / 5000 ohms (0.0018%), which is well over 1LSB (0.0015% for 16 bits).

## PRINTED CIRCUIT BOARD TRACK RESISTANCE

OHM'S LAW PREDICTS 1 LSB DROP IN  
5cm OF STANDARD PCB TRACK—  
BUT WHO BELIEVES OHM'S LAW?



FOR 1 OZ. COPPER:

$$\rho = 1.724 \times 10^{-6} \Omega \text{cm}, Y = 0.0038 \text{cm}$$

$$R = 0.45 \frac{Z}{X} \text{ m } \Omega,$$

$$\frac{Z}{X} = \text{NUMBER OF "SQUARES"}$$

$$R = \text{SHEET RESISTANCE FOR 1 SQUARE (Z = X),}$$

$$R = 0.45 \text{m}\Omega/\text{SQUARE}$$

Figure 11.5



## Skin Effect

This, of course, is a DC effect. At high frequencies, we must also consider the "skin effect", where inductive effects cause currents to flow only in the *surface* of conductors. This has the effect of increasing the resistance of a conductor at high frequencies (note that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased - that will be dealt with later). Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this seminar. However, a good approximation for copper is that the skin depth in centimeters is  $6.6/\sqrt{f}$ , ( $f$  in Hz).

Assuming that skin effects become important when the skin depth is less

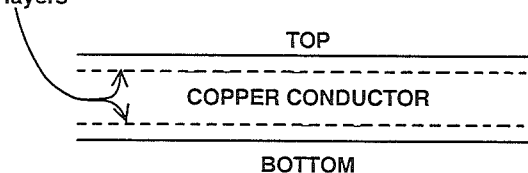
than 50% of the thickness of the conductor, this tells us that for normal 0.038mm PC foil, we must be concerned about skin effects at frequencies above approximately 12MHz.

Where skin effect is important, the resistance per square for copper is  $2.6 \times 10^{-7} \sqrt{f}$  Ohms per square, ( $f$  in Hz).

When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines), so the resistance per square of PC foil may be half the above value.

### SKIN EFFECT

- HF Current flows only in thin surface layers



- Skin Depth:  $6.61/\sqrt{f}$  cm,  $f$  in Hz
- Skin Resistance:  $2.6 \times 10^{-7} \sqrt{f}$  ohms per square,  $f$  in Hz
- Since skin currents flow in both sides of a PC track, the value of skin resistance in PCBs must take account of this

Figure 11.6

## SKIN EFFECT

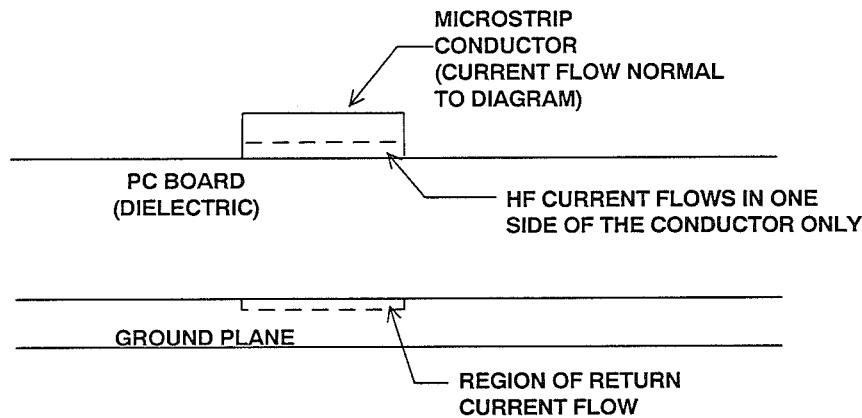


Figure 11.7

## Voltage Drop in Signal Leads - "Kelvin" Feedback

The gain error resulting from resistive voltage drop in signal leads is important only at high resolutions (as in the example), or where large signal currents flow. Where the load impedance is constant and resistive, it can be compensated by adjusting the overall system gain. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback.

Separate force and sense connections at a load remove any errors resulting from voltage drops in the force lead, but, of course, may only be used in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point.

## USE OF A SENSE CONNECTION MOVES ACCURACY TO THE LOAD

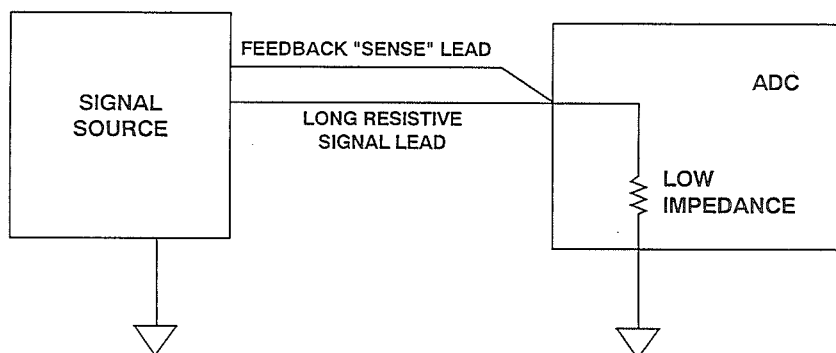


Figure 11.8

## Leakage in Insulators

Just as conductors are improperly viewed as superconductors, so are insulators often mistakenly treated as perfect insulators, rather than very high resistances, which is the more accurate model.

Most printed circuit board materials are very good insulators, but they are not perfect, and inadequately cleaned PCB material may be quite a poor insulator. Furthermore, PCBs are anisotropic - even on a clean PCB, different parts of the surface may have different resistivities, and the bulk resistance

(between two plated through holes, for instance) is generally lower than the surface resistance between two tracks.

Since the insulation resistance is so variable (and it will vary further with temperature and humidity), it is hard to predict in any particular circumstances, but it is safe to assume that it is unlikely that the resistance between two conductors on a clean PCB will drop below  $10^{10}$  -  $10^{11}$  ohms, and with Teflon PCB material (which is very expensive) will usually be over  $10^{12}$  ohms.

## Guard rings

In applications where high impedances and very low currents are involved, a guard ring may be used to minimize the effects of low insulation resistance. If critical high impedance nodes are surrounded by a ring of conductor which is at (or very close to) the potential of the node itself, then the leakage current at the node will be minimized. If the node is at, or near to, ground, then a grounded guard ring will be appropriate. If it is at some other potential it may be necessary to use a high input impedance buffer amplifier, with its

input connected to the node, to force the guard ring to the node potential. It is obvious that, in general, guard rings should be on both sides of the PCB with plated-through holes.

Nodes which are sufficiently sensitive to require guard rings should not contain plated through holes (unless the PCB is made of Teflon) because, as mentioned above, the bulk resistivity of PCB material is less than the surface resistivity.

### LEAKAGE RESISTANCE ON PC BOARDS

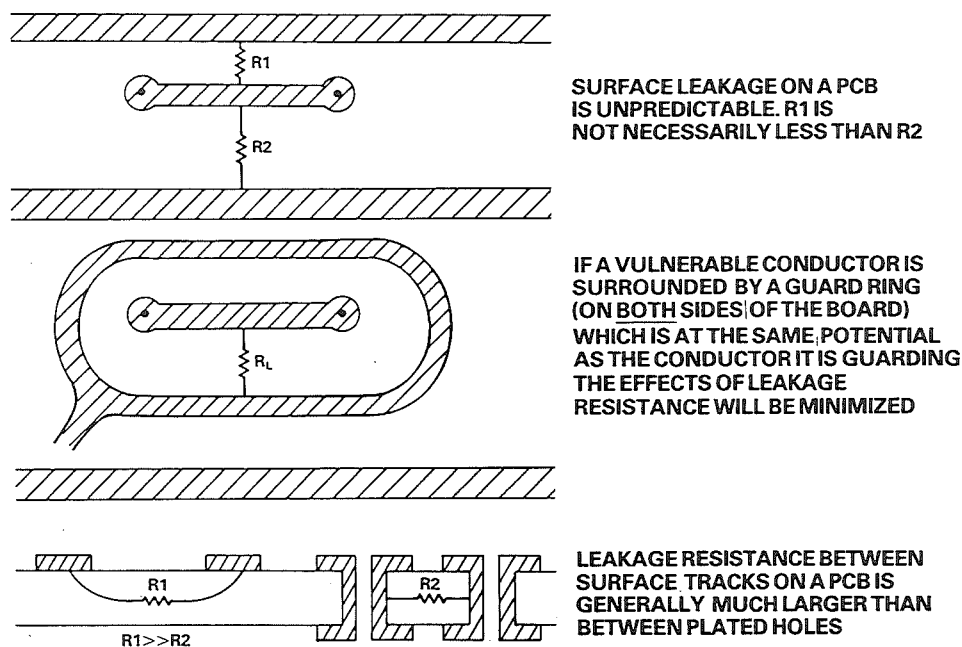


Figure 11.9

An alternative to the use of a guard ring is to use Teflon stand-off insulator(s) to support the high impedance point(s). If virgin Teflon is used, insulation resistance of around  $10^{15}$  ohms is possible ("Virgin Teflon" is a

solid piece of new Teflon material which has been machined to shape and has not been welded together from powder or grains). The material of the rest of the circuit board need not have particularly high insulation resistance.

## A VIRGIN TEFLON STANDOFF INSULATOR HAS MUCH LOWER LEAKAGE THAN A PRINTED CIRCUIT BOARD TRACK

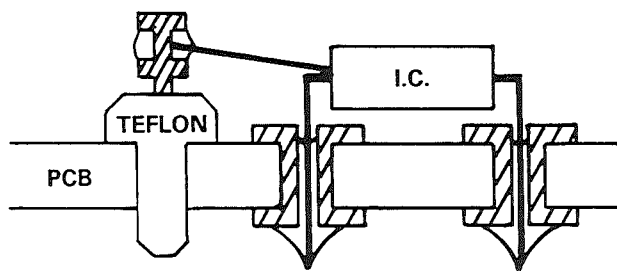


Figure 11.10

### Electrostatic damage (ESD)

Where resistances are very high, especially in conditions of low humidity, there is always the possibility of electrostatic charge and electrostatic damage. A full discussion of electrostatic damage (ESD) and its prevention will be found in Analog Devices' Application Note on the subject, which is available free of charge from Analog Devices (Reference 2).

This application note describes procedures to minimize the risk of electrostatic damage to sensitive devices. The basic principle of all ESD protection is to prevent a vulnerable item from being

in the path of a discharge. Many of the precautions used in factories are designed to minimize the possibility of any damaging discharge, even in the event of carelessness. When experienced engineers handle ICs, they may dispense with most of the ESD protection apparatus and merely ensure that the IC is never in any potential discharge path: when taking a circuit from conductive foam, touch the foam to equalize charge before touching the circuit, similarly, touch the foam with the hand before inserting the circuit in it, and hold your colleague's hand **BEFORE** passing the IC.

## ELECTROSTATIC DISCHARGE (ESD)

- All ICs are vulnerable to ESD damage
- Internal ESD protection circuits may degrade performance:  
This is a design tradeoff
- ESD damage may not be catastrophic, but may degrade performance
- Keep IC out of potential discharge paths:

Touch conductive foam before removing or inserting IC

Figure 11.11

All integrated circuit structures are vulnerable to damage from the high voltages, and high peak currents are involved in even small electrostatic discharges, but precision analog circuits suffer from a special disadvantage - the circuitry used to protect integrated circuit structures from ESD can often degrade the analog accuracy of the circuit where it is employed. Thus, we have the choice between high performance and a high degree of protection. Which we choose will depend upon individual circumstances, but it is essential to realize that the choice must be made - and if it is made in favor of accuracy, then the circuit involved must not be exposed to electrostatic discharge.

A precision analog circuit exposed to ESD may not fail totally, but merely

suffer degradation of its analog performance, and possible reduction of life expectancy. When an IC is returned to Analog Devices for failure analysis of inadequate performance, the first check that is made when the package is opened is a visual inspection for evidence of electrostatic damage - and this is found in a large percentage of cases.

An interesting example of an unobvious effect of ESD occurred in Finland, where very cold winters produce very low humidity and particularly severe electrostatic problems. A customer complained that the AD549 low bias current BiFET op-amp had poor long-term reliability, and that its noise performance deteriorated over a few years of use.

## ELECTROSTATIC DISCHARGE PROTECTION

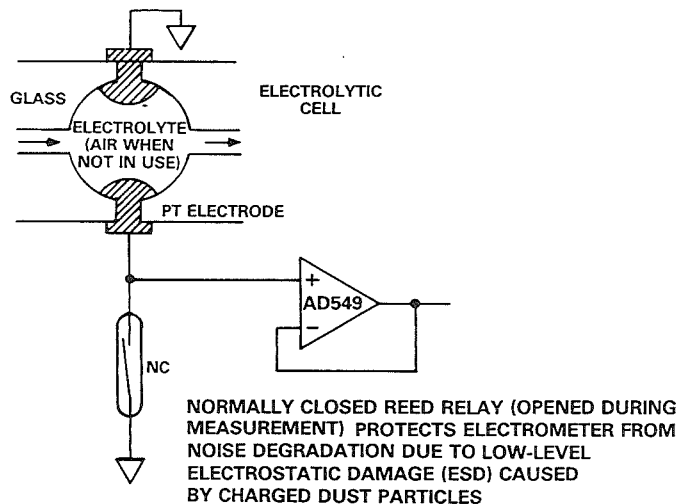


Figure 11.12

The amplifier was being used as a unity gain buffer with an electrochemical cell, and the non-inverting input was connected to a platinum electrode, and to nothing else. In use, this electrode was immersed in electrolyte, but after use, it was washed (automatically) in deionized water and air dried. It was then left unconnected until the machine was next used.

Although there was no possibility of the electrode being touched at this time (it

was in the very center of the machine), it could encounter random particles of electrostatically charged dust - and the pulse currents as these dust particles discharged were sufficient to cause gradual deterioration of the noise figure. As soon as arrangements were made to ground the electrode when it was not in use (with an NC reed relay for minimum leakage), the problem disappeared.

## Parasitic Effects in Resistors

When we model a circuit, either informally, or with a program such as SPICE, we generally assume that a resistor is a simple resistance. In fact,

any resistor is a much more complex device containing, at the very least, an inductance, a noise source, a capacitor, and two thermocouples.

### THE EQUIVALENT CIRCUIT OF A RESISTOR IS NOT



**BUT**

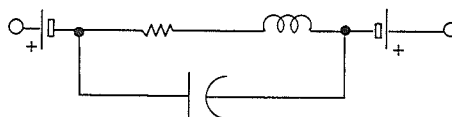


Figure 11.13

### *Inductive Resistors*

All resistors have some inductance (as we shall see, a straight piece of wire has some inductance), but wirewound resistors actually consist of a coil of wire, which must inevitably be inductive. Even if the coil is “non-inductive” and consists of  $N$  clockwise turns and  $N$  anticlockwise turns, there will still be some mismatch and residual inductance. Residual inductance values of up to  $20\mu\text{H}$  can be expected in “non-inductive” wirewound resistors with values below  $10\text{k ohms}$ , although above  $10\text{k ohms}$ , the reactance of such a resistor is more likely to be a capacitance of around  $5\text{pF}$ .

Some film resistors are also inductive, consisting of a spiral of resistive material on a cylindrical ceramic body. Again, values of a few  $\mu\text{H}$  are typical. High frequency circuits must not use inductive resistors, since their impedance is not equal to their resistance and, indeed, varies with frequency. Even low frequency circuitry, where the inductance of the resistors would not seem to be a problem, may suffer from instability arising from unforeseen HF effects of resistor inductance (the transistors used in low frequency op-amps frequently have  $F_t$  of up to  $1\text{GHz}$ ).



# Thermo-electric Effects

Wirewound resistors have another problem. The junction of the resistance wire and the lead forms a thermocouple which has a thermoelectric EMF of  $42\mu\text{V}/^\circ\text{C}$  for the standard "Alloy 180"/Nichrome junction of an ordinary wirewound resistor. If a resistor is chosen with the [more expensive] copper/nichrome junction, the value is  $2.5\mu\text{V}/^\circ\text{C}$ . ("Alloy 180" is the standard component lead alloy of 77% copper and 23% nickel.)

Such thermocouple effects are unimportant at AC, or where a resistor is at a

uniform temperature, but if the dissipation in a resistor, or its location with respect to heat sources, can cause one of its ends to be warmer than the other, then there will be a net thermoelectric EMF which will introduce a DC error into the circuit. With a normal wirewound resistor, a temperature differential of only  $4^\circ\text{C}$  will introduce a dc error of  $168\mu\text{V}$  - which is greater than 1LSB in a 10V/16-bit system.

## MINIMIZING THERMOCOUPLE EFFECTS IN WIREWOUND RESISTORS

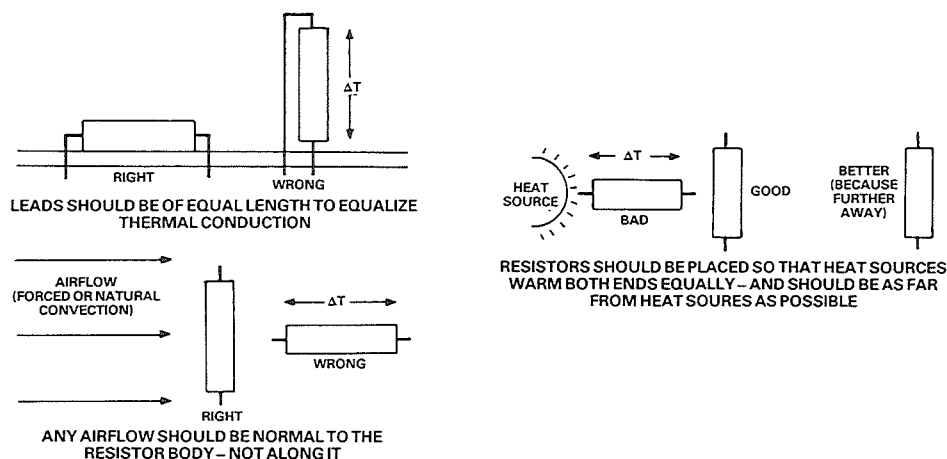


Figure 11.14

The problem may be minimized by mounting wirewound resistors to ensure that temperature differentials are minimized. This may be done by ensuring that both leads are of equal length to equalize thermal conduction through them, by making any airflow (whether forced or natural convection) normal to the resistor body, and by taking care

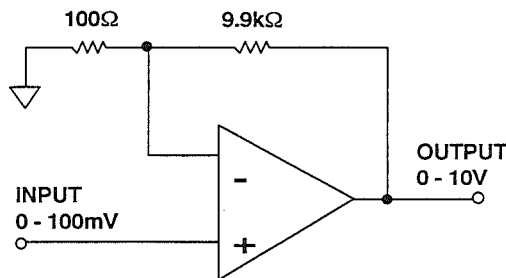
that both ends of the resistor are the same distance from any heat source on the PCB. Notwithstanding these precautions, it is wiser in circumstances where such thermoelectric EMFs may matter to use resistors with copper, rather than "Alloy 180" leads, and to site them as far as possible from any heat source.

## Stability & Matching

Thermal effects other than thermocouple effects will also affect the accuracy of circuits using resistors. Resistors are never completely stable with temperature, and if either the temperature coefficients, or the actual temperatures of two resistors in a precision circuit are

mismatched, then the performance of the circuit will suffer. Temperature mismatch of two identical resistors in similar environments may arise from differences in self-heating or other causes (Reference 3).

### GAIN OF 100 STAGE



- Resistor mismatch due to mismatch of temperature coefficients, mismatch of temperature (possibly due to self-heating), or both, can cause gain errors.
- Ideally, all resistors whose matching can affect accuracy should be fabricated on a single substrate.

Figure 11.15

Typical temperature coefficients of discrete resistors are apt to be around 100ppm/°C or more. The best way to minimize the effects of resistor temperature coefficients and to eliminate the effects of different resistor temperatures is to ensure that all resistors, whose resistor matching affects the accuracy of a system, are built on a single substrate. This substrate may be the glass or ceramic substrate of a thin film resistor network.

A better alternative, when possible, is to use an integrated circuit having laser trimmed thin film resistors on the silicon substrate of the IC. The temperature coefficient of such resistors can be well below 20ppm/°C, and the differential temperature coefficient between two resistors on the same substrate is of the order of 0.5ppm/°C or less.

### *Voltage Variation of Resistance*

It is not possible to fabricate very high resistances on thin film or IC substrates, and high value discrete resistors are considerably less stable than lower value ones. It is inadvisable, therefore, to rely on the stability of high

value resistors for the performance of a system. Some types of high value resistor have another imperfection: they have a slightly non-linear voltage/current curve and do not obey Ohm's Law accurately.

## HIGH VALUE RESISTORS

■ Likely to be Less Stable

and

■ Non-Linear with Voltage

Figure 11.16

### *Johnson Noise*

A final "imperfection" of resistors is an inconvenience, but cannot properly be regarded as an imperfection, as it is a

fundamental property of all resistors: thermal or Johnson noise.

## RESISTOR JOHNSON NOISE

- All Resistors Have Noise:  $V_n = \sqrt{4kTBR}$

T is Absolute Temperature

B is Bandwidth in Hertz

R is the Resistance in Ohms

k is Boltzmann's Constant

( $1.38\text{E-}23$  J/K)

- It is possible to reduce the noise of a resistor by reducing T, B, or R but it is NOT possible to reduce k because Boltzmann is dead.

Figure 11.17

At any temperature above absolute zero, all resistors have noise due to thermal motion of their structure. This noise, which is described by

$$V_n = \sqrt{4kTBR}$$

Where k is Boltzmann's constant:  
 $1.38\text{E-}23$  J/K.

Johnson noise is present in ALL resistors and can only be reduced by reducing R, the resistance itself, B, the bandwidth of interest, or T, the tem-

perature. Since the function involves a square root, the noise improvement for a drop in temperature from room temperature (298K) to liquid nitrogen (77K) is only of the order of 50%, so cooling a resistor, unless liquid helium is involved, is unlikely to be very profitable.

Johnson noise is purely an effect of resistance. The Johnson noise of complex impedances consists only of the Johnson noise of the resistive part of the impedance, so pure capacitance or inductance does not have Johnson noise, even though it has an impedance.

## RESISTOR COMPARISON CHART

TYPE		ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size Wide Range of Values	Poor Tolerance (5%) Poor Temperature Coefficient (1500 ppm/°C)
	Wirewound	Excellent Tolerance (0.01%) Excellent TC (1 ppm/°C) High Power	Reactance is a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100 ppm/°C) Moderate Cost Wide Range of Values Low Voltage Coefficient	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to < 1 ppm/°C) Low Reactance Low Voltage Coefficient	Low Power Very Expensive
	High Megohm	Very High Values ( $10^8$ to $10^{14}\Omega$ ) Only Choice for Some Circuits	High Voltage Coefficient (200 ppm/V) Fragile Glass Case (Needs Special Handling) Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimable Readily Available	Fair Matching (0.1%) Poor TC (>100 ppm/°C) Poor Tracking TC (10 ppm/°C)
	Thin Film	Good Matching (<0.01%) Good TC (<100 ppm/°C) Good Tracking TC (2 ppm/°C) Moderate Cost Laser-Trimable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Limited Values and Configurations

## CAPACITANCE

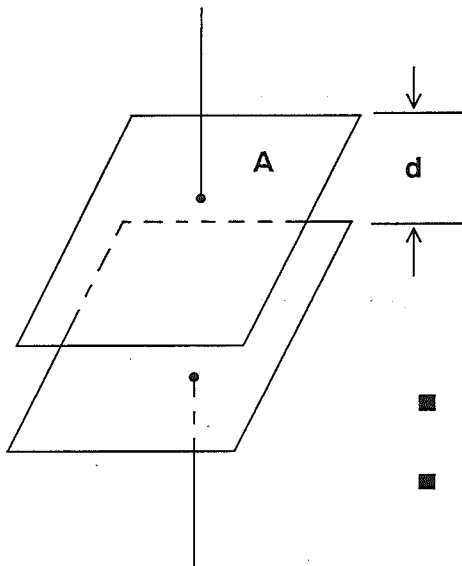
### Stray Capacitance

Where two conductors are not short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. There will therefore be a large number of capacitors associated with any circuit, which may or may not be considered in models of the circuit. Where high frequency performance matters (and even DC and VLF circuits may use devices with high  $F_t$  and therefore be vulnerable to HF instability), it is very important to consider the effects of stray capacity.

Any basic textbook will provide formulas for the capacitance of parallel wires, concentric spheres and cylinders, and many other configurations (Reference 3). The only example we need consider in this seminar is the parallel plate capacitor, which is often formed by conductors on opposite sides of a PCB.

Neglecting edge effects, the capacitance of two parallel plates of area  $A \text{ mm}^2$  and separation  $d \text{ mm}$  in a medium of dielectric constant  $E_r$  relative to air is  $0.00885 E_r A/d \text{ pF}$ .

## CAPACITANCE



$$C = \frac{0.00885 E_r A}{d} \text{ pF}$$

$A$  = plate area in  $\text{mm}^2$

$d$  = plate separation in mm

$E_r$  = dielectric constant relative to air

- Commonest type of PCB uses 1.5mm glass-fiber epoxy material with  $E_r = 4.7$
- Capacity of PC track over ground plane is roughly  $2.8\text{pF/cm}^2$

Figure 11.18

From this formula, we can calculate that for general purpose PCB material ( $E_r = 4.7$ ,  $d = 1.5\text{mm}$ ), the capacitance between conductors on opposite sides of the board is just under  $3\text{pF/cm}^2$ . In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance, but it is possible to use PCB

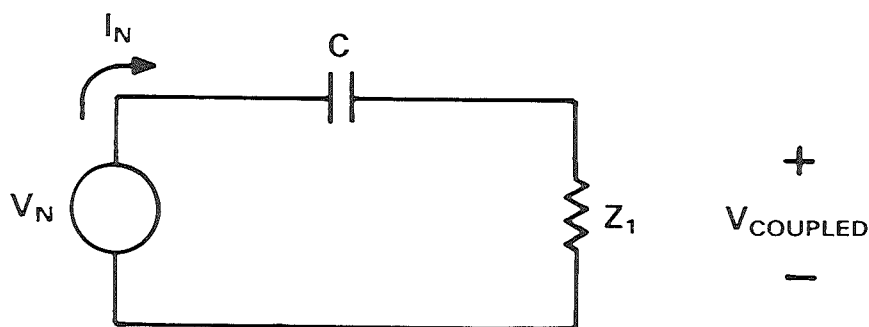
capacitance in place of small discrete capacitors. However, the dielectric properties of common PCB materials (Teflon is an expensive exception) cause such capacitors to have a rather high temperature coefficient and to have poor Q at high frequencies, which makes them unsuitable for many applications.

## Capacitive Noise & Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a

change of voltage on one, there will be a movement of charge on the other. The basic model is shown in Figure 11.19.

### CAPACITIVE COUPLING EQUIVALENT CIRCUIT



$$Z_1 = \text{CIRCUIT IMPEDANCE}$$

$$Z_2 = 1/j\omega C$$

$$V_{\text{COUPLED}} = V_N \left( \frac{Z_1}{Z_1 + Z_2} \right)$$

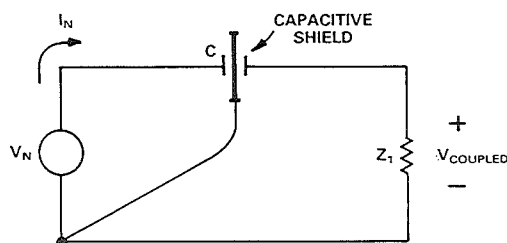
Figure 11.19

It is evident that the voltage coupled into  $Z_1$  may be reduced by reducing the signal voltage,  $V_N$ , the frequency involved, the capacitance, or  $Z_1$ , but frequently none of these can be

changed. The best solution is to insert a grounded conductor (known as a Faraday shield) between the noise source and the circuit which it affects.

## CAPACITIVE SHIELDING

## CAPACITIVE SHIELD INTERRUPTS THE COUPLING ELECTRIC FIELD



EQUIVALENT CIRCUIT ILLUSTRATES HOW A CAPACITIVE SHIELD CAUSES THE NOISE CURRENTS TO RETURN TO THEIR SOURCE WITHOUT FLOWING THROUGH  $Z_1$

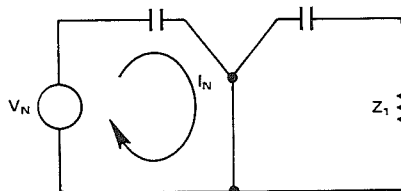


Figure 11.20

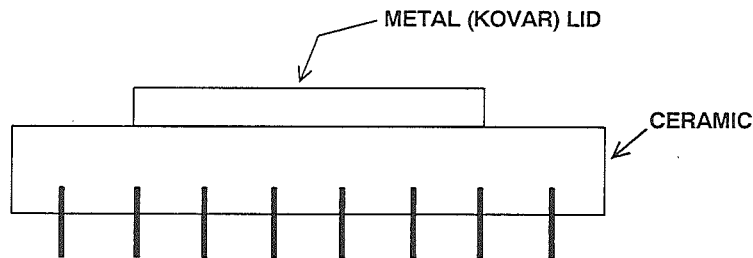
The Faraday shield is easily implemented and almost invariably successful. For this reason, capacitively coupled noise is rarely an intractable problem. However, to be effective, the shield must completely block the electric field between the noise source and the shielded circuit and must be connected so that the displacement current returns to its source without flowing in any part of the circuit where it might introduce conducted noise. A conductor intended as a Faraday shield must never be left unconnected, as this almost always increases capacity and exacerbates the problem.

An example of this problem is seen in side-brazed ceramic IC packages. These

DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected. Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Many analog circuits do not have a ground pin at a package corner, and the lid is left floating - such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.



## CAPACITIVE EFFECTS DUE TO METAL LIDS



- SIDEBRAZE CERAMIC D.I.L. PACKAGES SOMETIMES HAVE ISOLATED METAL LIDS
- THESE ARE VULNERABLE TO CAPACITIVE INTERFERENCE AND SHOULD BE GROUNDED (IF POSSIBLE)

Figure 11.21

Whatever the environmental noise level, it is good practice for the user to ground the lid of any side brazed ceramic IC where the lid is not grounded by the manufacturer - this can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip may be used to make the ground connection, or conductive paint from the

lid to the ground pin. Never attempt to ground such a lid without verifying that it is, in fact, unconnected, as occasionally device types will be found with the lid connected to a power supply rather than to ground!

One case where a Faraday shield is impracticable is between the bondwires of an integrated circuit chip. This has important consequences.

## STRAY CAPACITY BETWEEN CHIP BONDWIRES

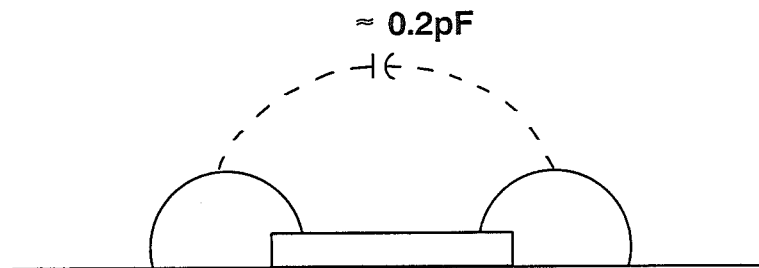


Figure 11.22

The stray capacitance between two chip bondwires and their associated leadframes is of the order of  $0.2\text{pF}$ . (Note this is “of the order” NOT “of the close order” - observed values generally lie between  $0.05$  and  $0.6\text{pF}$ .) If we have a high resolution converter (ADC or DAC) which is connected to a high speed data bus, then each line of the

data bus, which will be carrying noise with  $2\text{-}5\text{ V/ns dV/dT}$ , is connected to the converter analog port via this stray capacitance. Whenever the bus is active, intolerable amounts of noise will be capacitively coupled to the analog port, and will seriously degrade the performance of which the converter is capable.

**WITH A HIGH PERFORMANCE CONVERTER ON A  
HIGH SPEED DATA BUS, IT IS NOT POSSIBLE TO SHIELD  
THE ANALOG PORT FROM THE DIGITAL NOISE**

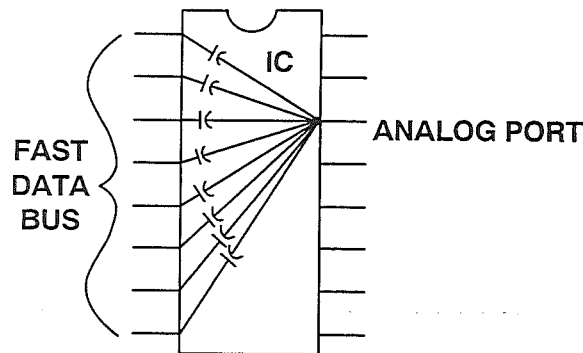


Figure 11.23

Present technology offers no cure for this problem, which also limits the performance possible from broadband monolithic mixed signal ICs having analog and digital circuitry on a single chip. However, it may be avoided quite simply by not connecting the data bus directly to the converter, but by using a

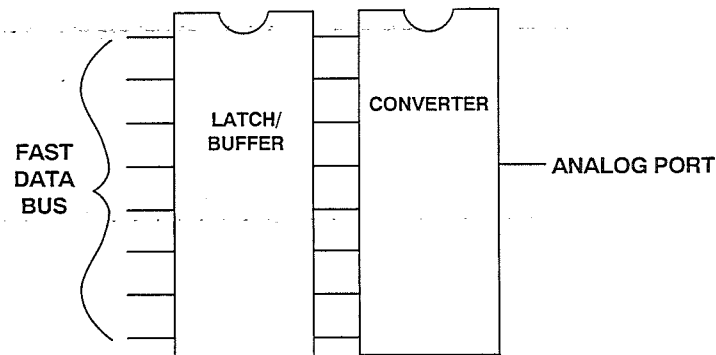
latched buffer as an interface. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power and complicates design - but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile in individual cases.

### Parasitic Effects in Capacitors

Just as we are too willing to assume that a resistor is a perfect resistor, so do we underestimate the parasitic components associated with a capacitor. Figure 11.25 shows the ideal, the gen-

eral model of a real capacitor, and the simplified models which are adequate for the analysis of non-ideal behavior in most applications.

## BUFFER LATCH USED AS A FARADAY SHIELD



- A BUFFER/LATCH CAN ACT AS A FARADAY SHIELD BETWEEN A FAST DATA BUS AND A HIGH PERFORMANCE CONVERTER.
- IT ADDS COST, BOARD AREA, POWER CONSUMPTION, RELIABILITY REDUCTION, DESIGN COMPLEXITY, AND IMPROVED PERFORMANCE.

Figure 11.24

## EQUIVALENT CIRCUITS OF A REAL CAPACITOR

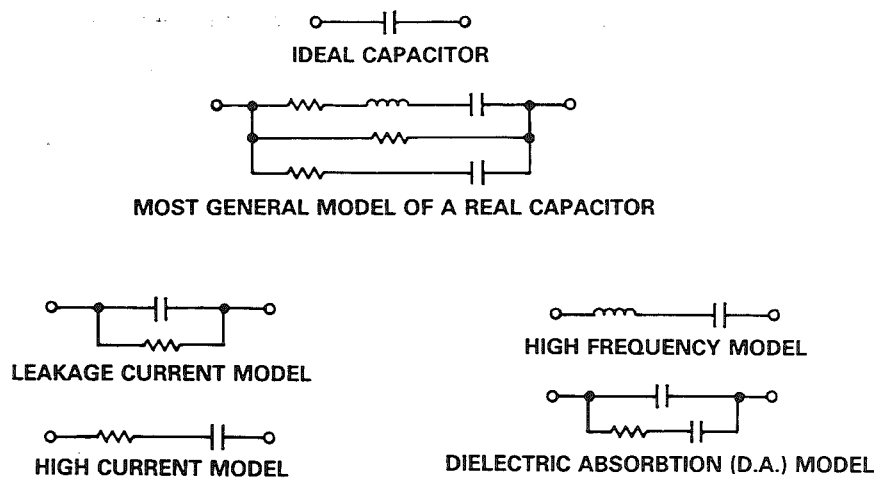


Figure 11.25

Capacitors are used for coupling (passing AC signals while blocking DC), for decoupling (removing AC superimposed on DC in both power and signal circuitry), for building filters or frequency-

### *Capacitor Leakage*

In coupling and SHA applications, the leakage of the capacitor can be important. Electrolytic capacitors, where the dielectric is formed by an electrochemical reaction, have relatively high leakage currents of microamperes or even more, and so are not used in applications where leakage matters. The leakage of electrolytic capacitors is greater during the first few minutes of operation after a period of storage (the leakage current while the capacitor is in use keeps the dielectric in good condition, and it may deteriorate slightly in storage) - this feature can be important in equipment which must perform correctly after a long quiescent period.

The leakage of tantalum electrolytic capacitors is lower than that of aluminum ones, and so in applications where capacitances of tens of microfarads or more (which can easily be achieved only with electrolytic capacitors) are re-

quired, tantalum ones are used, despite their extra cost, if particularly low values of leakage current are necessary. At room temperature, the leakage of aluminum electrolytic capacitors is of the order of  $20\text{nA}/\mu\text{F}$ , and that of tantalum ones is  $5\text{nA}/\mu\text{F}$ .

Another feature of electrolytic capacitors, both aluminum and tantalum, is that most of them are polarized and require a DC bias for correct operation - a reverse bias may do damage, and will certainly increase leakage (unpolarized electrolytic capacitors, which may be biased in either direction, do exist but they are uncommon, and considerably larger than the polarized variety).

Most other types of capacitor have leakage resistances in excess of hundreds of gigohms, so that for most applications their leakage currents can be disregarded.

### *Series/Loss Resistance*

The series resistance of capacitors causes them to dissipate power when high AC currents are flowing in them. This can have serious consequences at RF and in supply decoupling capacitors

carrying high ripple currents, but is unlikely to have much effect in precision analog circuitry. The series inductance, however, can have very inconvenient consequences.

### *Inductance of Capacitors*

The transistors used in precision analog circuits have transition frequencies ( $F_t$ ) of hundreds of MHz, or even several GHz, even though the precision circuitry itself may be operating at DC or low frequencies. This makes it essential that the power supply terminals of such circuits should be decoupled properly at high frequency.

A common structure for capacitors is two sheets of metal foil separated by sheets of plastic or paper dielectric and formed into a roll. Such a structure has considerable self inductance and behaves as an inductance rather than a capacitor at frequencies of more than a few MHz. It is therefore inadvisable to use electrolytic, paper, or plastic film capacitors for decoupling at high frequencies.

Monolithic ceramic capacitors have very low series inductance (they are formed of a multilayer sandwich of metal films and ceramic dielectric and all the films are joined to a bus-bar rather than being connected in series). They are therefore ideal for high frequency decoupling. However, monolithic ceramic capacitors can be microphonic, and some types may be self-resonant, with comparatively high  $Q$ . Disc ceramic capacitors, on the other hand, are sometime quite inductive, although less expensive.

The best way of ensuring that an analog circuit is adequately decoupled at both high and low frequencies is to use a tantalum bead capacitor in parallel with a monolithic ceramic one. The combination will have high capacitance, but will remain capacitive at VHF frequencies. It is generally unnecessary to have a tantalum capacitor on each individual IC, if there is less than 10cm of reasonably wide PC track between each IC and the tantalum capacitor, it is possible to share one tantalum capacitor among several ICs.

There is little point in taking great care in the choice of a non-inductive capacitor if it is then unsuitably mounted. Short lengths of wire have appreciable inductance, so HF decoupling capacitors must be mounted as close as possible to the points that they are decoupling with short, wide PC tracks. Ideally, HF decoupling capacitors should be surface-mount parts to eliminate lead inductance, but wire-ended capacitors are permissible, provided the device leads are no longer than 1.5mm. It is also important to understand where HF decoupling currents should flow and why HF decoupling is more important at some points than at others - the subject is covered at some length in an Analog Devices Application Note (Reference 4).

## HIGH FREQUENCY DECOUPLING (REQUIRED EVEN BY LF ANALOG CIRCUITS)

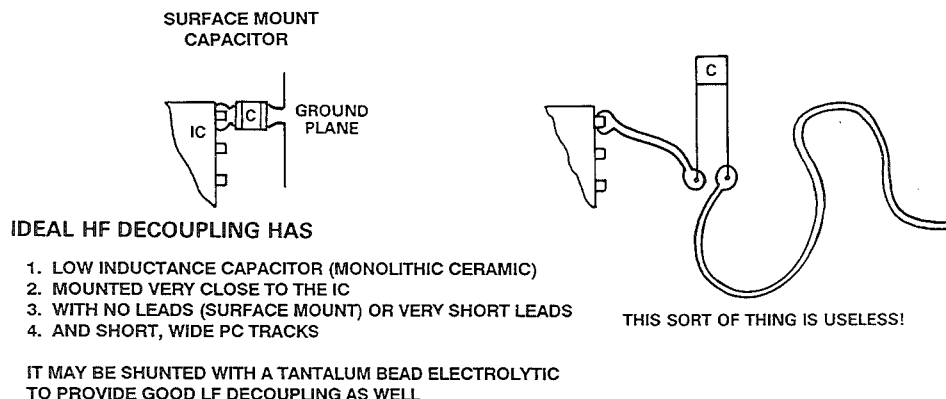


Figure 11.26

HF instability in analog circuits is more common than is realized. Oscillation at hundreds of MHz will cause serious malfunction of precision circuitry, but may not affect an oscilloscope (indeed, the presence of an oscilloscope probe may damp the oscillation, so that the circuit works only when an oscilloscope is attached to it - this is an important

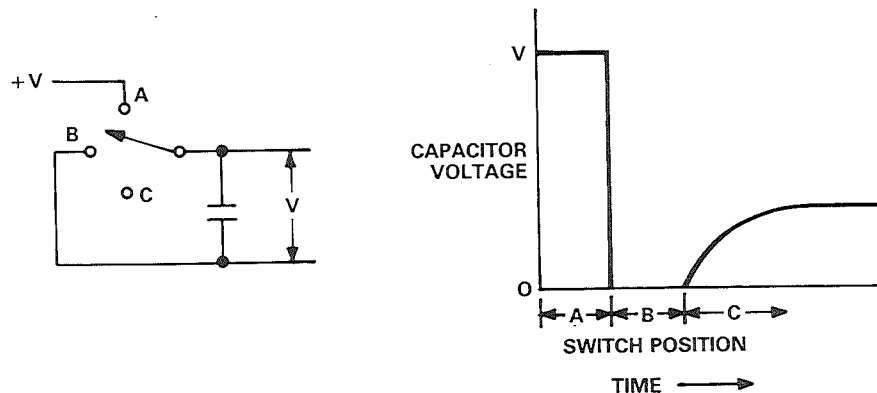
diagnostic clue). It is quite good practice to use a broadband spectrum analyzer (say 1-1500 MHz) and a low capacity FET probe to check for parasitic oscillation any analog circuit which is malfunctioning for no obvious reason. This test will also show if the malfunction is due to the presence of a strong RF field from an external source.

### *Dielectric Absorption*

Monolithic ceramic capacitors are excellent for HF decoupling, but they have considerable dielectric absorption, which makes them unsuitable for use as the hold capacitor of a SHA. Dielectric absorption causes a capacitor which is quickly discharged and then open-

circuited to recover some of its charge. Since the amount of charge recovered is a function of its previous charge, this is, in effect, a charge memory and will cause errors in any SHA where dielectric absorption is present in the hold capacitor.

## CAPACITORS HAVING SIGNIFICANT DIELECTRIC ABSORPTION ARE USELESS FOR SAMPLE-AND-HOLD APPLICATIONS



DIELECTRIC ABSORPTION CAUSES A BRIEFLY DISCHARGED CAPACITOR TO RECOVER A PERCENTAGE OF ITS PREVIOUS CHARGE ON BEING OPEN CIRCUITED.

Figure 11.27

Capacitors for this application should therefore be selected to have minimal dielectric absorption. The best strategy is to use a SHA which is supplied with an internal capacitor, or where the SHA manufacturer supplies the capacitor with the SHA. If this is not possible (sometimes one may require a longer hold time - and hence extra capacity), a capacitor should be chosen which has its low dielectric absorption (DA) specified on its data sheet.

Such capacitors are normally plastic dielectric types (polystyrene, polypropylene, or Teflon), but it is not safe to use just any plastic dielectric capacitor with a SHA, as special processing and testing is necessary to ensure that it has low DA. For use with a SHA, a capacitor should be chosen which is specified for low DA applications.



## CAPACITOR COMPARISON CHART

TYPE	TYPICAL DIELECTRIC ABSORPTION	ADVANTAGES	DISADVANTAGES
NPO Ceramic	<0.1%	Small case size Inexpensive Good stability Wide Range of Values Many Vendors Low Inductance	DA generally low, but may not be specified Limited to small values ( $\leq 10\text{nF}$ )
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values Good Stability	Damaged by Temperature $> +85^{\circ}\text{C}$ Large Case Size High Inductance
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Available Wide Range of Values	Damaged by Temperature $> +105^{\circ}\text{C}$ Large Case Size High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational above $+125^{\circ}\text{C}$ Wide Range of Values	Relatively Expensive Large High Inductance
MOS	0.01%	Good DA Small Operational above $+125^{\circ}\text{C}$ Low Inductance	Limited Availability Available only in Small Capacitance Values
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range	Large DA Limits to 8-bit Applications High Inductance
Polyester	0.3% to 0.5%	Moderate Stability Low Cost Wide Temperature Range Low Inductance (Stacked Film)	Large DA Limits to 8-bit Applications High Inductance
Monolithic Ceramic (High K)	$>0.2\%$	Low Inductance Wide Range of Values	Poor Stability Poor DA High Voltage Coefficient
Mica	$>0.003\%$	Low Loss at HF Low Inductance Very Stable Available in 1% Values or Better	Quite Large Low Values ( $<10\text{nF}$ ) Expensive
Aluminum Electrolytic	High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability Poor Accuracy Inductive
Tantalum Electrolytic	High	Small Size Large Values Medium Inductance	Quite High Leakage Usually Polarized Expensive Poor Stability Poor Accuracy

## INDUCTANCE

### Stray Inductance

All conductors are inductive, and at high frequencies, the inductance of even quite short pieces of wire may be important. The inductance of a straight wire of length  $L$  mm and circular cross-section with radius  $R$  mm in free space is given by the equation shown in Figure 11.28.

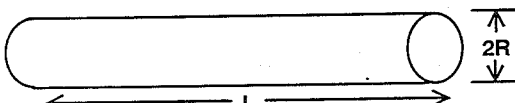
The inductance of a strip conductor (an approximation to a PC track) of width  $W$  mm and thickness  $H$  mm in free space is also given in Figure 11.28.

In real systems, these formulas both turn out to be approximate, but they do

give some idea of the order of magnitude of inductance involved. They tell us that 1cm of 0.5mm o.d. wire has an inductance of 7.26nH, and 1cm of 0.25mm PC track has an inductance of 9.59nH - these figures are reasonably close to measured results.

At 10MHz, an inductance of 7.26nH has an impedance of 0.46 ohm, and so can give rise to 1% error in a 50 ohm system.

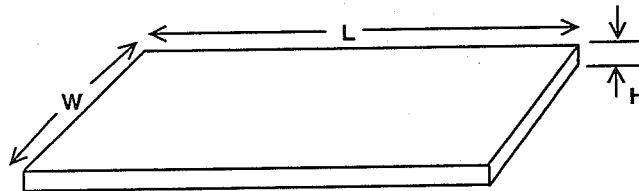
### INDUCTANCE



L, R in mm

$$\text{WIRE INDUCTANCE} = 0.0002L \left[ \ln \left( \frac{2L}{R} \right) - 0.75 \right] \mu\text{H}$$

EXAMPLE: 1cm of 0.5mm o.d. wire has an inductance of 7.26nH  
( $2R = 0.5\text{mm}$ ,  $L = 1\text{cm}$ )



$$\text{STRIP INDUCTANCE} = 0.0002L \left[ \ln \left( \frac{2L}{W+H} \right) + 0.2235 \left( \frac{W+H}{L} \right) + 0.5 \right] \mu\text{H}$$

EXAMPLE: 1cm of 0.25 mm PC track has an inductance of 9.59 nH  
( $H = 0.038\text{mm}$ ,  $W = 0.25\text{mm}$ ,  $L = 1\text{cm}$ )

Figure 11.28

## Mutual Inductance

Another consideration regarding inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in closed paths - there is always an outward and return path. The whole path forms a single-

turn inductor. If the area enclosed by the turn is large, the inductance, and hence the AC impedance, will also be large; whereas if the outward and return paths are close together, the inductance will be much smaller. The principle is illustrated in Fig 11.29.

## NONIDEAL AND IMPROVED SIGNAL ROUTING

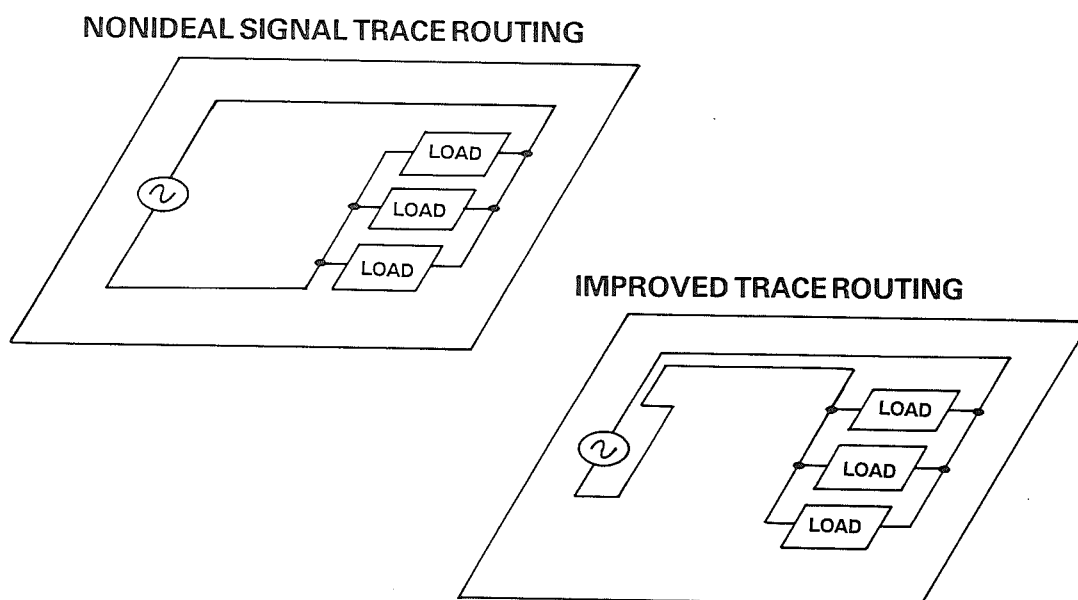


Figure 11.29

The nonideal routing in Figure 11.29 has another drawback - the large area enclosed by the conductor produces extensive external magnetic fields, which may interact with other circuits and cause unwanted coupling. Similarly, the large area is more vulnerable

to interaction with external magnetic fields, which can induce unwanted signals in the loop. The basic principle is illustrated in Figure 11.30, and is a common mechanism for the transfer of unwanted signals (noise) between circuits.

## BASIC PRINCIPLES OF INDUCTIVE COUPLING

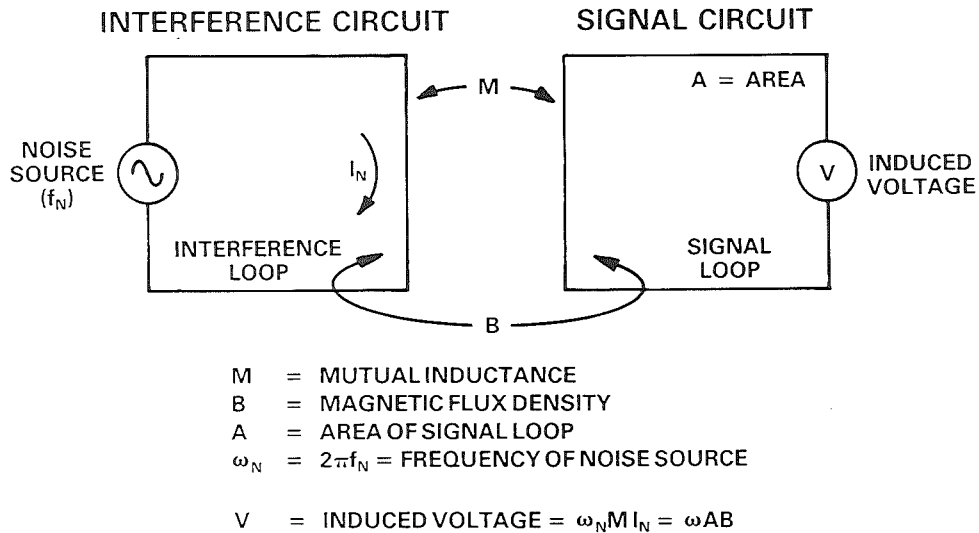


Figure 11.30

As with most other sources of noise, as soon as we define the principle at work, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 11.30 will reduce the coupling. Reducing the frequency or amplitude of the current causing the interference may be impractical, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on both sides and, possibly, increasing the distance between them.

Mutual inductance is a common problem in ribbon cables, especially when a single return is common to several signal circuits. Separate signal and return lines for each signal circuit reduces the problem, and using a cable with twisted pairs for each signal circuit is even better (but more expensive and often unnecessary).

## PROPER SIGNAL ROUTING REDUCES MUTUAL INDUCTANCE

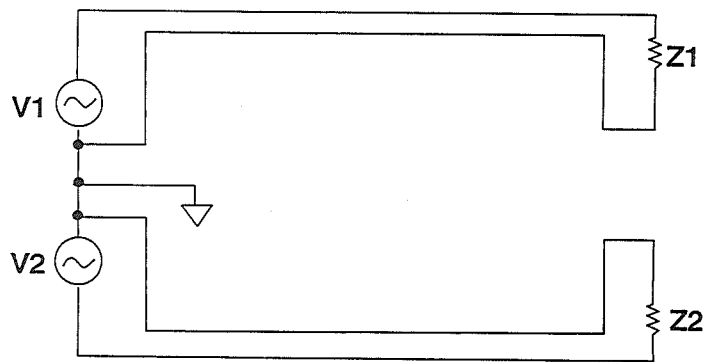
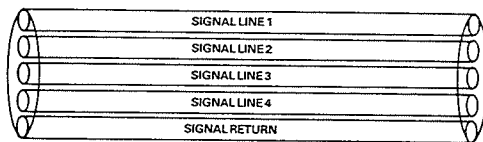
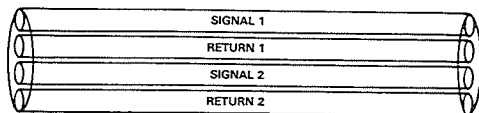


Figure 11.31

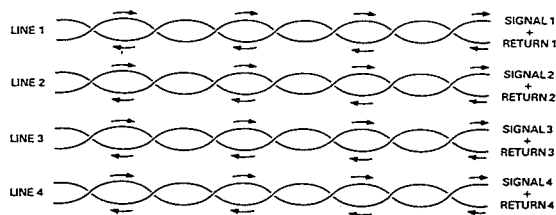
## MUTUAL INDUCTANCE AND SIGNAL COUPLING IN RIBBON CABLE



FLAT RIBBON CABLE WITH SINGLE  
RETURN HAS LARGE MUTUAL  
INDUCTANCE BETWEEN CIRCUITS



SEPARATE AND ALTERNATE SIGNAL  
AND RETURN LINES FOR EACH CIRCUIT  
REDUCE MUTUAL INDUCTANCE



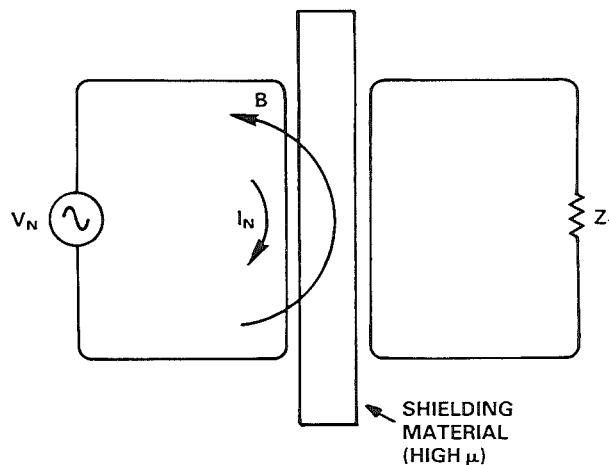
TWISTED PAIRS REDUCE MUTUAL  
INDUCTANCE STILL FURTHER

Figure 11.32

Shielding magnetic fields to reduce mutual inductance is sometimes possible, but is by no means as easy as shielding electric fields with a Faraday shield. HF magnetic fields are blocked by conductive material provided the skin depth in the conductor at the frequency to be screened is much less than the thickness of the conductor, and the screen has no holes (Faraday

shields can tolerate small holes, magnetic screens cannot). LF and DC fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

### MAGNETIC SHIELDING



- Magnetic shielding is not as easily accomplished as electrostatic shielding, but may be done at HF with a simple conducting screen, and at LF and DC with a screen of high permeability material such as Mu-metal.

Figure 11.33

### Ringings

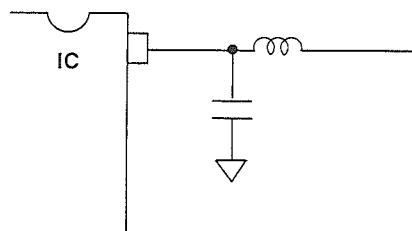
An inductor in series or parallel with a capacitor forms a resonant, or “tuned”, circuit, whose key feature is that it shows marked change in impedance over a small range of frequency (how sharp the effect is depends on the  $Q$  of the tuned circuit). The effect is widely used to define the frequency response of narrow-band circuitry, but can also be a source of problems.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit, then

that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency. A common example is shown in Figure 11.34, where the resonant circuit formed by an inductive power line and its decoupling capacitor may be excited by pulse currents drawn by the IC.

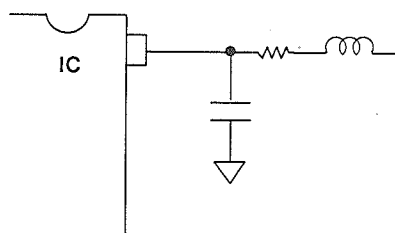
The effect may be minimized by lowering the  $Q$  of the inductance, which is most easily done by inserting a small resistance in the power line, close to the IC.

## RESONANT CIRCUITS FORMED BY DECOUPLED POWER LINES



EQUIVALENT CIRCUIT  
OF DECOUPLED POWER  
LINE - RESONANT AT

$$f = \frac{1}{2\pi\sqrt{LC}}$$



SMALL SERIES RESISTANCE  
CLOSE TO THE IC REDUCES THE Q

Figure 11.34

### *Parasitic Effects in Inductors*

Although inductance is one of the fundamental properties of an electronic circuit, inductors are less common as precision components than resistors and capacitors. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of  $\mu$ H, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are relatively rarely used in precision analog circuitry, except in

tuned circuits for high frequency narrow band applications.

Of course, they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant. The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core, its inductance will be essentially unaffected by the current it is carrying, but if it is wound on a core of a magnetic material (magnetic alloy or ferrite), its inductance will be non-linear, since at high currents, the core will start to saturate.

## SATURATION

- Inductors with solid cores (magnetic alloy or ferrite)
  - will behave non-linearly
  - if required to carry too much current.
- This is unlikely to be a direct problem in precision circuitry but may affect power supply noise performance and thus affect precision circuitry indirectly.

Figure 11.35

Such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits.

Since all inductors will have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet), and should only be used as precision inductors at frequencies well below this.



## STRAY CAPACITANCE MAKES ALL INDUCTORS INTO TUNED CIRCUITS

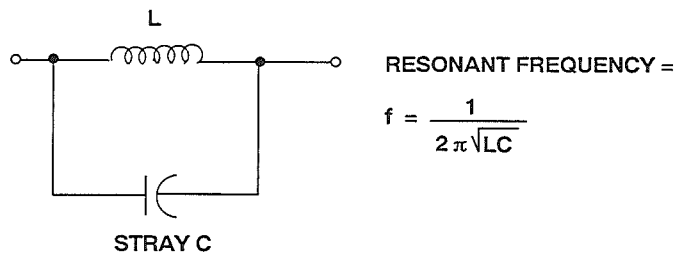


Figure 11.36

### *Q or "Quality Factor"*

The other characteristic of inductors is their *Q* (or "Quality Factor"), which is the ratio of their reactive impedance to their resistance:

$$Q = 2\pi f L / R$$

It is rarely possible to calculate the *Q* of an inductor from its DC resistance, since skin effect (and core losses if the inductor has a magnetic core) ensure that the *Q* of an inductor at high frequencies is always lower than that predicted from DC values.

*Q* is also a characteristic of tuned circuits (and of capacitors - but capaci-

tors generally have sufficiently high values of *Q* that it may be disregarded for most practical purposes). The *Q* of a tuned circuit, which is generally very similar to the *Q* of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance.

LC tuned circuits rarely have *Q* of much more than 100 (3dB bandwidth of 1%), but ceramic resonators may have *Q* of thousands, and quartz crystals have *Q* of tens of thousands.

## Q OR "QUALITY FACTOR"

- The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.

$$Q = 2\pi f L/R$$

- The resistance is the HF and NOT the DC value.
- The 3 dB bandwidth of a single tuned circuit is  $F_c/Q$  where  $F_c$  is the center frequency.

Figure 11.37

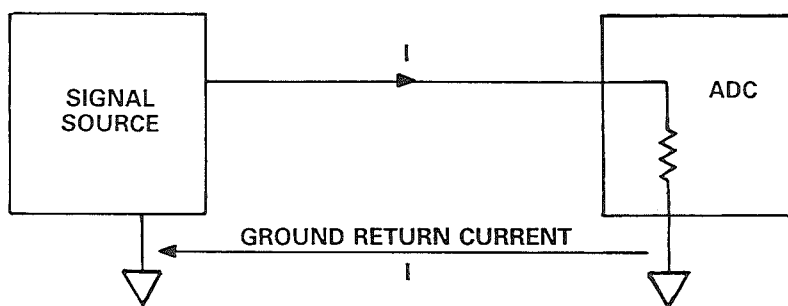
## GROUNDING AND SIGNAL ROUTING

### Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particu-

larly, that the return current must always be considered when analyzing a circuit (Reference 5).

### KIRCHOFF'S LAW



AT ANY POINT IN A CIRCUIT  
THE ALGEBRAIC SUM OF THE CURRENTS IS ZERO  
OR  
WHAT GOES OUT MUST COME BACK  
WHICH LEADS TO THE CONCLUSION THAT  
ALL VOLTAGES ARE DIFFERENTIAL  
(EVEN IF THEY'RE GROUNDED)

Figure 11.38

Most people consider the return current when considering a fully differential circuit, but when considering the more usual circuit where a signal is referred to "ground", it is common to assume

that all the points on the circuit diagram where the ground symbol is to be found are at the same potential. This is unwise.

## THE IDEAL GROUND

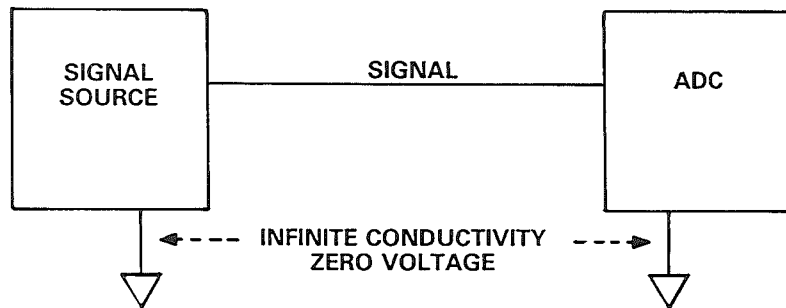


Figure 11.39

### *Ground Noise & Ground Loops*

A more realistic model of ground is shown in Figure 11.40. Not only does the return current flow in the complex impedance which exists between the two "ground" points shown in Figure 11.39, giving rise to a voltage drop in the total signal path, but external currents may also flow in the same path, generating uncorrelated noise voltages which are seen by the ADC.

It is evident, of course, that other currents can only flow in the ground

impedance if there is a current path for them. Figure 11.40 shows such a path at "ground" potential, which is the notorious "Ground Loop", but equally severe problems could be caused by a circuit sharing an unlooped ground return with the signal source, but drawing a large and varying current from its supply and ground return.

## A MORE REALISTIC GROUND

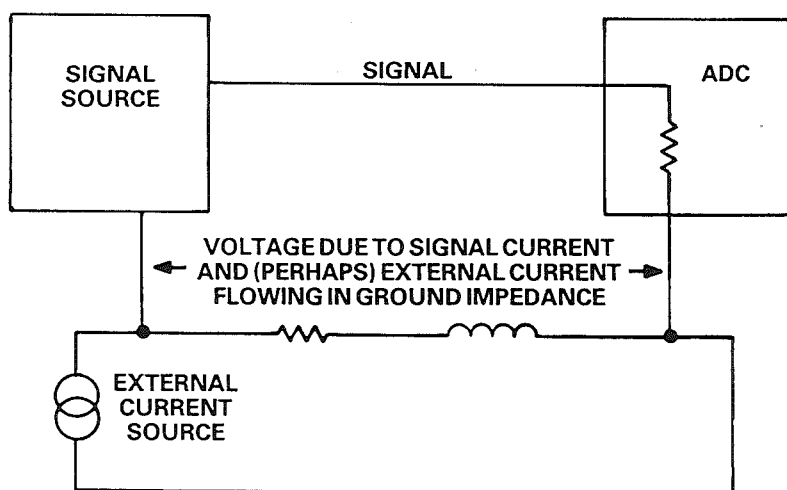


Figure 11.40

## ANY CURRENT FLOWING IN A COMMON GROUND MAKES NOISE; A GROUND LOOP IS NOT NECESSARY

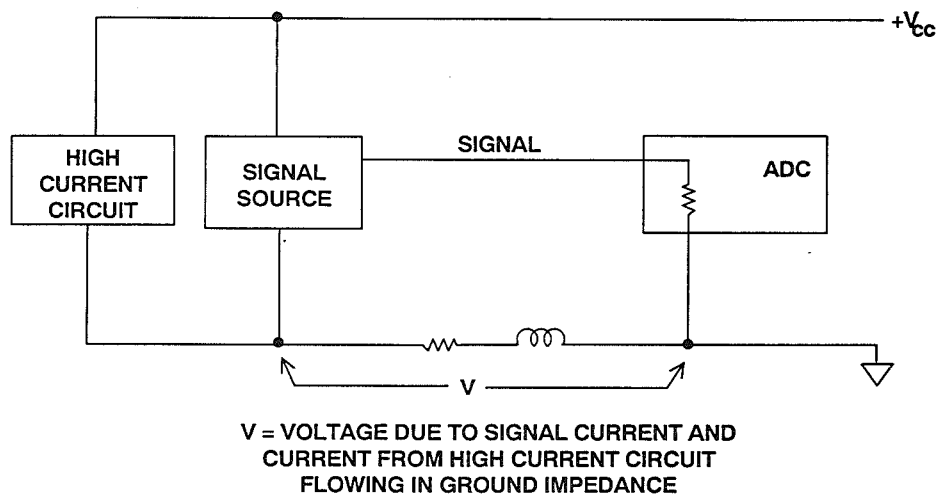


Figure 11.41

It is evident from Figure 11. 42 that if a ground network contains loops, there is a greater danger of it being vulnerable to EMFs induced by external magnetic

fields, and of ground current “escaping” from high current areas to cause noise in sensitive regions. For these reasons ground loops are best avoided.

## GROUND LOOP

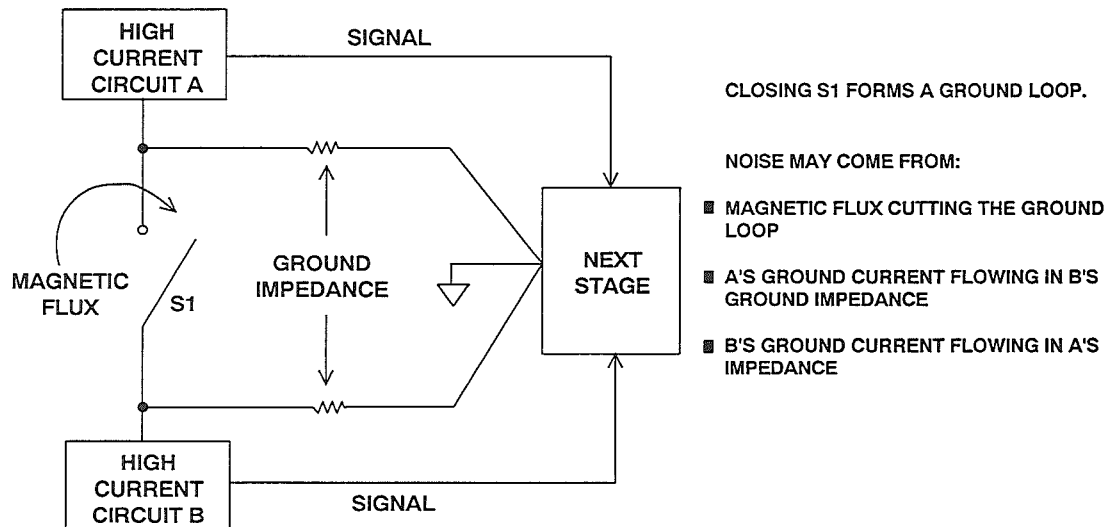


Figure 11.42

However, there are situations where looped grounds are unlikely to cause unacceptable noise, and the configuration may actually offer benefits in the form of safety or reduced impedance. In such circumstances, the optimum ground arrangement may contain loops. Sensible engineers should not allow the almost superstitious dread inspired by the term “ground loop” to prevent the adoption of such designs, if careful analysis and experiment has shown that they actually are optimum.

There are a number of possible ways of attacking the problem of ground noise, apart from the (presently) impractical one of using superconducting grounds. It is rare for a single method to be used to the exclusion of all others, and systems generally contain a mixture of approaches. For the purposes of description, however, it is better to describe each approach separately.

## *Star Grounds*

The “star” ground philosophy builds on the theory that there is a single point in a circuit to which all voltages are re-

ferred. This is known as the “star” point.

## STAR GROUNDS

■ If all signal voltages in a system are measured with respect to a single point that point is said to be the *star* ground of the system.

Figure 11.43

This philosophy is reasonable, but frequently encounters practical difficulties. For example, if we design a system with a star ground, drawing all the signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we frequently find, when the power supplies are added to the circuit diagram, that the power supplies either add unwanted ground paths or that supply currents, flowing

in existing ground paths, are sufficiently large, or noisy, or both, as to corrupt the signal transmission. This problem may often be avoided by having separate power supplies for different parts of the circuit - separate analog and digital supplies, and separate analog and digital grounds, joined at the star point, are common in mixed signal applications.

## Separate Analog and Digital Grounds

Digital circuitry is noisy. Saturating logic draws large, fast current spikes from its supply during switching and, having noise immunity of hundreds of millivolts or more, has little need of high levels of supply decoupling.

Analog circuitry, on the other hand, is very vulnerable to noise in supplies or grounds. It is therefore sensible to separate analog and digital circuitry to prevent digital noise from corrupting analog performance. Such separation will involve separation of both grounds

and power supplies, which may be inconvenient in a mixed signal system. Nevertheless, if a system is to give the full performance of which it is capable, it is often essential to have separate analog and digital grounds and power supplies. The fact that some analog circuitry will operate from a single +5V supply does NOT mean that it may safely be operated from the same noisy +5V supply as the microprocessor and dynamic RAM, the electric fan, and the solenoid jackhammer!

## SUPPLY AND GROUND NOISE

- Digital circuitry is noisy
- Analog circuitry is quiet
- Circuit noise from digital circuitry carried by power and ground leads can corrupt precision analog circuitry
- It is advisable to separate the power and ground of the digital and analog parts of a system
- Analog and digital grounds must be joined at ONE point

Figure 11.44



However, analog and digital ground in a system must be joined at some point to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system - it is often convenient to make the connection at the power supplies.

Many ADCs and DACs have separate "analog ground" and "digital ground"

pins, and users are advised, on the data sheets, to connect these pins together at the device package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

## **ANALOG AND DIGITAL GROUND**

- Monolithic and hybrid ADCs frequently have separate AGnd and DGnd pins which must be joined together at the device.
- This is not done from a desire to be difficult, but because the voltage drop in the bondwires is too large to allow the connection to be made internally.
- The best solution to the grounding problem arising from this requirement is to connect both pins to system "analog ground"
- It is likely that neither the digital noise so introduced in the system AGnd, nor the loss of digital noise immunity, will seriously affect the system performance.

**Figure 11.45**

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the parts of the converter to which the pins are connected, and not to the system grounds to which they must go. In general, these two pins should be joined together, and to the *analog* ground of the system. It is not possible to join the two pins within the IC package, because the analog part of the converter cannot tolerate the voltage resulting from the digital cur-

rent flowing in the bond wire to the chip.

If these pins are connected in this way, the digital noise immunity of the converter is diminished by the amount of common-mode noise between the digital and analog system grounds. Since digital noise immunity is of the order of hundreds or thousands of millivolts, this is unlikely to be important.

# ANALOG GROUND (AGND) AND DIGITAL GROUND (DGND) OF ADCs/DACs SHOULD BE RETURNED TO SYSTEM ANALOG GROUND

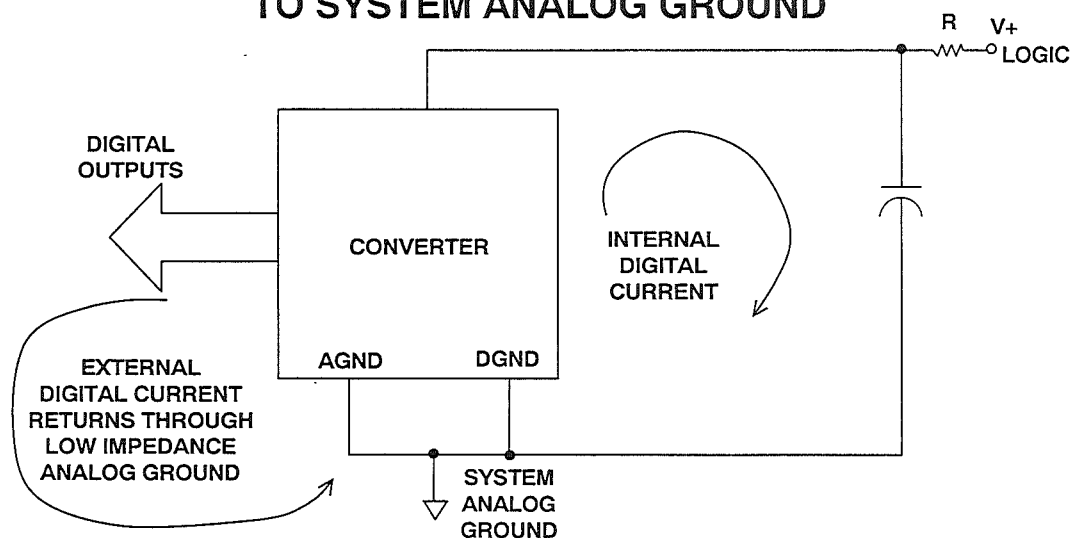


Figure 11.46

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be quite small, and can be minimized by ensuring that the converter outputs do not drive large fanouts. If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a  $0.1\mu\text{F}$  capacitor located as close

to the converter as possible, all the internal digital currents of the converter will return to ground through the capacitor and will not appear in the external ground circuit. If the analog ground impedance is as low, as it should be for adequate analog performance, the additional noise due to the external digital ground current should rarely present a problem.

## Ground planes

Related to the star ground system is the use of a ground plane. One side of a double-sided PCB, or one layer of a multi-layer one, is made of continuous metal, which is used as ground. The

theory behind this is that the large amount of metal will have low resistance and as low inductance as is possible.

## GROUND PLANES

- One entire side or layer of a PCB is continuous grounded conductor.
- This gives minimum ground resistance and inductance but is not always sufficient to solve all grounding problems.
- Breaks in ground planes can improve or degrade circuit performance--there is no general rule.
- Twenty years ago ground planes were difficult to fabricate. Today they are not.
- If your PCB facility objects to fabricating ground planes ---  
**GET A NEW PCB FACILITY!**

Figure 11.47

It is sometimes argued that ground planes should not be used because they are liable to introduce problems in manufacture and assembly. Such an argument may have had a limited validity twenty years ago when PCB adhesives were less well developed, wave-soldering less reliable, and solder resist techniques less well understood, but today it should not be tolerated.

Ground planes solve many ground impedance problems, but not all. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, they can be enough to prevent proper circuit function. Figure 11.48 shows such a problem - and a possible solution.

Consider a ground-plane PCB 100mm wide with a ground connection at one end and a power amplifier at the other drawing 15A. If the ground plane is 0.038mm thick and 15A flows in it, there will be a voltage drop of  $68\mu\text{V}/\text{mm}$ . This voltage drop would cause quite serious problems to any ground-referenced precision circuitry sharing the PCB. However, if we slit the ground plane so that high current does not flow in the region of the precision circuitry, we can possibly solve the problem - even though the voltage gradient will increase in those parts of the ground plane where the current does flow.

## A SLIT IN THE GROUND PLANE CAN RECONFIGURE CURRENT FLOW FOR BETTER ACCURACY

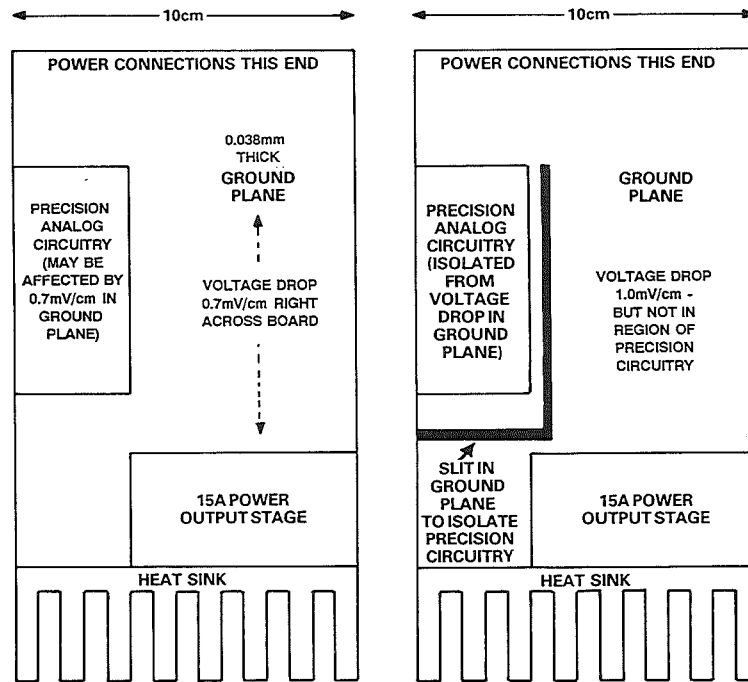


Figure 11.48

### Transmission Lines

A break in a ground plane is not always a good thing. We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As we saw in Figure 11.47, when an HF signal flows in a PC track running over a ground plane, the arrangement functions as a microstrip transmission line, and the majority of the return current flows in the ground plane underneath the line.

The characteristic impedance of the line will depend upon the width of the track

and the thickness and dielectric constant of the PCB material. For most lower frequency applications, the characteristic impedance will be unimportant, as the line will not be correctly terminated, but at UHF and higher it is possible to use PCB tracks as microstrip transmission lines in properly terminated systems. If losses in such systems are to be minimized, the PCB material must be chosen for low high frequency loss. This usually means the use of expensive Teflon PCB material.

## MICROSTRIP TRANSMISSION LINE

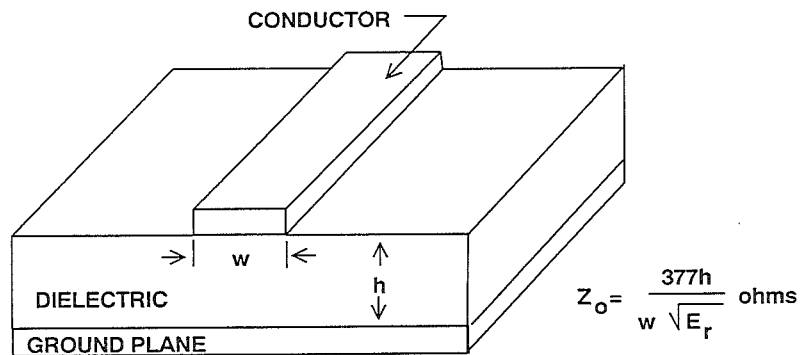


Figure 11.49

Where there is a break in the ground plane under a conductor, the return current must flow around the break,

and both the inductance and the vulnerability of the circuit to external fields are increased.

## BREAKS IN GROUND PLANE RAISE INDUCTANCE

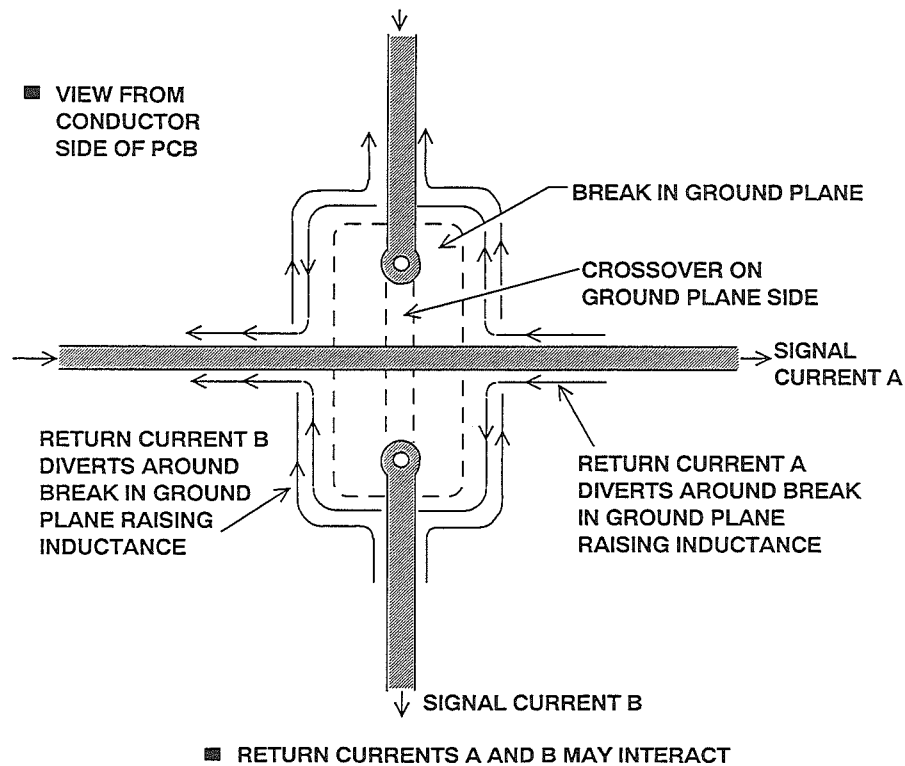


Figure 11.50

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multi-layer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multi-layer PCBs are expensive and harder to troubleshoot than simple double-sided boards,

but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

Use of double-sided or multi-layer board with at least one continuous ground plane is undoubtedly one of the most successful approaches to the design of high performance mixed signal circuitry. Often the impedance of the ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system, but this does depend upon the resolution and bandwidth required, and the amount of digital noise in the system.

### *System Grounds*

In systems where there are several PCBs, grounding may be more of a problem. At first sight, it would appear that the problem is similar to that of a single PCB, where particular sub-systems must be positioned so that large ground currents do not flow where ground noise must be minimized - in a multicard system, the grounds of individual PCBs must be interconnected so that such harmful interactions are minimized.

There are three problems with this. First of all there is far less opportunity for rearranging the physical layout of a system consisting of a few cards connected to a common backplane. Secondly, many multicard systems are designed to be reconfigured in a "mix 'n' match" arrangement to allow large numbers of system options - it can be impossible to predict what systems are

going to be required and to ensure that all of them are noise free. Finally, multicard systems are likely to have higher ground currents than occur on single, relatively simple, PCBs - but these currents must flow in the higher impedances which are associated with the intercard connectors, even when multiple ground pins are used.

The basic principles still apply: ground impedance must be as low as possible, high level and low level signals must be separated so that they do not interfere with each other, and capacitance and mutual inductance coupling must be avoided. Nevertheless, it must be accepted that situations can arise where it is not possible to transfer a high speed, high accuracy signal from one PCB to another without unacceptable signal degradation.

## MULTIPLE CARD SYSTEMS

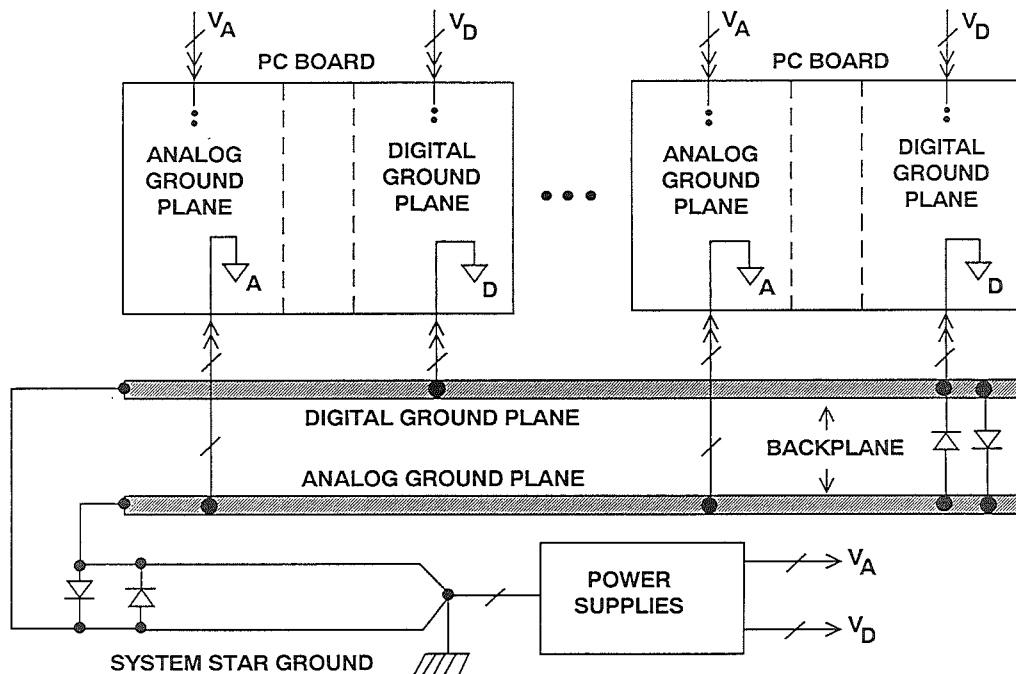
- Multiple card systems are likely to have higher ground currents and higher ground impedances than are found on a single PCB.
- It is therefore more difficult to transfer ground-referenced signals accurately between cards than across a PCB.
- In some cases it will be IMPOSSIBLE to transfer ground-referenced signals between PCBs without unacceptable loss of quality.

Figure 11.51

The best way of minimizing ground impedance in a multocard system is to use another PCB as a backplane and have a ground plane (or even two - one analog, one digital) on that mother card. If the earlier advice about multiple ground pins has been observed, this arrangement is capable of excellent performance. Where there are several card cages (racks for PCBs), the ground planes of the several mother boards must be tied together and, probably, to the metal chassis holding the card cages - the exact layout of the interconnections will depend on the overall system architecture.

If a mother board with a ground plane is not possible, then the ground pins of the PCB sockets must be wired together, with due attention to probable current flows and common ground impedances, with heavy, multi-strand wire, having as low resistance as possible. In many cases, the resulting ground screen will be tied to chassis ground at a number of points, but it will sometimes be better to join them at a single star point.

## SEPARATING ANALOG AND DIGITAL GROUNDS IN A MULTIPLE, STAR GROUND SYSTEM



**Figure 11.52**

It is not just the ground layout that is important in high performance mixed signal systems, the location of different

## Signal Routing

It is evident that we can minimize noise by paying attention to the system layout and preventing different signals from interfering with each other. High level analog signals should be separated from low level analog signals, and both should be kept away from digital signals. We have seen elsewhere that in

subsystems and the routing of signals is most important in determining overall system performance.

waveform sampling and reconstruction systems, the sampling clock (which is a digital signal), is as vulnerable to noise as any analog signal, but is as liable to cause noise as any digital signal, and so must be kept isolated from both analog and digital systems.



## SIGNAL ROUTING IN MIXED SIGNAL SYSTEMS

- Physically separate analog and digital signals.
- Avoid crossovers between analog and digital signals.
- Be careful with sampling clock and ADC analog input runs.
- Be careful with high impedance points.
- Use lots of ground plane.
- Use microstrip techniques for controlled impedances.

Figure 11.53

## A PC BOARD LAYOUT SHOWING GOOD SIGNAL ROUTING

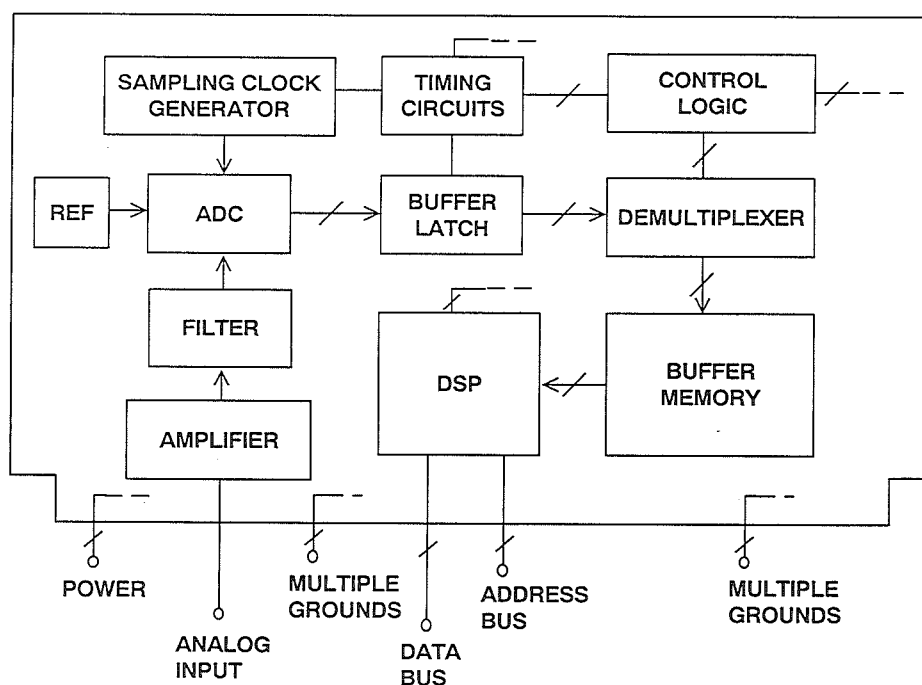


Figure 11.54

If a ground plane is used, as it should in be most cases, it can act as a shield where sensitive signals cross. Figure 11.54 shows a good layout for a data acquisition system where all sensitive areas are isolated from each other, and signal paths are kept as short as possible. While real life is rarely as tidy as this, the principle remains a valid one.

There are a number of important points to be considered when making signal and power connections. First of all, a connector is one of the few places in the system where all signal conductors must run parallel - it is therefore a good idea to separate them with ground pins to reduce coupling between them.

## **EDGE CONNECTIONS**

- Separate sensitive signals by ground pins.
- Keep down ground impedance with multiple (20-30% of total) ground pins.
- Have several pins for each power line.
- Critical signals may require a separate connector (possibly coax).

**Figure 11.55**

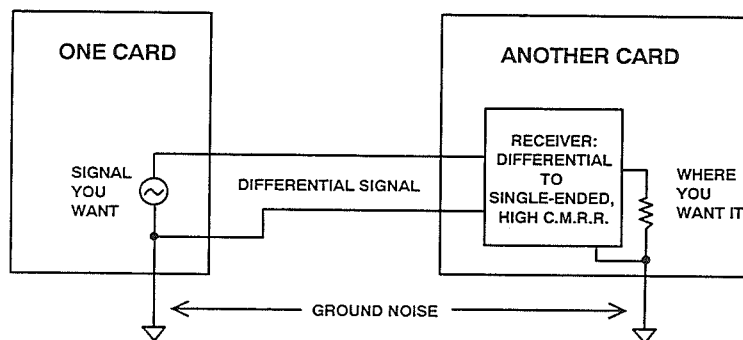
Multiple ground pins are important for another reason: they keep down the ground impedance at the junction between the board and the backplane. The contact resistance of a single pin of a PCB connector is quite low (of the order of 10 mOhms) when the board is new - as the board gets older, the contact resistance is likely to rise, and the board's performance may be compro-

mised. It is therefore well worthwhile to afford extra PCB connector pins so that there are many ground connections (perhaps 20-30% of all the pins on the PCB connector should be ground pins). For similar reasons, there should be several pins for each power connection, although there is no need to have as many as there are ground pins.

Modern high performance mixed signal systems handle signals with resolutions of 8 bits at sampling rates of over 500MHz and resolutions of 14 bits sampled at more than 10MHz. Preserv-

ing signal integrity between cards in a multi-card system is extremely difficult at such performance levels, and may be impossible.

### DIFFERENTIAL TRANSMISSION MINIMIZES GROUND ERRORS



- At DC and LF the receiver will be an instrumentation amplifier
- At HF the receiver will be a transformer
- There is no ideal receiver for video signals which have components from DC to HF

Figure 11.56

The use of balanced transmission lines can help, but if the signal bandwidth extends to DC, there will be a need for a very high performance instrumentation amplifier at the receiving end to restore a ground referenced signal.

The best, and in many cases the only, solution to problems of this sort, is to partition the system so that the highest quality signals are not transferred between boards.

## VIDEO SIGNAL TRANSMISSION

- It is often IMPOSSIBLE to transmit very broadband high accuracy signals between PCBs of a multcard system without unacceptable loss of quality.
- In such cases the system must be reconfigured to allow all the analog processing to take place on a single PCB.
- It may be inconvenient, but it's the only way you'll get it to work!

Figure 11.57

## POWER SUPPLIES

When we design an electronic circuit, we generally assume that the power supplies provide noise-free power, at exactly the nominal voltage, with zero source impedance at all frequencies. This is rarely the case.

We also assume that the published power supply rejection figures (PSRR) for the devices which we use are valid at all frequencies from DC to light. This is rarely the case either.

## POWER SUPPLY NOISE

- Long-term variation  
(Long-term variations in voltage or AC line voltage)
- AC Line noise  
(Both 100/120 Hz ripple on rectifier output and transient noise on the AC line which passes to the DC output)
- Switching Noise  
(Digital noise from switching-mode power supplies)
- Power line noise transfer  
(Unwanted signals which pass from one part of a circuit to another via the common power supply)

Figure 11.58

### *Power Supply Noise*

Every power supply is noisy. This noise may contain long-term voltage drift, line ripple at 100 or 120Hz, high frequency spikes from switching regulators, or all of these at once. Power supplies also have finite output impedance, so that if a circuit draws a varying current, the supply voltage will vary with the current - if two circuits are supplied from a common supply, this provides a mechanism whereby one circuit may affect the other. Once we appreciate all these effects, we can attempt to quantify them, and take steps to minimize their adverse effects on our systems.

Long-term supply voltage changes, whether due to battery voltage drop during life or line voltage variations, are rarely a problem since where such variations might cause difficulties, the

system will incorporate a supply voltage regulator to keep variations within acceptable limits. Similarly, ripple at twice the AC line frequency, and any spikes or HF noise which may enter the system via the AC supply, should not cause degradation of performance in a well-designed system: if the decoupling capacitors in the rectifier circuitry do not adequately minimize the effect, the series regulator almost certainly will. It is, however, always worthwhile to have a surge eliminator on the AC line input to any system - while such a circuit is unlikely to be needed in preventing normal line noise from corrupting system performance, it is essential to prevent occasional large surges (from lightning or similar causes) from doing actual damage to the power supply or the system that it is powering.

## Switching-Mode Power Supplies

The most common type of power supply noise is switching noise. Switching power supplies are small, cheap, efficient and, in too many cases, extremely noisy! Not only do they generate con-

ducted noise, they are also efficient producers of capacitively coupled noise, magnetically coupled noise, and electro-magnetically coupled noise. The best possible advice is not to use them.

### SWITCHING-MODE POWER SUPPLIES

- Generate every imaginable type of noise and some inconceivable ones as well
- DO NOT USE THEM WHERE NOISE IS IMPORTANT
- If their use is unavoidable do not relax and enjoy it, but take extreme precautions against all forms of noise
- Remember that a manufacturer's design change in a bought-in switching mode power supply may alter its effects on your system noise without altering its published specification.
- When developing a system using a switching mode supply it is instructive and often frightening to temporarily replace the switching supply with a battery or a linear supply and to remeasure the system noise!

Figure 11.59

It is, unfortunately, not always possible to avoid the use of switching power supplies. Where they must be, used they must be treated with the gravest suspicion, and all possible precautions should be taken to prevent their noise from corrupting the analog circuits that they power. Their input and output lines should be decoupled at all frequencies, they should be shielded to prevent external electric and magnetic fields from causing interference, and they should be located as far as possible from sensitive circuits so that residual electric and magnetic fields are prevented by distance from doing serious damage.

Where switching supplies are used, it is always worthwhile to remove them temporarily and supply the system with batteries or a low noise bench supply, in order to determine if the system performance is being compromised by the switching supply. It often is.

The noise transients on the output lines of switching supplies consist of voltage spikes of very short duration. As we have pointed out above, large capacitors, such as electrolytic or plastic film types, have quite considerable inductance and too high an impedance at HF to decouple such spikes satisfactorily.

The best output filter for a switching supply will have high value capacitors to remove the low frequency noise which will also be present, and a pi filter using ceramic capacitors, with short leads having low impedance at

HF, plus a series inductor (which may be a ferrite bead on the output line), to provide inductive blocking of the spikes. It is possible to buy such a pi filter as a single bulkhead mounted feedthrough component.

## **Electromagnetic Interference**

### **Radio Frequency Interference**

Noise can enter a circuit as electromagnetic radiation. Circuits can also generate electromagnetic radiation which can interfere with electronic devices at quite considerable distances away. Recent legislation in the United States, the European Community, and many other countries sets limits on the amount of interference generated and the vulnerability of circuits to such interference (Reference 6).

This legislation, and the techniques needed to comply with it, are the subjects of many seminars and training courses, and an Analog Devices Application Note (Reference 7). It is not proposed to cover the topics in detail in this seminar.

## **ELECTROMAGNETIC NOISE GENERATION**

- Circuits must be designed so that external E/M fields are minimized.
- This is done by shielding, decoupling, minimizing the area of HF current loops, and designing circuits which generate as little EMI as possible.
- IT'S NOT JUST A GOOD IDEA
- IT'S THE LAW!!

**Figure 11.60**

However, the principles of minimizing external radiation are closely related to the principles of low noise design which we have already discussed: high frequency and high  $dV/dT$  signals should be screened with Faraday shields, the area of current loops should be minimized, conductors should be decoupled at HF wherever unnecessary HF signals might otherwise occur, and external wires should be isolated with inductors or ferrite beads.

It is still too common to encounter skepticism about the need to protect

circuitry from external electromagnetic fields. Even twenty years ago, such skepticism was unjustified, but today, when transmitters are ubiquitous, it is folly. Besides the more obvious broadcast, emergency, and mobile radio services, there are cellular and cordless telephones, radar, garage door openers, and other remote controls, telemetry, and amateur and CB radio. For any designer to imagine that his circuit will never encounter a radio transmitter during its lifetime is folly on a grand scale.

## **ELECTROMAGNETIC NOISE INTERFERENCE**

- The world is full of radio transmitters.
- Police, taxis, broadcast, amateur, CB, cellular and cordless telephones, telemetry, and garage door openers.
- Do not imagine that your circuit will never encounter one!

**Figure 11.61**

This is particularly so because the design of circuits which are immune to electromagnetic radiation of reasonable levels is not particularly difficult. If

every conductor which leaves a PCB can be decoupled with a ceramic capacitor and a ferrite bead, it is probable that no further precaution is necessary.



## EMI PREVENTION

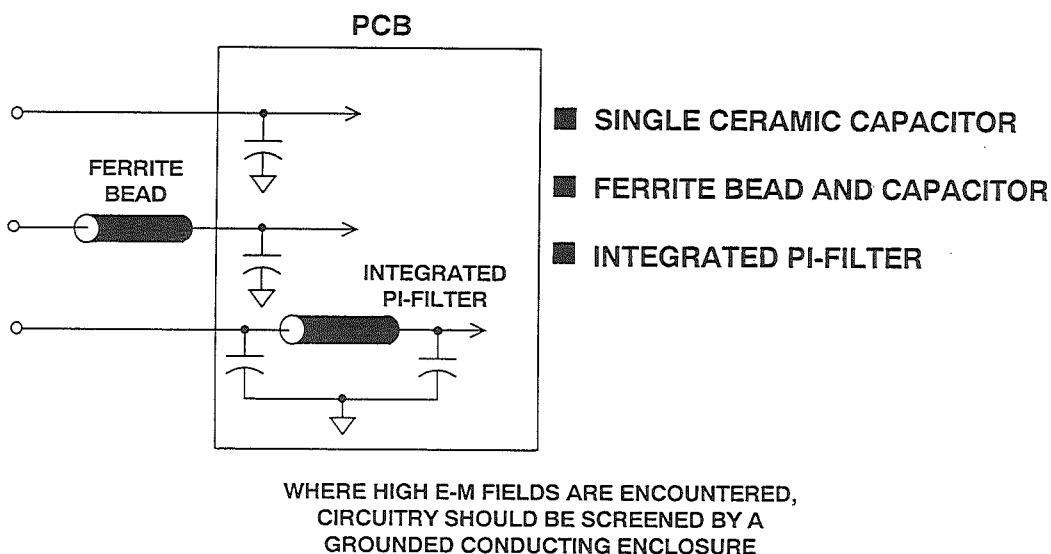


Figure 11.62

A few ports may be more vulnerable and require a pi filter rather than an L filter, and, of course, ports where an HF signal must actually enter or leave the board must be filtered to suppress other EMI, but allow the signal to pass unaffected.

Boards which may be required to work in areas of high RF field should be screened with a conducting Faraday shield.

### *Photoelectric Effects*

Light is also a form of electromagnetic radiation and can affect semiconductor devices. Every silicon P-N junction is a photodiode, although their efficiencies vary widely. Wherever devices are not screened from ambient light, photoelectric effects may be observed.

(EPROMs are an exception, and it is possible to measure threshold changes in EPROMs as light intensity is varied, but since they are digital devices, and remain in specification despite light level changes, the effect is unimportant).

Nearly all integrated circuits are encapsulated in light-tight packages

Diodes, on the other hand, are frequently encapsulated in translucent

glass packages. When illuminated by light from fluorescent lamps, modulated at 120 or 100Hz, they can act as a source of hum.

When the signal source of an op-amp contains an energizing voltage which is much higher than the op-amp supply, it is common to use a diode and a current limiting resistor to protect the op-amp in the event of a sensor short-circuit. In normal operation, the diode is reverse

biased and contributes only its (low) leakage current to the circuit, but should the sensor be short-circuited, the resulting current will flow through the diode to the op-amp supply, rather than destroy the op-amp. It is, of course, important to choose the resistor so that it neither degrades the noise performance of the system nor allows too much current to pass under fault conditions.

### PHOTOCURRENT IN GLASS DIODES CAN CAUSE HUM IN AMPLIFIERS

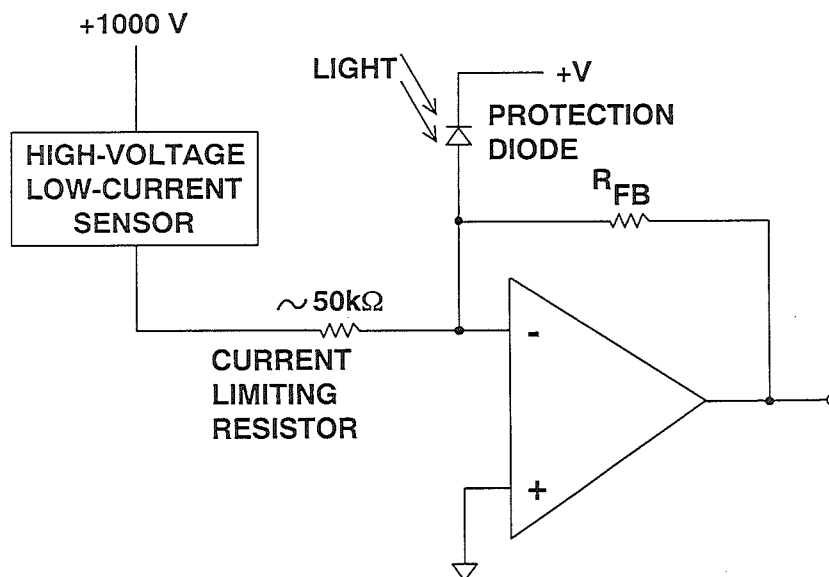


Figure 11.63

The European Applications Department of Analog Devices encountered such a system where about 10% of all the amplifiers built suffered from severe hum at twice the power line frequency. The customer, of course, blamed the op-amp for poor supply rejection, but analysis showed that even when the circuit was powered from batteries, the problem persisted. The cause eventually turned out to be fluorescent lighting affecting the protective diode - a 1N914 in a glass case.

About 10% of diodes from the particular manufacturer were quite active as photodiodes, and when illuminated by fluorescent lights, their leakage current was modulated at 100Hz (this was a European problem) - and the 100Hz was, of course, amplified with the sensor signal. Use of a black epoxy packaged diode provided a complete cure.

## LOGIC

The majority of this section of our seminar has considered problems within the analog parts of mixed signal systems. Despite their much greater noise immunity, the digital parts of these systems can also suffer from designers' lack of consideration of basic laws. Common problem areas include bus interface issues, including fan-out and

timing, for both converters and DSP processors, the care and feeding of sampling clocks, and the design of systems which generate minimum noise (we have already discussed how to keep logic noise from affecting the analog parts of a system - this task becomes easier if the logic noise is minimized in the first place).

### DIGITAL PROBLEM AREAS IN MIXED SIGNAL SYSTEMS

- Bus interface - fan-out
- Timing Variations
- Sampling Clock Jitter
- Logic Noise

Figure 11.64

#### *Fan-Out*

All Analog Devices' DSP processors, and most of their DSP ADCs, have TTL-compatible CMOS logic ports. The inputs have  $V_{il(max)}$  of 0.8V and  $V_{ih(min)}$  of 2.0V, while the outputs have  $V_{ol(max)}$  of 0.4V and  $V_{oh(min)}$  of 2.4V at particular currents. The DSP processors are also rated for the capacitive load that they will drive without degradation of their timing.

In order to determine the fan-out of such devices, it is necessary to consider the current that they are called upon to source and sink, and the capacitance that they will see. This is done from the data sheets of the devices that they will be called upon to drive.

## FACTORS LIMITING LOGIC FAN-OUT

- Maximum available source current (logic high):  
Dominant factor for *resistive* loads.
- Maximum available sink current (logic low):  
Dominant factor for *TTL* loads.
- Maximum permitted node capacitance:  
Dominant factor for *CMOS* loads.
- Node capacitance has contributions both from the input capacitances of gates on the node and from wiring and PC board tracks associated with the load.

Figure 11.65

Consider a typical fast TTL gate, such as the 74F32 OR-gate. Its maximum input high current ( $I_{ih(max)}$ ) is  $20\mu A$ , its maximum input low current ( $I_{il(max)}$ ) is  $0.6mA$ , and its maximum

input capacitance is  $5pF$ . An ADSP-2100 will source  $1mA$  when its output is high, it will sink  $4mA$  when its output is low, and it will drive capacitance of up to  $100pF$ .

## ADSP-2100 DRIVE CAPABILITY

- Will Drive 100 pF
- Will drive 1 mA at logic 1 ( $> 2.4$  V)
- Will sink 4 mA at logic 0 ( $< 0.4$  V)
- Therefore it will drive:
  - ◆ 22 74ACT CMOS Gates (= 99 pF, + 22  $\mu$ A)
  - ◆ 10 74LS Schottky TTL Gates (= -4 mA)
  - ◆ 7 74F Schottky TTL Gates (= -4.2 mA)
  - ◆ 1 Grounded 2.4 K resistor (= 1 mA)
  - ◆ Or any combination of loads which does not exceed a total capacitance of 100 pF, a total drain of 1 mA at logic 1, and a total source of 4 mA at logic 0.  
(Remember to allow for the capacitance of PCB tracks and wiring)

Figure 11.66

The ADSP-2100 will therefore drive the capacitance of 20 74F32 gates, it will drive the input current of fifty such gates in the logic 1 (high) state, but it will sink the input current of only 6.7 (in practical terms, 7) such gates. The lowest of these is evidently the fan-out which it will drive.

In typical systems, it is likely that a device will be called upon to drive a mixture of devices, so the calculations will be more complex - but the basic principle will be the same. In most systems involving TTL, the fan-out will be limited by the sink current, but in CMOS systems, the node capacitance is likely to be the limiting factor. The above calculations do not consider the capacitance of the PC tracks and any cables which the device may be called upon to drive, but such capacitance can sometimes be a limiting factor, and should always be considered, if only to be eliminated.

Most data converters have less powerful output stages than processors, and their fan-out is lower. Additionally, the return current of the output drive from a converter will flow in the system analog ground (for reasons discussed earlier in this section), and should therefore be kept as low as possible in order to minimize digital noise in the analog part of the system.

This is best achieved by using CMOS, rather than TTL logic. The DC input currents of CMOS are orders of magnitude lower than those of TTL. However, the input capacitances are comparable, so the switching transients are not much lower. It is therefore advisable to buffer ADC outputs with an external buffer to minimize digital output currents from the ADC. Such a buffer will also help to isolate the ADC from digital noise in the rest of the system.

### ***Timing Variations***

A common cause of malfunctions in digital systems, and particularly in the digital parts of mixed signal systems, is timing error, which often arises from failure to consider the effects of temperature variations on the system.

The specifications of converters, memories, and processors all contain such parameters as "set-up" and "hold"

times. These are the times, respectively, that data must be present before a clock edge may occur, or that it must remain valid after the edge. At room temperatures, many digital circuits are quite tolerant of operation with set-up and hold times which are shorter than the specified minimum - but at extremes of temperature, they may be more demanding.

## **LOGIC TIMING VARIES WITH TEMPERATURE**

- Specifications such as "set-up" & "hold" (the time a signal must be present before a strobe and the time that it must remain after one, respectively) can vary widely with temperature.
- A system designed with room temperature "typical" values may only perform properly at room temperature, if then.
- Designers **MUST** use min/max specifications at temperature extremes to ensure correct operation at all times.

**Figure 11.67**

Where a system consists only of digital circuitry, it is likely (but not certain) that changes in input and output timing will behave similarly, so that systems continue to function over temperature. Where ADCs or DACs are interfacing with digital systems, the very different processes used for the converters may result in timing changes not tracking and performance, or even functionality, suffering.

Engineers designing mixed signal systems should always ascertain that the maximum and minimum timing specifications of all the circuits in their systems are compatible over the full temperature range of intended operation. Where there is any doubt, buffers or monostables should be used as pulse extenders to ensure that all set-up and hold specifications are complied with.

### *Sampling Clock Noise*

As has been mentioned elsewhere in this seminar, phase noise on the clock of a sampled data system is indistinguishable from phase noise on the signal itself, and it is therefore of critical importance to ensure that the sampling clock has sufficient spectral purity that its phase noise is less than the smallest component to be detected in the signal under analysis.

To achieve this, the sampling clock should be isolated as much as possible

from the noise present in the digital parts of the system. In particular, buffers used for the sampling clock should, ideally, be on separate chips, with separately decoupled supplies, from the remainder of the digital system, and the sampling clock signal lines should not be located where they can pick up digital noise from the rest of the system.

## SAMPLING CLOCK NOISE

- Phase noise of the clock must be less than the minimum signal to be detected in the system.
- Therefore the sample clock signal must be protected from digital noise.

BUT

- Clocks are digital and can corrupt the analog part of the system.
- Therefore sampling clock lines must be kept separate from both the analog and the digital parts of the system.
- The sampling clock must use an oscillator with low phase noise.

Figure 11.68

Of course, the sampling clock is itself a digital signal. It has as much potential for causing noise in the analog part of the system as any other digital signal. In fact, due to its presence in the converter and SHA sections of a system, it is generally the leading suspect for noise. We therefore see that a sampling

clock is very inconvenient, as it must be isolated from both the analog and digital parts of the system.

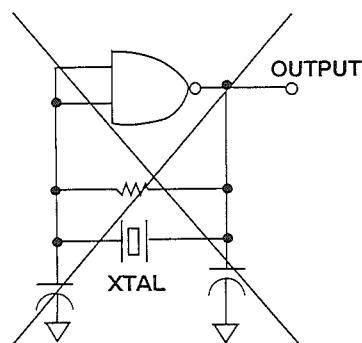
The sampling clock generator must also have adequate spectral purity. RC and other relaxation oscillators just will not do, since amplitude noise in whatever

circuit functions as a comparator will appear as phase noise on the output signal. LC oscillators have better phase noise, but the lowest noise is obtained with the use of a quartz crystal oscillator. For very high speed clocks, a SAW (surface acoustic wave) oscillator is preferable.

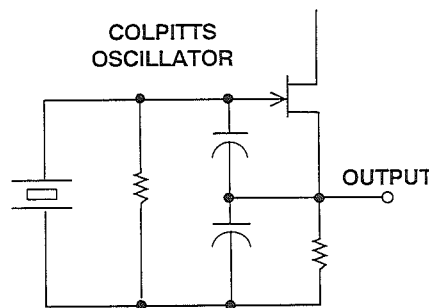
A popular design of quartz crystal oscillator uses a resistor, one or more logic gates, a quartz crystal, and a couple of capacitors. The design is not popular with engineers who understand

quartz crystals or oscillators - such designs have bad phase noise, and are liable to overdrive the quartz crystal (not enough to shatter it, as sometimes happened with self-excited crystal-controlled transmitters using vacuum tubes, but enough to affect its long-term stability). The only justification for the use of such oscillators is in watch and clock circuits, where the low voltages involved minimize the overdrive, and the phase noise is integrated over long periods, and so is unimportant.

## OSCILLATORS



Crystal oscillators built with logic gates have large phase noise.



Low noise crystal oscillators are easily designed with discrete components.

Figure 11.69

Ideally, quartz oscillators should use discrete bipolar and FET devices in the circuits recommended by the crystal manufacturers. These circuits are optimized for both crystal drive level

and phase noise. The output signal can then be amplified (possibly with a logic gate at this point) to drive the converters.



## ***Logic Noise***

One of the most common causes of loss of performance in mixed signal systems is degradation of analog performance by noise from the digital parts of the system. We have already discussed at some length how this digital noise may be isolated from the sensitive analog parts of the system, but it is also worthwhile considering how this noise may be diminished at its source.

It is well-known that TTL is noisy. This is partly because the "totem pole" output stage structure acts as a short-circuit on the supply for a nanosecond or so during switching - giving rise to a large current spike, partly because the current flowing in the input changes, and changes quickly, between logic 0

and logic 1, and partly because the output swing, which takes place in a few nanoseconds, is several volts.

High speed CMOS does not have the change in input current (although there is a capacitance charging current pulse during switching, this is smaller), but may draw a supply current pulse during switching, and certainly has a large output swing with a large  $dV/dT$ .

4000-Series CMOS is almost 20 years old and slow. It is also widely available, cheap, resistant to RFI, and quite remarkably noise free, since it has low output  $dV/dT$  and does not generate a supply current pulse.

## **LOGIC NOISE**

- TTL has large voltage swings large, fast input and output current pulses and asymmetrical circuitry.
- HCMOS has large voltage swings large, fast output current pulses and symmetrical circuitry.
- 4000-Series CMOS is old, slow, cheap and very quiet.
- ECL has smaller voltage swings and smaller current surges than TTL and HCMOS even though it is faster.
- There is no single ideal logic family

**Figure 11.70**

ECL also draws almost constant current during switching (unless it is driving asymmetrical loads), and has much smaller output voltage swings than TTL or CMOS. Thus, although ECL is faster than TTL and CMOS, it tends to generate less noise (Reference 8).

No single logic family is ideal for all applications (otherwise there would only be one logic family), but it is safe to conclude that TTL should not be used where its noise can corrupt precision analog circuitry but should be replaced by CMOS.

Where only low speeds are necessary, 4000 CMOS has overwhelming noise

advantages, but may not be available in all necessary configurations, and does not interface well with TTL (although it will interface with high speed CMOS families).

In high speed systems, where noise is important, ECL may offer noise advantages at the interface between the analog and digital parts of the system, even though high speed CMOS is capable of the speeds being used. It is not necessary to use ECL throughout the system - just where its lower noise is advantageous.

## PROBLEM AREAS

### *Limitations of SPICE Modeling*

As we have seen, real electronic circuits contain many "components" which were not present in the circuit diagram, but which are there because of the physical properties of conductors, circuit boards, IC packages, etc. These components are difficult, if not impossible, to incorporate into computer modeling software, and yet they have substantial effects on circuit performance at high resolutions, or high frequencies, or both.

It is therefore inadvisable to use SPICE modeling or similar software to predict the ultimate performance of such high performance analog circuits. After modeling is complete, the performance must be verified by experiment.

This is not to say that SPICE modeling is valueless - far from it. Most modern high performance analog circuits could never have been developed without the aid of SPICE and similar programs, but

it must be remembered that such simulations are only as good as the models used, and these models are not perfect. We have seen the effects of parasitic components arising from the conductors, insulators and components on the PCB, but it is also necessary to appreciate that the models used within SPICE simulations are not perfect models.

Consider an operational amplifier. It contains some 20-40 transistors, almost as many resistors, and a few capacitors. A complete SPICE model will contain all these components, and probably a few of the more important parasitic capacitances and spurious diodes formed by the diffusions in the op-amp chip. This is the model that the designer will have used to evaluate the device during his design. In simulations, such a model will behave very like the actual op-amp, but not exactly.

## SPICE MODELING

- SPICE modeling is a powerful tool for predicting the performance of analog circuits.

### HOWEVER

- Models omit real-life effects
- No model can simulate all the parasitic effects of discrete components and a PCB layout.

### THEREFORE

- Prototypes must be built and proven before production.

Figure 11.71

However, this model is not published, as it contains too much information which would be of use to other semiconductor companies who might wish to copy or improve on the design. It would also take far too long for a simulation of a system containing such models of a number of op-amps to reach a useful result. For these, and other reasons, the

SPICE models of analog circuits published by manufacturers or software companies are “macro” models, which simulate the major features of the component, but lack some of the fine detail. Consequently, SPICE modeling does not always reproduce the exact performance of a circuit and should always be verified experimentally.

## Sockets

It is tempting to mount expensive ICs in sockets, rather than soldering them in circuit — especially during circuit

development. Engineers would do well not to succumb to this temptation.

## USE OF SOCKETS WITH HIGH PERFORMANCE ANALOG CIRCUITS

**DON'T!** (If at all possible)

- Use "Pin sockets" or "Cage jacks" such as Amp Part No: 5-330808-3 or 5-330808-6 (Capped & uncapped respectively).
- Always test the effect of sockets by comparing system performance with and without the use of sockets.
- Do not change the type of socket used without evaluating the effects of the change on performance.

Figure 11.72

Sockets add resistance, inductance, and capacitance to the circuit and may degrade performance to quite unacceptable levels. When this occurs, though, it is always the IC manufacturer who is blamed - not the use of a socket. Even low profile, low insertion force sockets cannot be relied upon not to degrade the performance of high performance (high speed or high precision or, worst of all, both) devices, and as the socket ages and the board suffers vibration, the contact resistance of low insertion force sockets is very likely to rise. Where a socket must be used, the least loss of performance is achieved by using individual pin sockets (sometimes called "cage jacks") to make up a multi-pin socket in the PCB itself.

It really is best not to use IC sockets with high performance analog and

mixed signal circuits. If their use can be avoided, it should be. However, at medium speeds and medium resolutions, the trade-off between performance and convenience may fall on the side of convenience. It is very important, when sockets are used, to evaluate circuit performance with and without the socket chosen to ensure that the type of socket chosen really does have minimal effect on the way that the circuit behaves. The effects of a change of socket on the circuit should be evaluated as carefully as a change of IC would be, and the drawings should be prepared so that the change procedures for a socket are as rigorous as for an IC - in order to prevent a purchase clerk who knows nothing of electronics from devastating the system performance in order to save five cents on a socket.

### ***Prototyping High Performance Analog Circuitry***

As we have seen, circuit board layout is part of the circuit design of all high performance analog circuits.

Prototyping techniques derived from the "node" theory, while ideal for logic breadboarding at low and medium speeds, are quite unsuitable for any analog circuits, or even for very fast digital ones. Vector board and wire wrap prototyping will tell an engineer nothing about the behavior of a properly laid out version of the analog circuit.

The best technique for analog prototyping is to use a prototype of the final PCB - certainly no design is complete until the final PCB layout has been proved to give the required performance. Nevertheless, this approach may be a little limiting where a number of different possibilities are to be evaluated, or for a multiscard system.

## **PROTOTYPING MIXED SIGNAL CIRCUITRY**

- **NEVER** use vector boards or wire-wrap for the analog parts of the system (they can be invaluable for data buses and address lines in the digital part).
- Wherever possible avoid the use of sockets for analog ICs.
- Use a prototype of your final PCB layout as early as possible.

**Figure 11.73**

In this case, components should be mounted on a board having a continuous copper ground plane (ideally on both sides of the board, though while convenient, this is not essential), with ground connections made to the plane, and short point to point wiring made above and below it. The overall component placing and signal routing should be as close as possible to the planned final layout.

As we have already indicated, IC sockets can degrade the performance of analog ICs. While directly soldered components are ideal for prototyping, an IC socket made of pin sockets mounted in the ground plane board may be acceptable (clear the copper, on both sides of the board, for about 0.5mm around each ungrounded pin socket - solder the grounded ones to ground on both sides of the board).

Allowing wiring to float in the air can be a little tricky. There is a breadboarding system which is conceptually very similar to that described above, but which provides adhesive PC pads which stick to the ground plane and allow more rigid component mounting and wiring. This system is manufactured by Wainwright Instruments, and is known as "Minimount" in Europe and "Solder Mounts" in the USA. The manufacturer's and distributors' addresses are given in the references at the end of this section (Reference 9).

Manufacturer's evaluation boards are also useful in system prototyping, since they have already been optimized for best performance. Analog Devices offers

many evaluation boards for a wide array of products. They offer the designer an excellent starting point for the layout.

When the prototype layout is transferred to a CAD system for PCB layout, it is important to disable, or at any rate override where necessary, any automatic routing or component placing software. The criteria used by such software are more closely related to "node" theory, and aesthetically pleasing rows of components (which, admittedly, are also easier on automatic component placing machinery) than to optimizing stray inductance and capacitance and minimizing common ground impedances.

## ADDITIONAL PROTOTYPING HINTS

- Pay *equal* attention to signal routing, component placing and supply decoupling in *both* the prototype and the final design.
- Verify performance as well as functionality at each stage of the design.
- For "freehand" prototyping use a copper-clad board, mount components to it by their ground pins and wire the remaining connections point-to-point (use Wainwright Instruments' Minimount/Solder Mount adhesive PC pads if aerial point-to-point wiring seems too fraught with peril).

Figure 11.74

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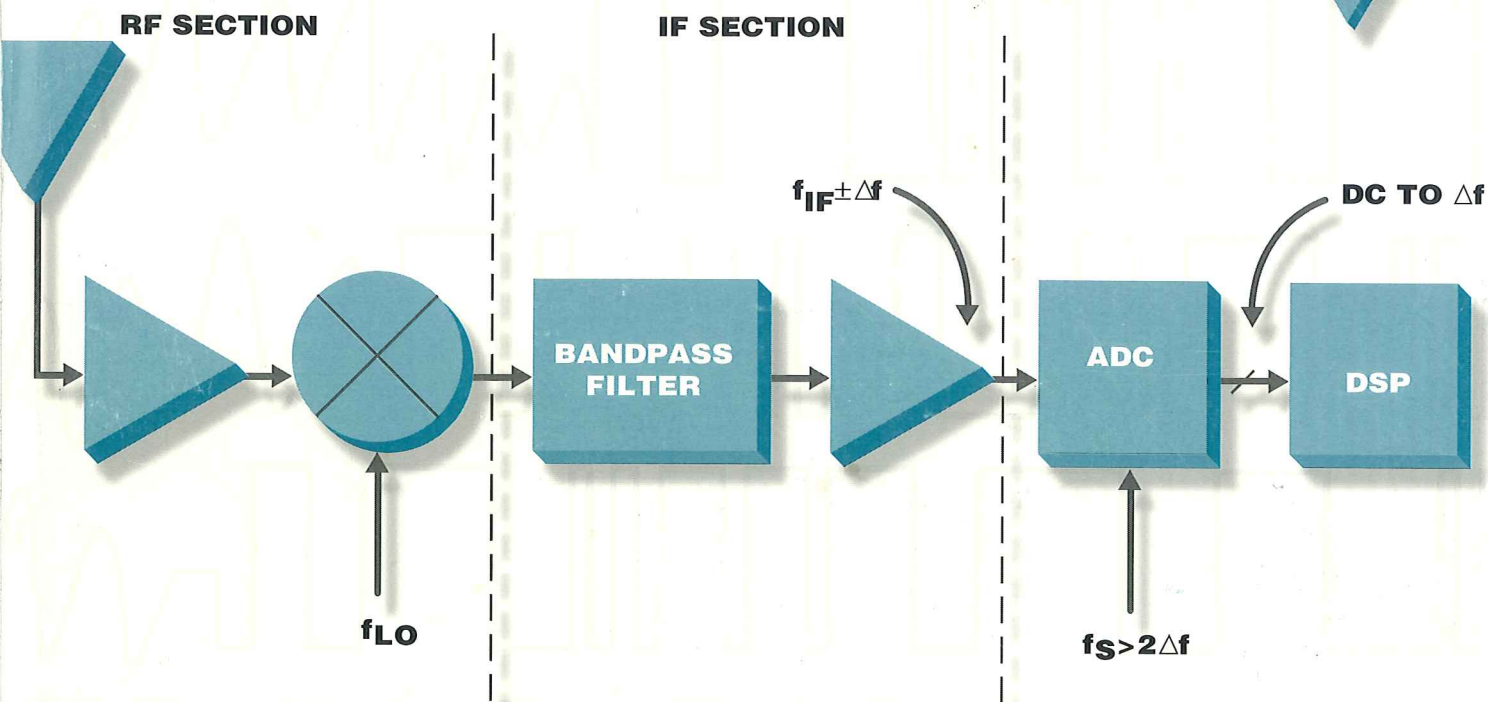
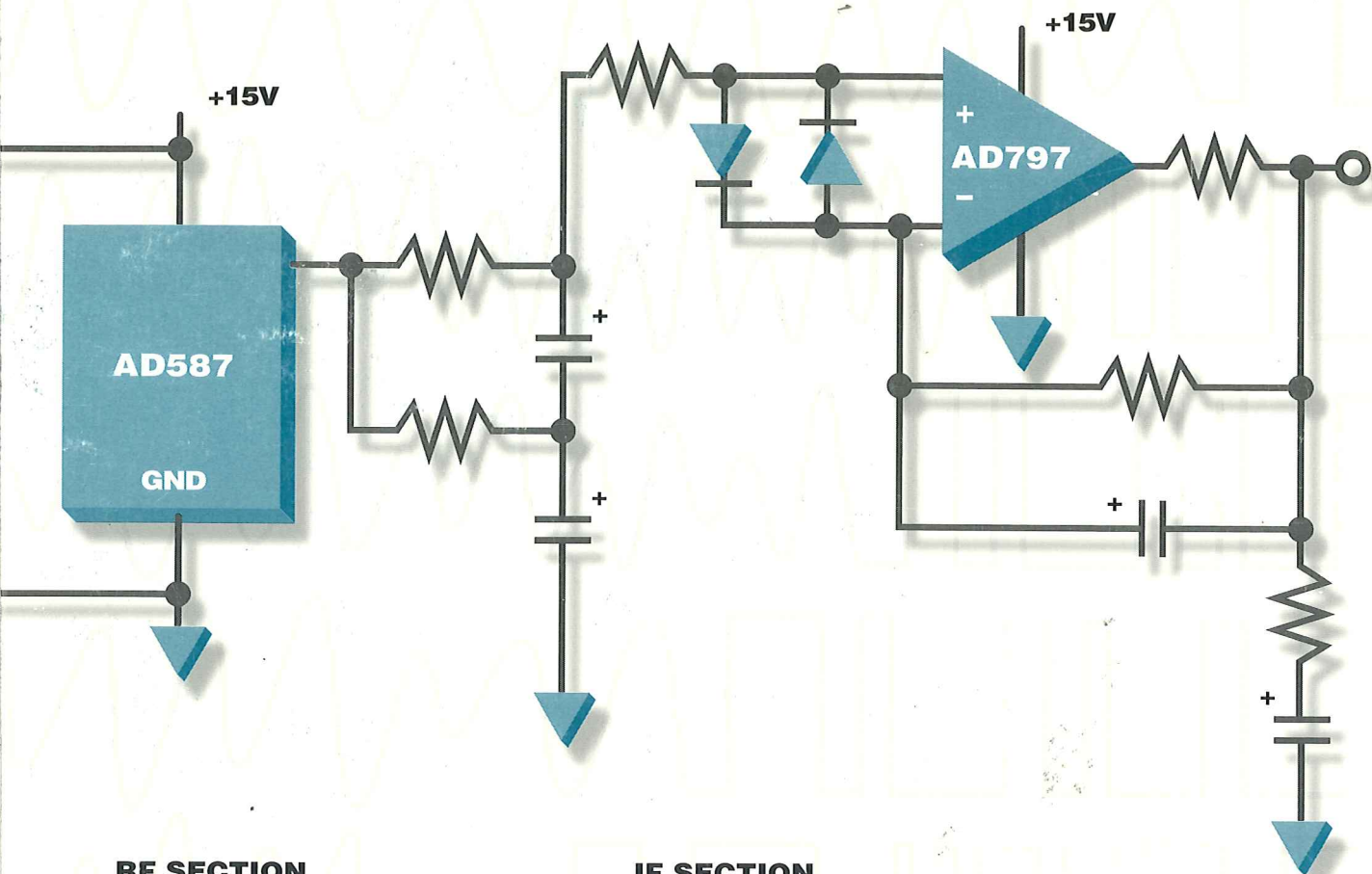
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